1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
8	0001102717	ENGINEERING RELEASED	2011-04-07

J40G MLB-GS

Thu Apr 7 15:35:59 2011

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DOCUMENTS / BOARDS / ASSEMBLIES

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8937	1	SCHEM,MLB-GS,J40G	SCH		
820-3059	1	PCBF,MLB-GS,J40G	MLB		
639-1822		PCBA,MLB-GS,GDDR-HYNIX,J40G			
639-1823		PCBA,MLB-GS,GDDR-SAMSUNG,J40G			
085-2724	1	DEV LIST,MLB-GS,J40G	DEV1		DEVELOPMENT_LIST

DRAWING
TITLE=SHORTSTACK
ABBREV=DRAWING

DRAWING TITLE: SCH,MLB-GS,J40G

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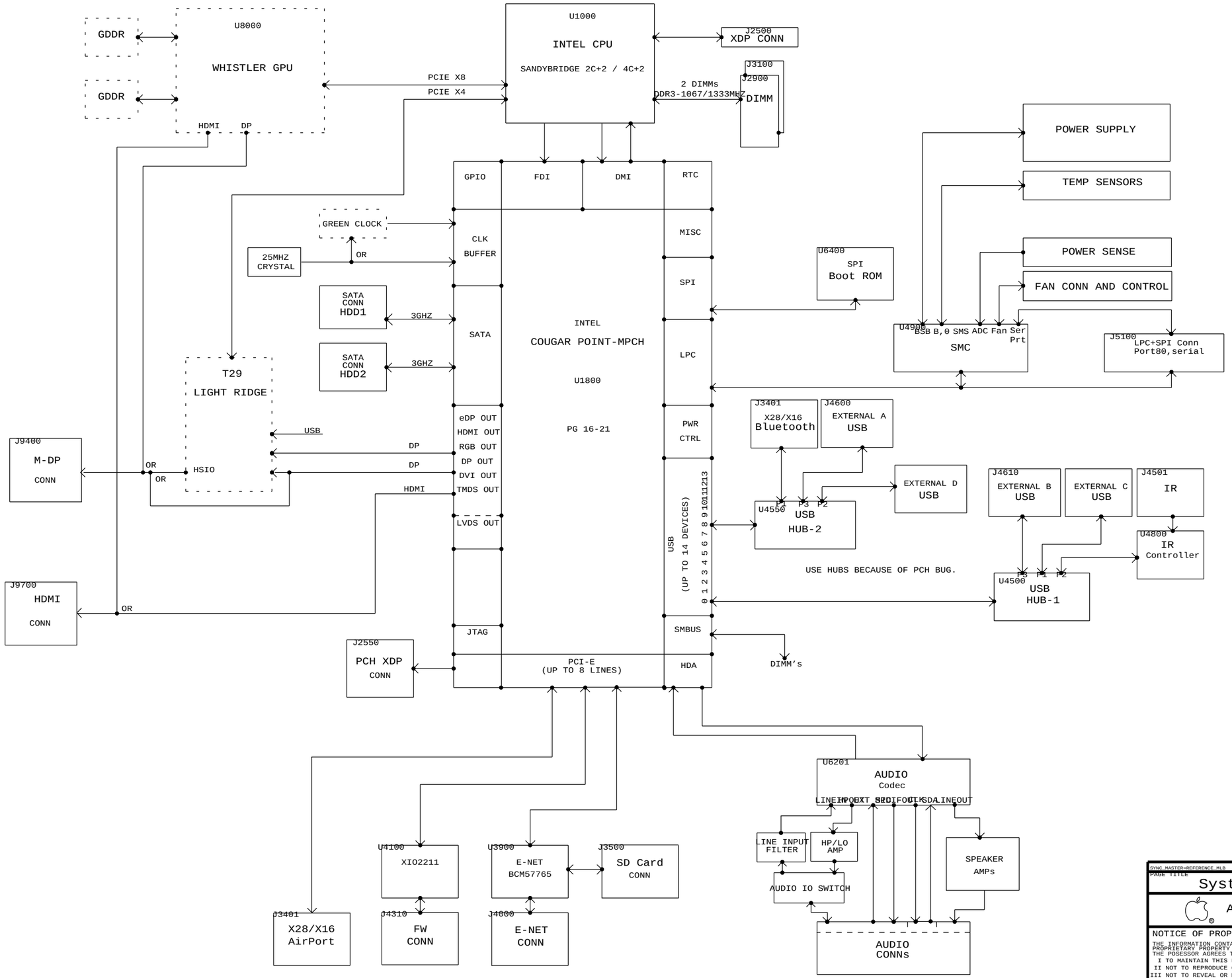

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System Block Diagram

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Power Block Diagram

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PLATFORM CONTROL HUB (PCH)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3980	1	IC,PCH,COUGAR_POINT,QMZQ,SUPER SKU,BGA,ES1/B0	U1800	CRITICAL	COUGAR_POINT:B0
337S4022	1	IC,PCH,COUGAR_POINT,QXXX,SUPER SKU,BGA,QS/B1	U1800	CRITICAL	COUGAR_POINT:B1
337S4025	1	IC,PCH,COUGAR_POINT,QNJH,SUPER SKU,BGA,QS/B2	U1800	CRITICAL	COUGAR_POINT:B2
337S4029	1	IC,PCH,COUGAR_POINT,SLH9D,BD82HM65,BGA,PRQ/B2	U1800	CRITICAL	COUGAR_POINT:B2_PRQ_OLD
337S4087	1	IC,PCH,COUGAR_POINT,SLJ4P,BD82HM65,BGA,PRQ/B3	U1800	CRITICAL	COUGAR_POINT:B3_PRQ

PROGRAMMED PARTS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
341T0338	1	IC,EFI BOOTROM,J40	U6400	CRITICAL		BASE: 335S0770,335S0769
341T0335	1	IC,SMC,J40G	U4900	CRITICAL	SMC:J40G	BASE: 338S0895
341T0336	1	IC,SMC,J40I	U4900	CRITICAL	SMC:J40I	BASE: 338S0895
341T0337	1	IC,SMC,J40S	U4900	CRITICAL	SMC:J40S	BASE: 338S0895
341T0340	1	IC,IR CONTROLLER,J40	U4700	CRITICAL		BASE: 338S0375
341T0341	1	IC,ENET ROM J40	U3990	CRITICAL		BASE: 335S0539, 335S0663, OR 335S0800

NON-SCHEMATIC PARTS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-6838	1	LBL,SERIAL NUMBER	LBL		

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0286	128S0248	?	?	39UF CAP FROM SANYO AND CHEMI-CON
132S0099	132S0203	?	?	0.1UF CAP,X7R
138S0676	138S0691		?	22UF CAP FROM MURATA
138S0681	138S0638		?	10UF CAP FROM TAIYO YUDEN
152S0138	152S0694	?	?	INDUCTOR FROM VISHAY
152S1447	152S1269	?	?	INDUCTOR FROM CYNTEC
152S1282	152S1155	?	?	INDUCTOR FROM CYNTEC
152S1366	152S1289	?	?	INDUCTOR FROM TOKO
155S0641	155S0397	?	?	FERRITE FROM LAIRD
155S0457	155S0329		ALL	MAG LAYERS ALT TO MURATA
157S0058	157S0055		ALL	DELTA ALT TO TDK MAGNETICS
353S3196	353S3326	?	?	DIFFERENT TEMP RATING
371S0679	371S0652	?	?	PIN DIODE FROM NXP
376S0914	376S0881		?	SI7121DN AS ALTERNATE
376S0957	376S0999		?	DUAL FET FROM FAIRCHILD
376S0958	376S0953		?	DUAL FET FROM FAIRCHILD
376S1000	376S0960		?	DUAL FET FROM FAIRCHILD
376S0972	376S0612		?	FET FROM ROHM
376S0613	376S0859		?	OLDER DUAL FET FROM TOSHIBA
376S0855	376S0859		?	DUAL FET FROM DDS
376S0977	376S0859		?	DUAL FET FROM DDS
138S0703	138S0648		?	CAP FROM MURATA
197S0339	197S0179		?	OSC. FROM SITIME
376S0926	376S0610		?	DUAL FET FROM FAIRCHILD
376S0572	376S0659		?	FET FROM ALPHA OMEGA
377S0124	377S0057		?	VARISTOR FROM AMOTECH

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COMMON PARTS TABLE

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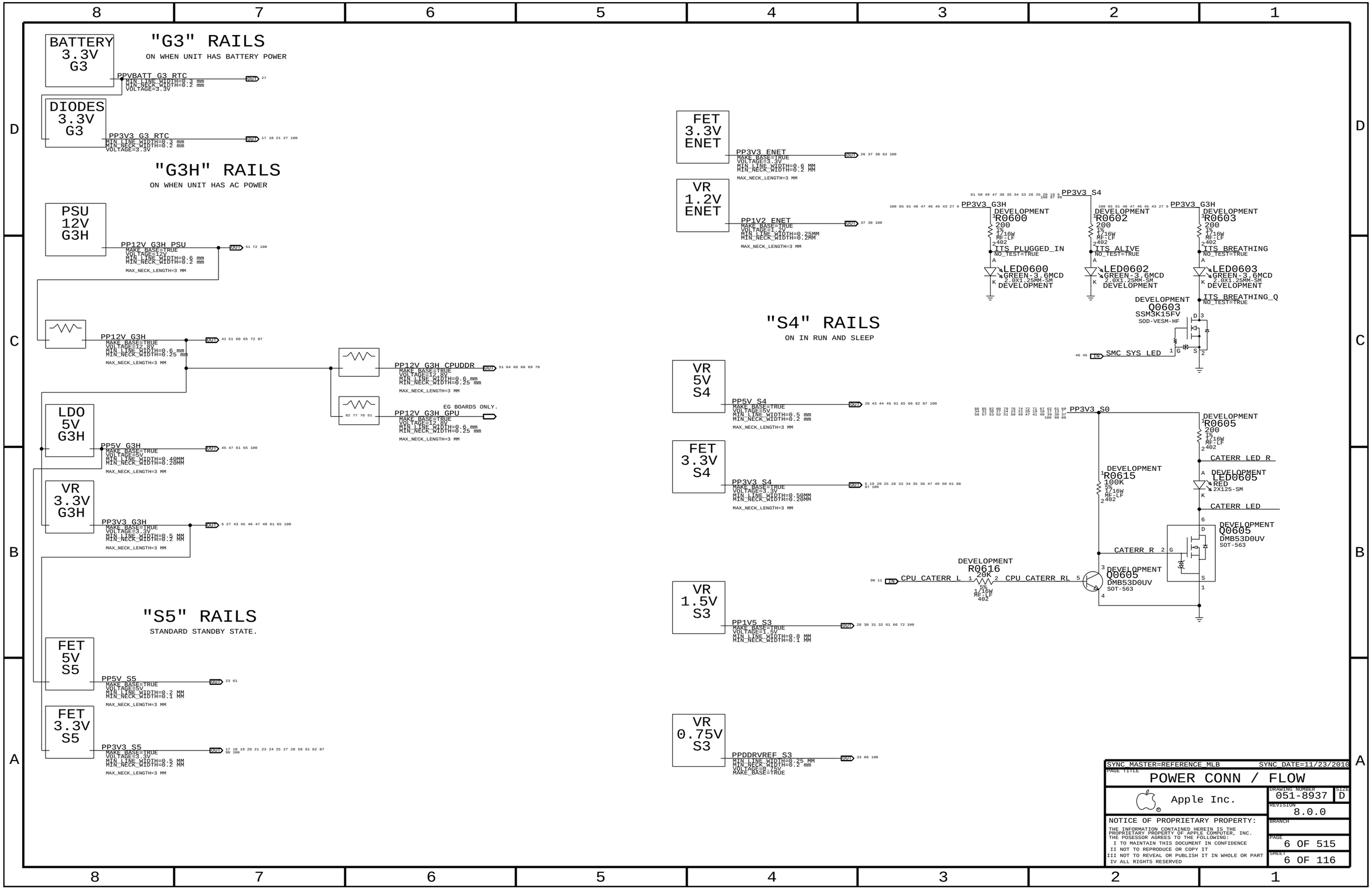
"G3" RAILS
ON WHEN UNIT HAS BATTERY POWER
BATTERY 3.3V G3
PPVBATT_G3_RTC
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
OUT 27
DIODES 3.3V G3
PP3V3_G3_RTC
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
OUT 17 18 21 27 100
"G3H" RAILS
ON WHEN UNIT HAS AC POWER
PSU 12V G3H
PP12V_G3H_PSU
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
MAX_NECK_LENGTH=3 MM
OUT 51 72 100
PP12V_G3H
MAKE_BASE=TRUE
VOLTAGE=12.8V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
MAX_NECK_LENGTH=3 MM
OUT 41 51 60 65 72 87
PP12V_G3H_CPUDDR
MAKE_BASE=TRUE
VOLTAGE=12.8V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
MAX_NECK_LENGTH=3 MM
OUT 51 64 66 68 69 70
EG BOARDS ONLY.
PP12V_G3H_GPU
MAKE_BASE=TRUE
VOLTAGE=12.8V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
MAX_NECK_LENGTH=3 MM
82 77 76 51
LDO 5V G3H
PP5V_G3H
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.40MM
MIN_NECK_WIDTH=0.20MM
MAX_NECK_LENGTH=3 MM
OUT 45 47 61 65 100
VR 3.3V G3H
PP3V3_G3H
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
MAX_NECK_LENGTH=3 MM
OUT 6 27 43 45 46 47 48 61 65 100
"S5" RAILS
STANDARD STANDBY STATE.
FET 5V S5
PP5V_S5
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.1 MM
MAX_NECK_LENGTH=3 MM
OUT 23 61
FET 3.3V S5
PP3V3_S5
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
MAX_NECK_LENGTH=3 MM
OUT 17 18 19 20 21 23 24 25 27 28 59 61 62 87 98 100
FET 3.3V ENET
PP3V3_ENET
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
MAX_NECK_LENGTH=3 MM
OUT 26 37 38 62 100
VR 1.2V ENET
PP1V2_ENET
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.25MM
MIN_NECK_WIDTH=0.2MM
MAX_NECK_LENGTH=3 MM
OUT 37 38 100
PP3V3_S4
PP3V3_G3H
DEVELOPMENT
R0600
200
1%
1/16W
MF-LF
402
ITS_PLUGGED_IN
NO_TEST=TRUE
LED0600
GREEN-3.6MCD
2.0X1.25MM-SM
DEVELOPMENT
DEVELOPMENT
R0602
200
1%
1/16W
MF-LF
402
ITS_ALIVE
NO_TEST=TRUE
LED0602
GREEN-3.6MCD
2.0X1.25MM-SM
DEVELOPMENT
PP3V3_G3H
DEVELOPMENT
R0603
200
1%
1/16W
MF-LF
402
ITS_BREATHING
NO_TEST=TRUE
LED0603
GREEN-3.6MCD
2.0X1.25MM-SM
DEVELOPMENT
ITS_BREATHING_Q
NO_TEST=TRUE
DEVELOPMENT
Q0603
SSM3K15FV
SOD-VESM-HF
SMC_SYS_LED
IN 46 45
"S4" RAILS
ON IN RUN AND SLEEP
VR 5V S4
PP5V_S4
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
MAX_NECK_LENGTH=3 MM
OUT 28 43 44 45 61 65 66 82 87 100
FET 3.3V S4
PP3V3_S4
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
MAX_NECK_LENGTH=3 MM
OUT 6 19 20 25 28 33 34 35 38 47 49 50 61 86 87 100
PP3V3_S0
DEVELOPMENT
R0605
200
1%
1/16W
MF-LF
402
CATERR_LED_R
DEVELOPMENT
LED0605
RED
2X125-SM
CATERR_LED
DEVELOPMENT
Q0605
DMB53D0UV
SOT-563
DEVELOPMENT
R0615
100K
5%
1/16W
MF-LF
402
CATERR_R
DEVELOPMENT
R0616
20K
5%
1/16W
MF-LF
402
CPU_CATERR_L
CPU_CATERR_RL
IN 90 11
DEVELOPMENT
Q0605
DMB53D0UV
SOT-563
VR 1.5V S3
PP1V5_S3
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.8 MM
MIN_NECK_WIDTH=0.1 MM
OUT 28 30 31 32 61 66 72 100
VR 0.75V S3
PPDDRVREF_S3
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE
OUT 33 66 100
SYNC_MASTER=REFERENCE_MLB
SYNC_DATE=11/23/2016
PAGE TITLE
POWER CONN / FLOW
Apple Inc.
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051-8937
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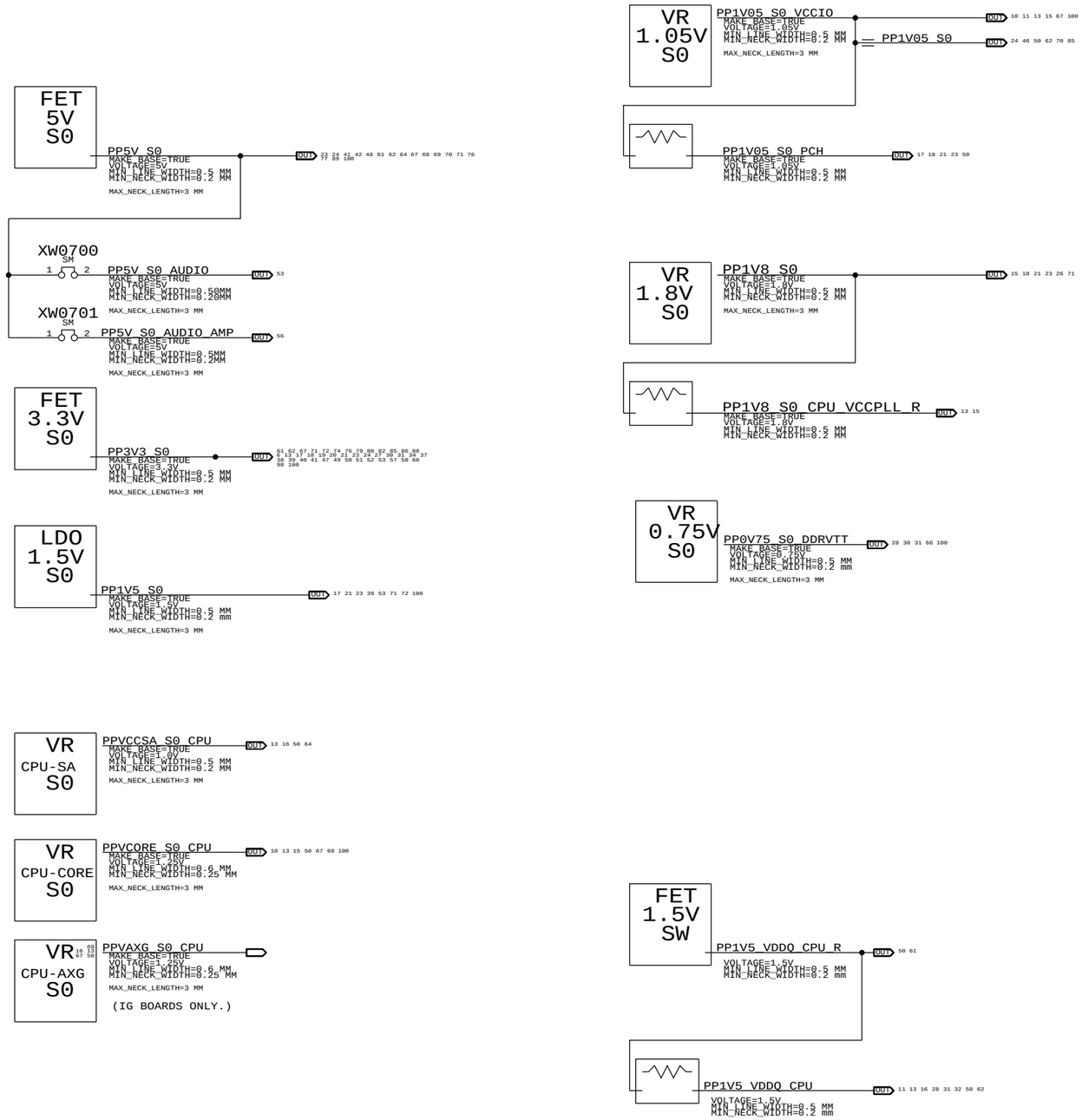

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POWER FLOW CONT.

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EXTERNAL GRAPHICS

DISCONNECT INTEGRATED GRAPHICS

DON'T NEED FDI BUS

=FDI_DATA_P<7..0>	MAKE_BASE=TRUE	NC_FDI_CPU_DATAP<7..0>	
=FDI_DATA_N<7..0>	MAKE_BASE=TRUE	NC_FDI_CPU_DATAN<7..0>	
=FDI_INT	MAKE_BASE=TRUE	PD_FDI_CPU_INT	
=FDI_FSYNC<0>	MAKE_BASE=TRUE	PD_FDI_CPU_FLSYNC	
=FDI_FSYNC<1>			
=FDI_LSYNC<0>			
=FDI_LSYNC<1>			

R0831 1K 5% 1/16W MF-LF 402 — R0832 1K 5% 1/16W MF-LF 402

NC_FDI_PCH_DATAP<7..0>	MAKE_BASE=TRUE	FDI_DATA_P<7..0>	
NC_FDI_PCH_DATAN<7..0>	MAKE_BASE=TRUE	FDI_DATA_N<7..0>	
NC_FDI_PCH_INT	MAKE_BASE=TRUE	FDI_INT	
NC_FDI_PCH_FSYNC<1..0>	MAKE_BASE=TRUE	FDI_FSYNC<1..0>	
NC_FDI_PCH_LSYNC<1..0>	MAKE_BASE=TRUE	FDI_LSYNC<1..0>	

INTERNAL DISPLAY PORT

=IG_DP_EXTA_DDC_CLK	MAKE_BASE=TRUE	NC_IG_DP_EXTA_DDC_CLK
=IG_DP_EXTA_DDC_DATA	MAKE_BASE=TRUE	NC_IG_DP_EXTA_DDC_DATA
=IG_DP_EXTA_AUXCH_C_N	MAKE_BASE=TRUE	NC_IG_DP_EXTA_AUXCH_CN
=IG_DP_EXTA_AUXCH_C_P	MAKE_BASE=TRUE	NC_IG_DP_EXTA_AUXCH_CP
=IG_DP_EXTA_HPD	MAKE_BASE=TRUE	NC_IG_DP_EXTA_HPD
=IG_DP_EXTA_ML_C_N<3..0>	MAKE_BASE=TRUE	NC_IG_DP_EXTA_ML_CN<3..0>
=IG_DP_EXTA_ML_C_P<3..0>	MAKE_BASE=TRUE	NC_IG_DP_EXTA_ML_CP<3..0>

HDMI

=IG_HDMI_LS_SCL	MAKE_BASE=TRUE	NC_IG_HDMI_LS_SCL
=IG_HDMI_LS_SDA	MAKE_BASE=TRUE	NC_IG_HDMI_LS_SDA
=IG_HDMI_LS_HPD	MAKE_BASE=TRUE	NC_IG_HDMI_LS_HPD
=IG_HDMI_DATA_C_N<2..0>	MAKE_BASE=TRUE	NC_IG_HDMI_DATA_CN<2..0>
=IG_HDMI_DATA_C_P<2..0>	MAKE_BASE=TRUE	NC_IG_HDMI_DATA_CP<2..0>
=IG_HDMI_CLK_C_N	MAKE_BASE=TRUE	NC_IG_HDMI_CLK_CN
=IG_HDMI_CLK_C_P	MAKE_BASE=TRUE	NC_IG_HDMI_CLK_CP

CONNECT EXTERNAL GRAPHICS

PCIE

=PEG_D2R_N<7..0>	MAKE_BASE=TRUE	PEG_D2R_N<7..0>
=PEG_D2R_P<7..0>	MAKE_BASE=TRUE	PEG_D2R_P<7..0>
=PEG_R2D_C_N<7..0>	MAKE_BASE=TRUE	PEG_R2D_C_N<7..0>
=PEG_R2D_C_P<7..0>	MAKE_BASE=TRUE	PEG_R2D_C_P<7..0>

EXTERNAL DISPLAY PORT

=EG_DP_EXTA_DDC_CLK	MAKE_BASE=TRUE	DP_EXTA_DDC_CLK
=EG_DP_EXTA_DDC_DATA	MAKE_BASE=TRUE	DP_EXTA_DDC_DATA
=EG_DP_EXTA_AUXCH_C_P	MAKE_BASE=TRUE	DP_EXTA_AUXCH_C_P
=EG_DP_EXTA_AUXCH_C_N	MAKE_BASE=TRUE	DP_EXTA_AUXCH_C_N
=EG_DP_EXTA_HPD	MAKE_BASE=TRUE	DP_EXTA_HPD
=EG_DP_EXTA_ML_C_N<3..0>	MAKE_BASE=TRUE	DP_EXTA_ML_C_N<3..0>
=EG_DP_EXTA_ML_C_P<3..0>	MAKE_BASE=TRUE	DP_EXTA_ML_C_P<3..0>

HDMI

=EG_HDMI_DDC_CLK	MAKE_BASE=TRUE	HDMI_LS_SCL
=EG_HDMI_DDC_DATA	MAKE_BASE=TRUE	HDMI_LS_SDA
=EG_HDMI_HPD	MAKE_BASE=TRUE	HDMI_LS_HPD
=EG_HDMI_C_N<2..0>	MAKE_BASE=TRUE	HDMI_DATA_C_N<2..0>
=EG_HDMI_C_P<2..0>	MAKE_BASE=TRUE	HDMI_DATA_C_P<2..0>
=EG_HDMI_CLK_N	MAKE_BASE=TRUE	HDMI_CLK_C_N
=EG_HDMI_CLK_P	MAKE_BASE=TRUE	HDMI_CLK_C_P

=SMC_GFX_THROTTLE_L	MAKE_BASE=TRUE	SMC_GFX_THROTTLE_L

=IG_DP_T29SNK0_CTRL_CLK	MAKE_BASE=TRUE	NC_IG_DP_T29SNK0_CTRL_CLK
=IG_DP_T29SNK0_CTRL_DATA	MAKE_BASE=TRUE	NC_IG_DP_T29SNK0_CTRL_DATA
=IG_DP_T29SNK0_AUXCH_C_N	MAKE_BASE=TRUE	NC_IG_DP_T29SNK0_AUXCH_CN
=IG_DP_T29SNK0_AUXCH_C_P	MAKE_BASE=TRUE	NC_IG_DP_T29SNK0_AUXCH_CP
=IG_DP_T29SNK0_HPD	MAKE_BASE=TRUE	NC_IG_DP_T29SNK0_HPD
=IG_DP_T29SNK0_ML_C_N<3..0>	MAKE_BASE=TRUE	NC_IG_DP_T29SNK0_ML_CN<3..0>
=IG_DP_T29SNK0_ML_C_P<3..0>	MAKE_BASE=TRUE	NC_IG_DP_T29SNK0_ML_CP<3..0>

T29

PCIE

=PCIE_T29_D2R_N<3..0>	MAKE_BASE=TRUE	PCIE_T29_D2R_N<3..0>
=PCIE_T29_D2R_P<3..0>	MAKE_BASE=TRUE	PCIE_T29_D2R_P<3..0>
=PCIE_T29_R2D_C_N<3..0>	MAKE_BASE=TRUE	PCIE_T29_R2D_C_N<3..0>
=PCIE_T29_R2D_C_P<3..0>	MAKE_BASE=TRUE	PCIE_T29_R2D_C_P<3..0>

T29 DISPLAY PORT INPUT

=EG_DP_T29SNK0_AUXCH_C_N	MAKE_BASE=TRUE	DP_T29SNK0_AUXCH_C_N
=EG_DP_T29SNK0_AUXCH_C_P	MAKE_BASE=TRUE	DP_T29SNK0_AUXCH_C_P
=EG_DP_T29SNK0_HPD	MAKE_BASE=TRUE	DP_T29SNK0_HPD
=EG_DP_T29SNK0_ML_C_N<3..0>	MAKE_BASE=TRUE	DP_T29SNK0_ML_C_N<3..0>
=EG_DP_T29SNK0_ML_C_P<3..0>	MAKE_BASE=TRUE	DP_T29SNK0_ML_C_P<3..0>

=EG_DP_T29SNK1_AUXCH_C_N	MAKE_BASE=TRUE	DP_T29SNK1_AUXCH_C_N
=EG_DP_T29SNK1_AUXCH_C_P	MAKE_BASE=TRUE	DP_T29SNK1_AUXCH_C_P
=EG_DP_T29SNK1_HPD	MAKE_BASE=TRUE	DP_T29SNK1_HPD
=EG_DP_T29SNK1_ML_C_N<3..0>	MAKE_BASE=TRUE	DP_T29SNK1_ML_C_N<3..0>
=EG_DP_T29SNK1_ML_C_P<3..0>	MAKE_BASE=TRUE	DP_T29SNK1_ML_C_P<3..0>

USED FOR PCH IN GPU CONFIG

ZT0840 STDOFF-4.0OD2.23H-SM

ZT0841 STDOFF-4.0OD2.23H-SM

USED FOR T29 IC

ZT0850 STDOFF-4.0OD1.85H-SM

ZT0851 STDOFF-4.0OD1.85H-SM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0945	1	IC,T29,SLHAJ,FCBGA,15X15MM	U9000	CRITICAL	
335S0550	1	IC,EEPROM,SERIAL,SPI,4KX8,1.8V,MLP8,LF	U9090	CRITICAL	T29ROM:BLANK
341T0342	1	IC,CONF ROM,T29,J40I,S	U9090	CRITICAL	T29ROM:PROG_IS
341T0380	1	IC,CONF ROM,T29,J40G	U9090	CRITICAL	T29ROM:PROG_G
337S3997	1	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29MCU:BLANK
341T0339	1	IC,PROGRMD,T29 PORT MCU,HVQFN25	U9330	CRITICAL	T29MCU:PROG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3151	1	IC,CBTL04DP081,2:1 DP MUX,QFN	U9390	CRITICAL	T29DPMUX:NXP
353S3151	1	IC,CBTL04DP081,2:1 DP MUX,QFN	U9390	CRITICAL	T29DPMUX:BOTH
353S3055	1	IC,PI3VEDP212,2:1 DP MUX,QFN	U9390	CRITICAL	T29DPMUX:PERICOM

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S3055	353S3151	T29DPMUX:BOTH	?	DP MUX FROM PERICOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3936	1	IC,GPU,AMD,WHISTLER-ES,962FCBGA,M2	U8000	CRITICAL	GPU:WHISTLER_ES
337S3969	1	IC,GPU,AMD,WHISTLER-PRO,962FCBGA,M2	U8000	CRITICAL	GPU:WHISTLER_PRO
337S3970	1	IC,GPU,AMD,WHISTLER-XT,962FCBGA,M2	U8000	CRITICAL	GPU:WHISTLER_XT
337S4015	1	IC,GPU,AMD,WHISTLER-LP,962FCBGA,M2	U8000	CRITICAL	GPU:WHISTLER_LP
337S3979	1	IC,GPU,AMD,SEYMOUR-LP,ES1,962BGA,M2	U8000	CRITICAL	GPU:SEYMOUR-ES1

333S0543	2	IC,SGRAM,GDDR5,32MX32.1.25GHz,E-DIE,HF	U8500,U8550	CRITICAL	GDDR:FB_256_SAMSUNG-E
333S0599	2	IC,SGRAM,GDDR5,32MX32.1.25GHZ,G-DIE,HF	U8500,U8550	CRITICAL	GDDR:FB_256_SAMSUNG-G
333S0598	2	IC,SDRAM,GDDR5,32MX32,1.25GHZ,B-DIE,1.35V	U8500,U8550	CRITICAL	GDDR:FB_256_HYNIX

341S3019	1	IC,GPU ROM,J40G,PROG	U8701	CRITICAL	GPUROM:PROG
335S0724	1	IC,GPU ROM,K91/F,K92,BLANK	U8701	CRITICAL	GPUROM:BLANK

SYNC_MASTER=J40G SYNC_DATE=11/23/2010

PAGE TITLE

SPECIFIC ALIASES, TABLES

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CPU / NB HEATSINK MOUNTING HOLES / NUTS

ZT0960
STDOFF-4.5OD.98H-1.1-3.48-TH

ZT0961
STDOFF-4.5OD.98H-1.1-3.48-TH

ZT0962
STDOFF-4.5OD.98H-1.1-3.48-TH

ZT0966
STDOFF-4.5OD.98H-1.1-3.48-TH

ENCLOSURE MOUNTING POSTS

ZT0940
STDOFF-4.5OD10.75H-1.1-3.48-TH

ZT0941
STDOFF-4.5OD10.75H-1.1-3.48-TH

REAR I/O FENCE MOUNTING BOSS

ZT0910
4.0OD1.55H-M1.6X0.35-ST

ZT0912
4.0OD1.55H-M1.6X0.35-ST

ZT0911
4.0OD1.55H-M1.6X0.35-ST

ZT0913
4.0OD1.55H-M1.6X0.35-ST

ZT0914
4.0OD1.55H-M1.6X0.35-ST

SPEAKER BOSS

ZT0915
4.0OD1.55H-M1.6X0.35-ST

To be distributed after simulation

ZH0930 HOLE-VIA
ZH0935 HOLE-VIA
ZH0940 HOLE-VIA
ZH0945 HOLE-VIA
ZH0950 HOLE-VIA
ZH0955 HOLE-VIA
ZH0931 HOLE-VIA
ZH0936 HOLE-VIA
ZH0941 HOLE-VIA
ZH0946 HOLE-VIA
ZH0951 HOLE-VIA
ZH0956 HOLE-VIA
ZH0932 HOLE-VIA
ZH0937 HOLE-VIA
ZH0942 HOLE-VIA
ZH0947 HOLE-VIA
ZH0952 HOLE-VIA
ZH0957 HOLE-VIA
ZH0933 HOLE-VIA
ZH0938 HOLE-VIA
ZH0943 HOLE-VIA
ZH0948 HOLE-VIA
ZH0953 HOLE-VIA
ZH0958 HOLE-VIA
ZH0934 HOLE-VIA
ZH0944 HOLE-VIA
ZH0949 HOLE-VIA
ZH0954 HOLE-VIA

Digital Ground

GND
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
MAX_NECK_LENGTH=3 MM
VOLTAGE=0V
MAKE_BASE=TRUE

57 56 GND_AUDIO_SPKRAMP

DEVELOPMENT
J0900
SM-TP3P4X1P8-TOP

DEVELOPMENT
J0901
SM-TP3P4X1P8-TOP

PLACE ONE ON EACH SIDE OF BOARD
IN EASILY ACCESSIBLE LOCATION.
LABEL "GND".

POGO PINS FOR GROUNDING HEATPIPE ASSEMBLY.

ZP0900
POGO-2.0OD-3.6H-K86-K87
SM

ZP0902
POGO-2.0OD-3.6H-K86-K87
SM

ZP0901
POGO-2.0OD-3.6H-K86-K87
SM

ZP0903
POGO-2.0OD-3.6H-K86-K87
SM

ZP0907
POGO-2.0OD-3.6H-K86-K87
SM

ZP0921
1.4DIA-SHORT-EMI-MLB-M97-M98
SM

ZP0922
1.4DIA-SHORT-EMI-MLB-M97-M98
SM

ZP0920
1.4DIA-SHORT-EMI-MLB-M97-M98
SM

ZP0923
1.4DIA-SHORT-EMI-MLB-M97-M98
SM

BLOWER SUPPORT POST.

ZT0970
STDOFF-3.040D6.1H-1.3-1.9-TH1

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE
MECHANICAL, GROUND VIAS

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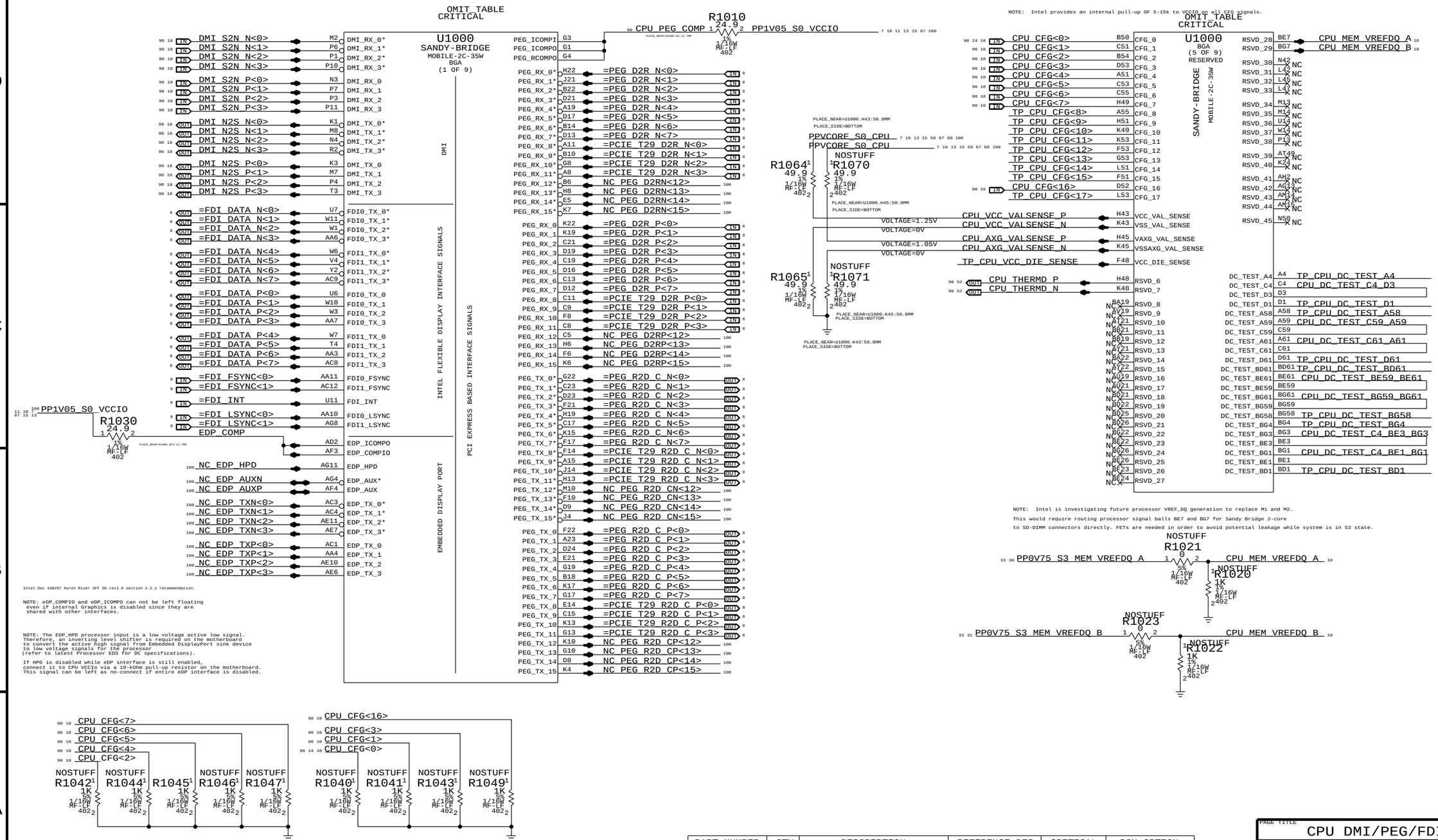

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4034	1	SNB,SR071,PRQ,J1,2.3,35W,2+2,1.30,3M,BGA	U1000	CRITICAL	CPU:PRQ_2G3DC
337S4035	1	SNB,SR04A,PRQ,J1,2.5,35W,2+2,1.30,3M,BGA	U1000	CRITICAL	CPU:PRQ_2G5DC
337S4036	1	SNB,SR041,PRQ,J1,2.7,35W,2+2,1.30,4M,BGA	U1000	CRITICAL	CPU:PRQ_2G7DC

PAGE TITLE
CPU DMI/PEG/FDI/RSVD

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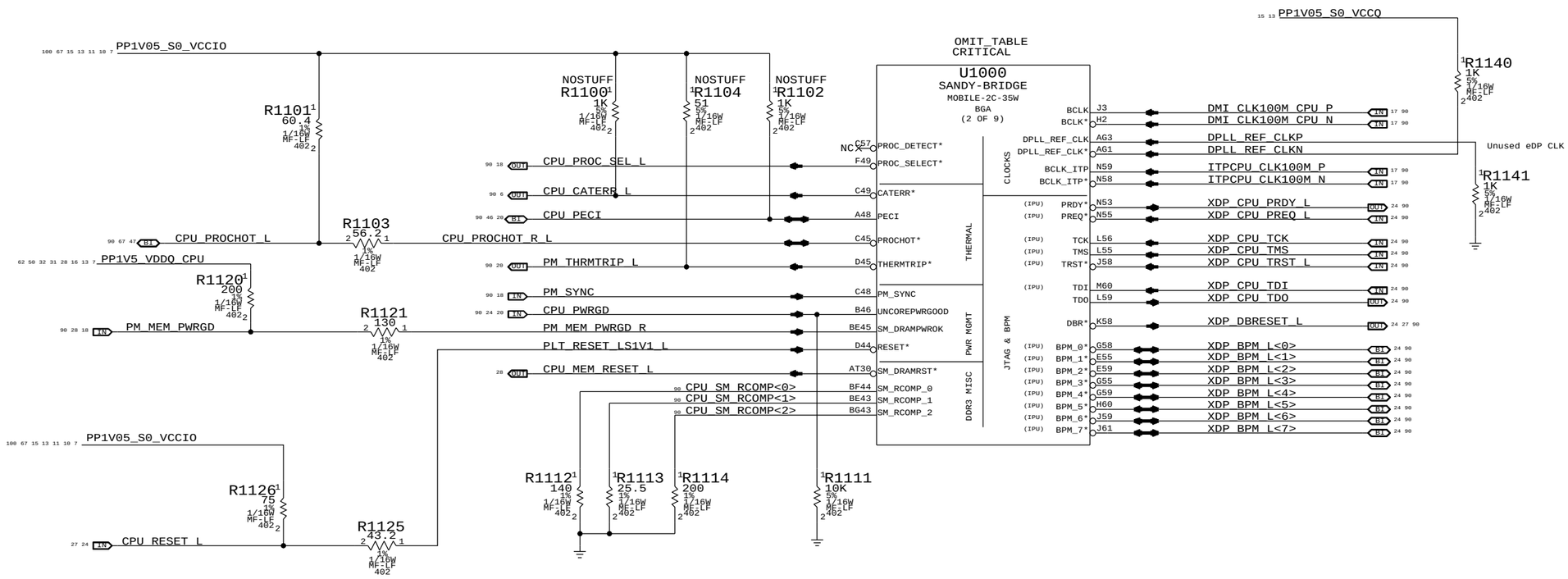

PAGE TITLE	CPU CLOCK/MISC/JTAG
Apple Inc.	DRAWING NUMBER 051-8937 SIZE D
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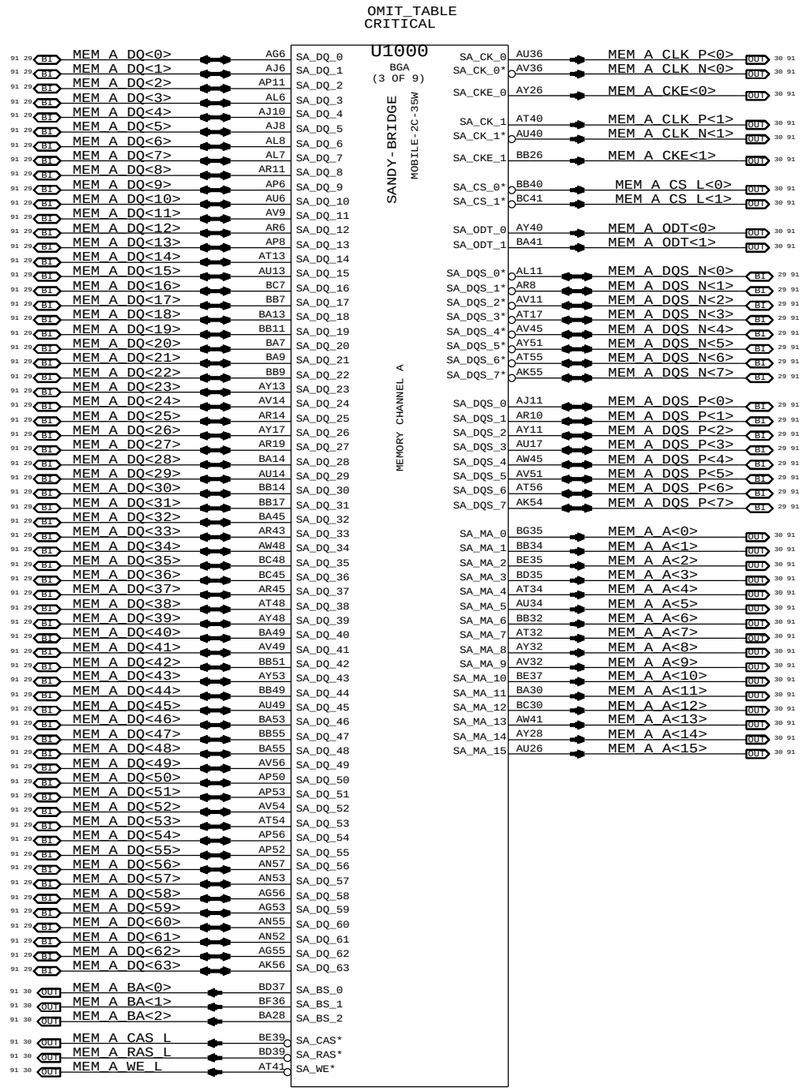

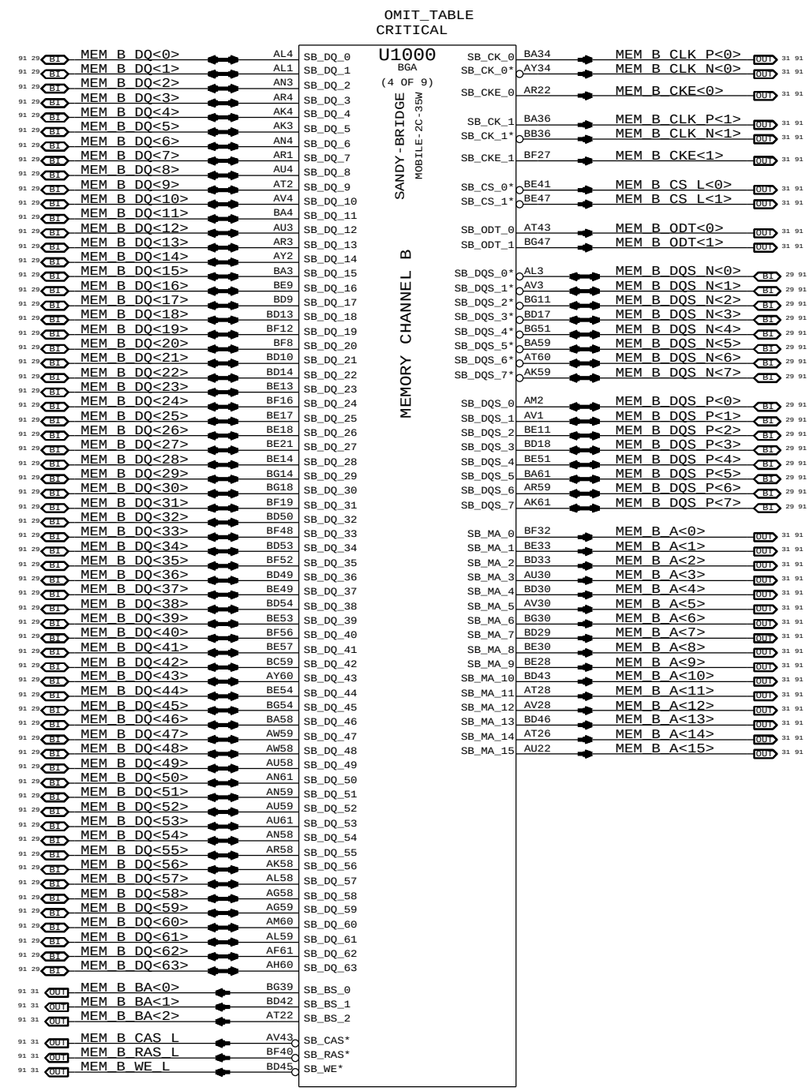

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PAGE TITLE
CPU DDR3 INTERFACES

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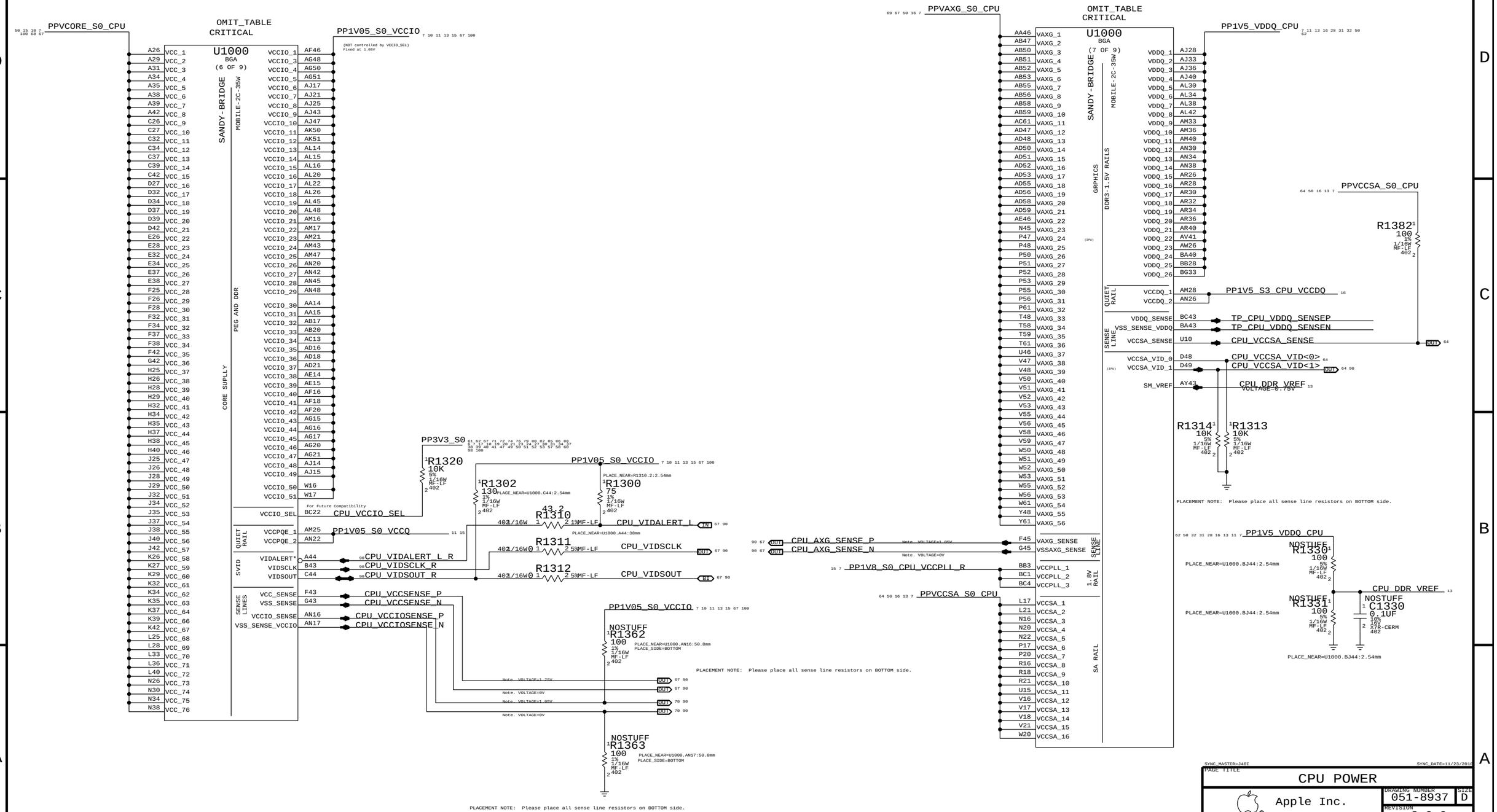

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PAGE TITLE	CPU POWER
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OMIT_TABLE
CRITICAL

U1000
BGA
(9 OF 9)
SANDY-BRIDGE
MOBILE-2C-35W

BG13	VSS	VSS	M11
BG17	VSS	VSS	M15
BG21	VSS	VSS	M58
BG24	VSS	VSS	N1
BG28	VSS	VSS	N17
BG37	VSS	VSS	N21
BG41	VSS	VSS	N25
BG45	VSS	VSS	N28
BG49	VSS	VSS	N33
BG53	VSS	VSS	N36
C29	VSS	VSS	N40
C35	VSS	VSS	N43
C40	VSS	VSS	N47
D4	VSS	VSS	N48
D6	VSS	VSS	N51
D10	VSS	VSS	N52
D14	VSS	VSS	N56
D18	VSS	VSS	N61
D22	VSS	VSS	P9
D26	VSS	VSS	P14
D29	VSS	VSS	P16
D35	VSS	VSS	P18
D40	VSS	VSS	P21
D43	VSS	VSS	P58
D46	VSS	VSS	P59
D50	VSS	VSS	R4
D54	VSS	VSS	R17
D58	VSS	VSS	R20
E3	VSS	VSS	R46
E25	VSS	VSS	T1
E29	VSS	VSS	T47
E35	VSS	VSS	T50
E40	VSS	VSS	T51
F13	VSS	VSS	T52
F15	VSS	VSS	T53
F19	VSS	VSS	T55
F29	VSS	VSS	T56
F35	VSS	VSS	U8
F40	VSS	VSS	U13
F55	VSS	VSS	V20
G6	VSS	VSS	V61
G48	VSS	VSS	W8
G51	VSS	VSS	W13
G61	VSS	VSS	W15
H4	VSS	VSS	W18
H10	VSS	VSS	W21
H14	VSS	VSS	W46
H17	VSS	VSS	Y4
H21	VSS	VSS	Y47
H53	VSS	VSS	Y58
H58	VSS	VSS	Y59
J1	VSS		
J49	VSS		
J55	VSS		
K8	VSS		
K11	VSS		
K21	VSS	VSS_NCTF	A5
K51	VSS	VSS_NCTF	A57
L16	VSS	VSS_NCTF	BC61
L20	VSS	VSS_NCTF	BD3
L22	VSS	VSS_NCTF	BD59
L26	VSS	VSS_NCTF	BE4
L30	VSS	VSS_NCTF	BE58
L34	VSS	VSS_NCTF	BG5
L38	VSS	VSS_NCTF	BG57
L43	VSS	VSS_NCTF	C3
L48	VSS	VSS_NCTF	C58
L61	VSS	VSS_NCTF	D59
M4	VSS	VSS_NCTF	E1
M6	VSS	VSS_NCTF	E61

OMIT_TABLE
CRITICAL

U1000
BGA
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SANDY-BRIDGE
MOBILE-2C-35W

A9	VSS	VSS	AM34
A13	VSS	VSS	AM38
A17	VSS	VSS	AM42
A21	VSS	VSS	AM45
A25	VSS	VSS	AM48
A28	VSS	VSS	AM58
A33	VSS	VSS	AN1
A37	VSS	VSS	AN21
A40	VSS	VSS	AN25
A45	VSS	VSS	AN28
A49	VSS	VSS	AN33
A53	VSS	VSS	AN36
AA1	VSS	VSS	AN40
AA8	VSS	VSS	AN43
AA13	VSS	VSS	AN47
AA50	VSS	VSS	AN50
AA51	VSS	VSS	AN54
AA52	VSS	VSS	AP7
AA53	VSS	VSS	AP10
AA55	VSS	VSS	AP51
AA56	VSS	VSS	AP55
AB16	VSS	VSS	AR7
AB18	VSS	VSS	AR13
AB21	VSS	VSS	AR17
AB48	VSS	VSS	AR21
AB61	VSS	VSS	AR41
AC6	VSS	VSS	AR48
AC10	VSS	VSS	AR61
AC14	VSS	VSS	AT4
AC46	VSS	VSS	AT14
AD4	VSS	VSS	AT19
AD17	VSS	VSS	AT36
AD20	VSS	VSS	AT45
AD61	VSS	VSS	AT52
AE8	VSS	VSS	AT58
AE13	VSS	VSS	AU1
AF1	VSS	VSS	AU7
AF17	VSS	VSS	AU11
AF21	VSS	VSS	AU28
AF47	VSS	VSS	AU32
AF48	VSS	VSS	AU51
AF50	VSS	VSS	AV17
AF51	VSS	VSS	AV21
AF52	VSS	VSS	AV22
AF53	VSS	VSS	AV34
AF55	VSS	VSS	AV40
AF56	VSS	VSS	AV48
AF58	VSS	VSS	AV55
AF59	VSS	VSS	AW7
AG7	VSS	VSS	AW13
AG10	VSS	VSS	AW43
AG14	VSS	VSS	AW61
AG18	VSS	VSS	AY4
AG47	VSS	VSS	AY9
AG52	VSS	VSS	AY14
AG61	VSS	VSS	AY19
AH4	VSS	VSS	AY30
AH58	VSS	VSS	AY36
AJ7	VSS	VSS	AY41
AJ13	VSS	VSS	AY45
AJ16	VSS	VSS	AY49
AJ20	VSS	VSS	AY55
AJ22	VSS	VSS	AY58
AJ26	VSS	VSS	BA1
AJ30	VSS	VSS	BA11
AJ34	VSS	VSS	BA17
AJ38	VSS	VSS	BA21
AJ42	VSS	VSS	BA26
AJ45	VSS	VSS	BA32
AJ48	VSS	VSS	BA48
AK1	VSS	VSS	BA51
AK52	VSS	VSS	BB53
AL10	VSS	VSS	BC5
AL13	VSS	VSS	BC13
AL17	VSS	VSS	BC57
AL21	VSS	VSS	BD8
AL25	VSS	VSS	BD12
AL28	VSS	VSS	BD16
AL33	VSS	VSS	BD19
AL36	VSS	VSS	BD23
AL40	VSS	VSS	BD27
AL43	VSS	VSS	BD32
AL47	VSS	VSS	BD36
AL61	VSS	VSS	BD40
AM4	VSS	VSS	BD44
AM13	VSS	VSS	BD48
AM20	VSS	VSS	BD52
AM22	VSS	VSS	BD56
AM26	VSS	VSS	BE5
AM30	VSS	VSS	BG9

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CPU GROUNDS

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All INTEL recommendations from Intel doc #4439028 Huron River Platform Power Design Guide

CPU VCORE DECOUPLING

Intel recommendation (Section 6.2): 35x 2.2uF, 25x 22uF, 4x 470uF

68 67 50 13 10 7 100 PPVCORE_S0_CPU

C1600 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1601 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1602 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1603 2.2UF 20% 6.3V CERM 402-LF
C1604 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1605 2.2UF 20% 6.3V CERM 402-LF
C1606 2.2UF 20% 6.3V CERM 402-LF
C1607 2.2UF 20% 6.3V CERM 402-LF
C1608 2.2UF 20% 6.3V CERM 402-LF
C1609 2.2UF 20% 6.3V CERM 402-LF
C1610 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1611 2.2UF 20% 6.3V CERM 402-LF
C1612 2.2UF 20% 6.3V CERM 402-LF
C1613 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1614 2.2UF 20% 6.3V CERM 402-LF
C1615 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1616 2.2UF 20% 6.3V CERM 402-LF
C1617 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1618 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1619 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1620 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1621 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1622 2.2UF 20% 6.3V CERM 402-LF
C1623 2.2UF 20% 6.3V CERM 402-LF
C1624 2.2UF 20% 6.3V CERM 402-LF

C1625 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1626 2.2UF 20% 6.3V CERM 402-LF
C1627 2.2UF 20% 6.3V CERM 402-LF
C1628 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1629 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1630 2.2UF 20% 6.3V CERM 402-LF
C1631 2.2UF 20% 6.3V CERM 402-LF
C1632 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1633 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1634 2.2UF 20% 6.3V CERM 402-LF
C1635 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1636 2.2UF 20% 6.3V CERM 402-LF
C1637 2.2UF 20% 6.3V CERM 402-LF
C1638 2.2UF 20% 6.3V CERM 402-LF
C1639 2.2UF 20% 6.3V CERM 402-LF
C1640 2.2UF 20% 6.3V CERM 402-LF
C1641 2.2UF 20% 6.3V CERM 402-LF
C1642 2.2UF 20% 6.3V CERM 402-LF
C1643 2.2UF 20% 6.3V CERM 402-LF
C1644 2.2UF 20% 6.3V CERM 402-LF
C1645 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1646 2.2UF 20% 6.3V CERM 402-LF
C1647 2.2UF 20% 6.3V CERM 402-LF
C1648 2.2UF 20% 6.3V CERM 402-LF
NOSTUFF C1649 2.2UF 20% 6.3V CERM 402-LF

C1650 2.2UF 20% 6.3V CERM 402-LF
C1651 2.2UF 20% 6.3V CERM 402-LF
C1652 2.2UF 20% 6.3V CERM 402-LF
C1653 2.2UF 20% 6.3V CERM 402-LF
C1654 2.2UF 20% 6.3V CERM 402-LF

PLACEMENT_NOTE (C1655-C1666):
Place close to U1000 on top side.

C1655 22UF 20% 6.3V X5R-CERM1 0603
C1656 22UF 20% 6.3V X5R-CERM1 0603
C1657 22UF 20% 6.3V X5R-CERM1 0603
C1658 22UF 20% 6.3V X5R-CERM1 0603
C1659 22UF 20% 6.3V X5R-CERM1 0603
C1660 22UF 20% 6.3V X5R-CERM1 0603
C1661 22UF 20% 6.3V X5R-CERM1 0603
C1662 22UF 20% 6.3V X5R-CERM1 0603
C1663 22UF 20% 6.3V X5R-CERM1 0603
C1664 22UF 20% 6.3V X5R-CERM1 0603
C1665 22UF 20% 6.3V X5R-CERM1 0603
C1666 22UF 20% 6.3V X5R-CERM1 0603

PLACEMENT_NOTE (C1667-C1679):
Place close to U1000 on bottom side.

C1667 22UF 20% 6.3V X5R-CERM1 0603
C1668 22UF 20% 6.3V X5R-CERM1 0603
C1669 22UF 20% 6.3V X5R-CERM1 0603
C1670 22UF 20% 6.3V X5R-CERM1 0603
C1671 22UF 20% 6.3V X5R-CERM1 0603
C1672 22UF 20% 6.3V X5R-CERM1 0603
C1673 22UF 20% 6.3V X5R-CERM1 0603
C1674 22UF 20% 6.3V X5R-CERM1 0603
C1675 22UF 20% 6.3V X5R-CERM1 0603
C1676 22UF 20% 6.3V X5R-CERM1 0603
C1677 22UF 20% 6.3V X5R-CERM1 0603
C1678 22UF 20% 6.3V X5R-CERM1 0603
C1679 22UF 20% 6.3V X5R-CERM1 0603

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Section 6.5): 26x 1uF, 10x 10uF, 2x 330uF

PLACEMENT_NOTE (C1684-C167F):
Place on bottom side of U1000

13 11 10 7 100 67 PP1V05_S0_VCCIO

C1684 1UF 10% 10V X5R 402-1
C1685 1UF 10% 10V X5R 402-1
C1686 1UF 10% 10V X5R 402-1
C1687 1UF 10% 10V X5R 402-1
C1688 1UF 10% 10V X5R 402-1
C1689 1UF 10% 10V X5R 402-1
C1690 1UF 10% 10V X5R 402-1
C1691 1UF 10% 10V X5R 402-1
C1692 1UF 10% 10V X5R 402-1
C1693 1UF 10% 10V X5R 402-1
C1694 1UF 10% 10V X5R 402-1
C1695 1UF 10% 10V X5R 402-1
C1696 1UF 10% 10V X5R 402-1

C1697 1UF 10% 10V X5R 402-1
C1698 1UF 10% 10V X5R 402-1
C1699 1UF 10% 10V X5R 402-1
C169A 1UF 10% 10V X5R 402-1
C169B 1UF 10% 10V X5R 402-1
C169C 1UF 10% 10V X5R 402-1
C169D 1UF 10% 10V X5R 402-1
C169E 1UF 10% 10V X5R 402-1
C169F 1UF 10% 10V X5R 402-1
C161A 1UF 10% 10V X5R 402-1
C161B 1UF 10% 10V X5R 402-1
C161C 1UF 10% 10V X5R 402-1
C161D 1UF 10% 10V X5R 402-1

PLACEMENT_NOTE (C1672-C1681):
Place near U1000 on bottom side

C161E 10UF 20% 6.3V X5R 603
C161F 10UF 20% 6.3V CERM-X5R 0402-1
C162A 10UF 20% 6.3V CERM-X5R 0402-1
C162B 10UF 20% 6.3V CERM-X5R 0402-1
C162C 10UF 20% 6.3V CERM-X5R 0402-1
C162D 10UF 20% 6.3V CERM-X5R 0402-1
C162E 10UF 20% 6.3V CERM-X5R 0402-1
C167A 10UF 20% 6.3V CERM-X5R 0402-1
C167B 10UF 20% 6.3V CERM-X5R 0402-1
C167C 10UF 20% 6.3V CERM-X5R 0402-1

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

CRITICAL
R1601 0.010 1% 1/4W MF 0603

C167F 1UF 10% 10V X5R 402-1

PP1V05_S0_VCCQ 11 13
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
MAX_NECK_LENGTH=3 MM

CPU VCCPLL DECOUPLING

Intel recommendation (section 6.4): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):
Place near U1000 on top side

71 26 23 21 18 7 PP1V8_S0

R1600 0 5% 1/16W MF-LF 402

PLACE_NEAR=U1000.A652:2.54 MM:NO_VIA

C160X 1UF 10% 10V X5R 402-1
C160Y 1UF 10% 10V X5R 402-1
C160Z 270UF 20% 2V TANT CASE-B4-SM

PLACE_NEAR=U1000.A652:2.54 MM:NO_VIA
PLACE_NEAR=U1000.A651:5mm

PP1V8_S0_CPU_VCCPLL_R 7 13

CPU VCCPLL Low pass filter

SYNC_MASTER=J40I SYNC_DATE=11/23/2010

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VAXG DECOUPLING

Intel recommendation (section 6.3): 21x 1uF, 6x 10uF, 6x 22uF, 2x 470uF

69 67 50 13 7 PPVAXG_S0_CPU

PLACEMENT_NOTE (C1700-C1710):

Place on bottom side of U1000

C1700 1UF 10% 10V X5R 402-1
C1701 1UF 10% 10V X5R 402-1
C1702 1UF 10% 10V X5R 402-1
C1703 1UF 10% 10V X5R 402-1
C1704 1UF 10% 10V X5R 402-1
C1705 1UF 10% 10V X5R 402-1
C1706 1UF 10% 10V X5R 402-1
C1707 1UF 10% 10V X5R 402-1
C1708 1UF 10% 10V X5R 402-1
C1709 1UF 10% 10V X5R 402-1
C1710 1UF 10% 10V X5R 402-1

PLACEMENT_NOTE (C1711-C1716):

CRITICAL
C1711 10UF 20% 6.3V CERM-X5R 0402-1
C1712 10UF 20% 6.3V CERM-X5R 0402-1
C1713 10UF 20% 6.3V CERM-X5R 0402-1
C1714 10UF 20% 6.3V CERM-X5R 0402-1
C1715 10UF 20% 6.3V CERM-X5R 0402-1
C1716 10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1717-C1722):

CRITICAL
C1717 22UF 20% 6.3V X5R-CERM1 0603
C1718 22UF 20% 6.3V X5R-CERM1 0603
C1719 22UF 20% 6.3V X5R-CERM1 0603
C1720 22UF 20% 6.3V X5R-CERM1 0603
C1721 22UF 20% 6.3V X5R-CERM1 0603
C1722 22UF 20% 6.3V X5R-CERM1 0603

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation (Section 6.5): 10x 1uF, 8x 10uF, 1x 330uF

62 50 32 31 28 13 11 7 PP1V5_VDDQ_CPU

PLACEMENT_NOTE (C1738-C1747):

Place on bottom side of U1000

C1738 1UF 10% 10V X5R 402-1
C1739 1UF 10% 10V X5R 402-1
C1740 1UF 10% 10V X5R 402-1
C1741 1UF 10% 10V X5R 402-1
C1742 1UF 10% 10V X5R 402-1
C1743 1UF 10% 10V X5R 402-1
C1744 1UF 10% 10V X5R 402-1
C1745 1UF 10% 10V X5R 402-1
C1746 1UF 10% 10V X5R 402-1
C1747 1UF 10% 10V X5R 402-1

Place close to U1000 on bottom side

C1748 10UF 20% 6.3V CERM-X5R 0402-1
C1749 10UF 20% 6.3V CERM-X5R 0402-1
C1750 10UF 20% 6.3V X5R 603
C1751 10UF 20% 6.3V CERM-X5R 0402-1
C1752 10UF 20% 6.3V CERM-X5R 0402-1
C1753 10UF 20% 6.3V CERM-X5R 0402-1
C1754 10UF 20% 6.3V X5R 603
C1755 10UF 20% 6.3V CERM-X5R 0402-1

CRITICAL
C1756 270UF 20% 2V TANT CASE-B4-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

CRITICAL
R1702 0.010 1% 1/2W MF 0603

PP1V5_S3_CPU_VCCDQ 13
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 mm

C1757 1UF 10% 10V X5R 402-1

CPU VCCSA DECOUPLING

Intel recommendation (Section 6.6): 6x 1uf, 5x 10uf, 1x 330uf

PLACEMENT_NOTE (C1758-C1762):

64 50 13 7 PPVCCSA_S0_CPU

Place on bottom side of U1000

C1758 1UF 10% 10V X5R 402-1
C1759 1UF 10% 10V X5R 402-1
C1760 1UF 10% 10V X5R 402-1
C1761 1UF 10% 10V X5R 402-1
C1762 1UF 10% 10V X5R 402-1

C1763 10UF 20% 6.3V CERM-X5R 0402-1
C1764 10UF 20% 6.3V CERM-X5R 0402-1
C1765 10UF 20% 6.3V CERM-X5R 0402-1
C1766 10UF 20% 6.3V CERM-X5R 0402-1
C1767 10UF 20% 6.3V CERM-X5R 0402-1

CRITICAL
C1768 270UF 20% 2V TANT CASE-B4-SM

SYNC_MASTER=J40I SYNC_DATE=11/23/2010

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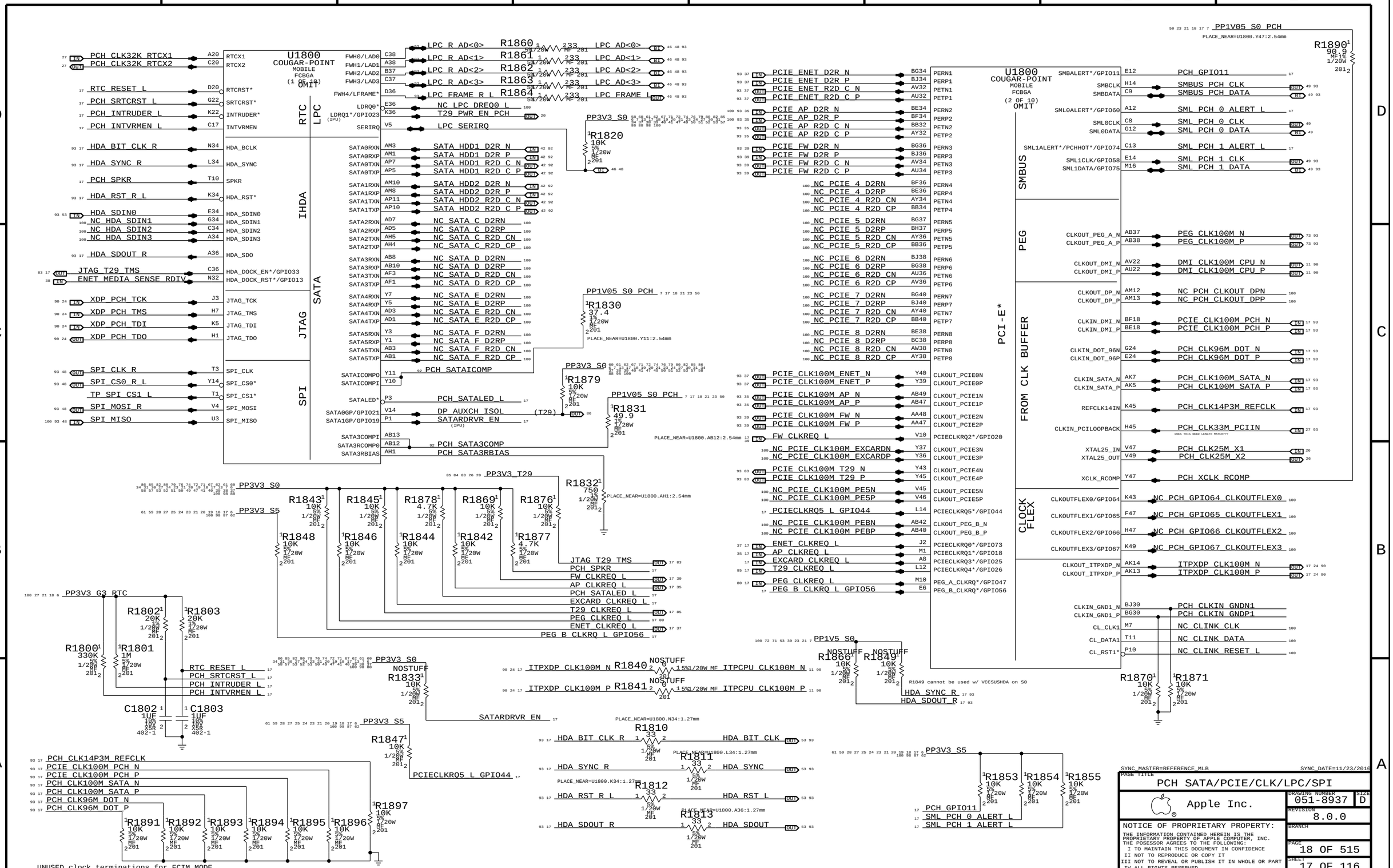
U1800
COUGAR-POINT
MOBILE
FCBGA
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OMIT
RTC
LPC
IHDA
SATA
JTAG
SPI
PCH CLK32K RTCX1
PCH CLK32K RTCX2
RTC RESET L
PCH SRTCRST L
PCH INTRUDER L
PCH INTVRMEN L
HDA BIT CLK R
HDA SYNC R
PCH SPKR
HDA RST R L
HDA SDIN0
NC HDA SDIN1
NC HDA SDIN2
NC HDA SDIN3
HDA SDOUT R
JTAG T29 TMS
ENET MEDIA SENSE RDIV
XDP PCH TCK
XDP PCH TMS
XDP PCH TDI
XDP PCH TDO
SPI CLK R
SPI CS0 R L
TP SPI CS1 L
SPI MOSI R
SPI MISO
LPC R AD<0>
LPC R AD<1>
LPC R AD<2>
LPC R AD<3>
LPC FRAME R L
NC LPC DREQ0 L
T29 PWR EN PCH
LPC SERIRQ
SATA HDD1 D2R N
SATA HDD1 D2R P
SATA HDD1 R2D C N
SATA HDD1 R2D C P
SATA HDD2 D2R N
SATA HDD2 D2R P
SATA HDD2 R2D C N
SATA HDD2 R2D C P
NC SATA C D2RN
NC SATA C D2RP
NC SATA C R2D CN
NC SATA C R2D CP
NC SATA D D2RN
NC SATA D D2RP
NC SATA D R2D CN
NC SATA D R2D CP
NC SATA E D2RN
NC SATA E D2RP
NC SATA E R2D CN
NC SATA E R2D CP
NC SATA F D2RN
NC SATA F D2RP
NC SATA F R2D CN
NC SATA F R2D CP
PCH SATAICOMP
PCH SATALED L
DP AUXCH ISOL (T29)
SATARDRVR EN
PCH SATA3COMP
PCH SATA3RBIAS
R1860 233 LPC AD<0>
R1861 233 LPC AD<1>
R1862 233 LPC AD<2>
R1863 233 LPC AD<3>
R1864 233 LPC FRAME L
PP3V3 S0
R1820 10K
R1830 37.4
PP1V05 S0 PCH
R1879 10K
R1831 49.9
R1832 750
PP3V3 T29
R1843 10K
R1845 10K
R1878 4.7K
R1869 10K
R1876 10K
R1848 10K
R1846 10K
R1844 10K
R1842 10K
R1877 4.7K
JTAG T29 TMS
PCH SPKR
FW CLKREQ L
AP CLKREQ L
PCH SATALED L
EXCARD CLKREQ L
T29 CLKREQ L
PEG CLKREQ L
ENET CLKREQ L
PEG B CLKRQ L GPIO56
PP3V3 G3 RTC
R1802 20K
R1803 20K
R1800 330K
R1801 1M
RTC RESET L
PCH SRTCRST L
PCH INTRUDER L
PCH INTVRMEN L
C1802 1UF
C1803 1UF
PP3V3 S5
R1833 10K
NOSTUFF
R1847 10K
PCIECLKRQ5 L GPIO44
ITPXDP CLK100M N
ITPXDP CLK100M P
R1840 0
R1841 0
ITPCPU CLK100M N
ITPCPU CLK100M P
PP1V5 S0
R1866 10K
R1849 10K
R1849 cannot be used w/ VCCSUSHDA on S0
HDA SYNC R
HDA SDOUT R
R1810 33
R1811 33
R1812 33
R1813 33
HDA BIT CLK R
HDA SYNC
HDA RST L
HDA SDOUT
PCH CLK14P3M REFCLK
PCIE CLK100M PCH N
PCIE CLK100M PCH P
PCH CLK100M SATA N
PCH CLK100M SATA P
PCH CLK96M DOT N
PCH CLK96M DOT P
R1891 10K
R1892 10K
R1893 10K
R1894 10K
R1895 10K
R1896 10K
R1897 10K
UNUSED clock terminations for FCIM MODE
PCIE ENET D2R N
PCIE ENET D2R P
PCIE ENET R2D C N
PCIE ENET R2D C P
PCIE AP D2R N
PCIE AP D2R P
PCIE AP R2D C N
PCIE AP R2D C P
PCIE FW D2R N
PCIE FW D2R P
PCIE FW R2D C N
PCIE FW R2D C P
NC PCIE 4 D2RN
NC PCIE 4 D2RP
NC PCIE 4 R2D CN
NC PCIE 4 R2D CP
NC PCIE 5 D2RN
NC PCIE 5 D2RP
NC PCIE 5 R2D CN
NC PCIE 5 R2D CP
NC PCIE 6 D2RN
NC PCIE 6 D2RP
NC PCIE 6 R2D CN
NC PCIE 6 R2D CP
NC PCIE 7 D2RN
NC PCIE 7 D2RP
NC PCIE 7 R2D CN
NC PCIE 7 R2D CP
NC PCIE 8 D2RN
NC PCIE 8 D2RP
NC PCIE 8 R2D CN
NC PCIE 8 R2D CP
PCIE CLK100M ENET N
PCIE CLK100M ENET P
PCIE CLK100M AP N
PCIE CLK100M AP P
PCIE CLK100M FW N
PCIE CLK100M FW P
FW CLKREQ L
NC PCIE CLK100M EXCARDN
NC PCIE CLK100M EXCARDP
PCIE CLK100M T29 N
PCIE CLK100M T29 P
NC PCIE CLK100M PE5N
NC PCIE CLK100M PE5P
PCIECLKRQ5 L GPIO44
NC PCIE CLK100M PEBN
NC PCIE CLK100M PEBP
ENET CLKREQ L
AP CLKREQ L
EXCARD CLKREQ L
T29 CLKREQ L
PEG CLKREQ L
PEG B CLKRQ L GPIO56
PCI-E*
SMBUS
PEG
FROM CLK BUFFER
CLOCK FLEX
PP1V05 S0 PCH
R1890 90.9
PCH GPIO11
SMBUS PCH CLK
SMBUS PCH DATA
SML PCH 0 ALERT L
SML PCH 0 CLK
SML PCH 0 DATA
SML PCH 1 ALERT L
SML PCH 1 CLK
SML PCH 1 DATA
PEG CLK100M N
PEG CLK100M P
DMI CLK100M CPU N
DMI CLK100M CPU P
NC PCH CLKOUT DPN
NC PCH CLKOUT DPP
PCIE CLK100M PCH N
PCIE CLK100M PCH P
PCH CLK96M DOT N
PCH CLK96M DOT P
PCH CLK100M SATA N
PCH CLK100M SATA P
PCH CLK14P3M REFCLK
PCH CLK33M PCIIN
PCH CLK25M X1
PCH CLK25M X2
PCH XCLK RCOMP
NC PCH GPIO64 CLKOUTFLEX0
NC PCH GPIO65 CLKOUTFLEX1
NC PCH GPIO66 CLKOUTFLEX2
NC PCH GPIO67 CLKOUTFLEX3
ITPXDP CLK100M N
ITPXDP CLK100M P
PCH CLKIN GNDN1
PCH CLKIN GNDP1
NC CLK CLK
NC CLINK DATA
NC CLINK RESET L
R1870 10K
R1871 10K
PP3V3 S5
R1853 10K
R1854 10K
R1855 10K
PCH GPIO11
SML PCH 0 ALERT L
SML PCH 1 ALERT L
SYNC MASTER=REFERENCE_MLB
SYNC DATE=11/23/2016
PCH SATA/PCIE/CLK/LPC/SPI
Apple Inc.
DRAWING NUMBER 051-8937
SIZE D
REVISION 8.0.0
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PAGE 18 OF 515
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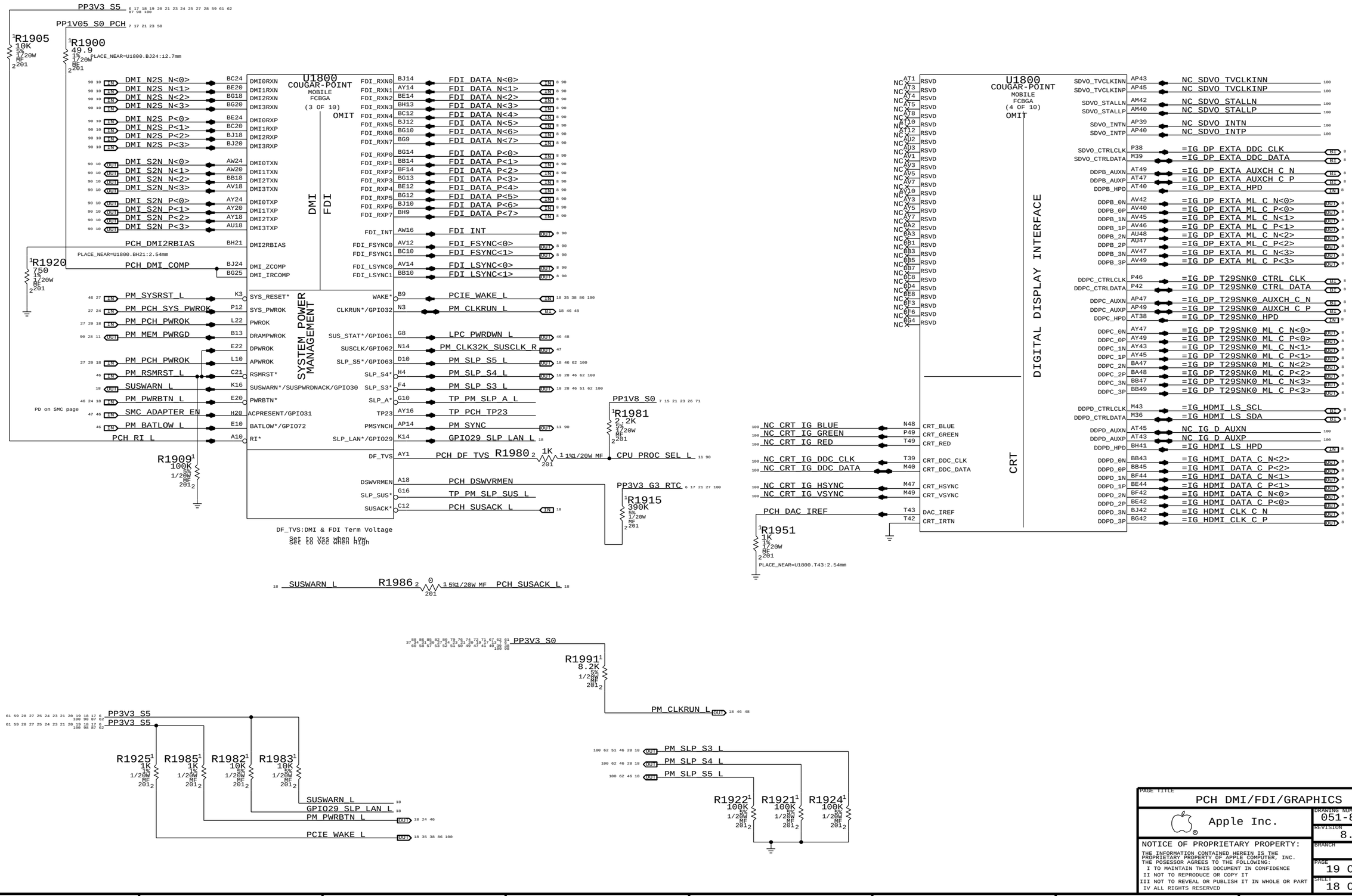

PAGE TITLE
PCH DMI/FDI/GRAPHICS

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DRAWING NUMBER 051-8937 SIZE D
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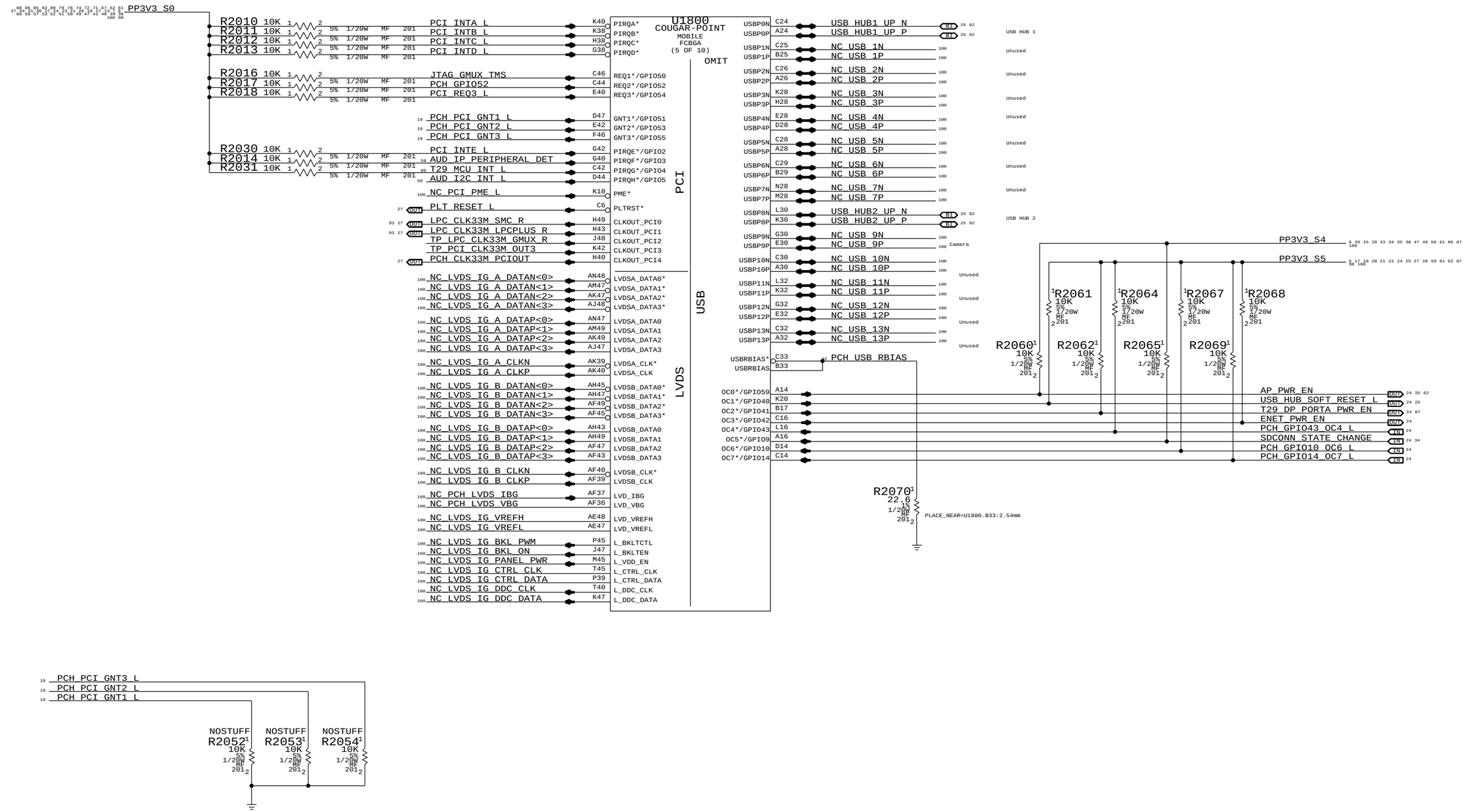

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE
PCH PCI/FLASHCACHE/USB

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DRAWING NUMBER 051-8937 SIZE D
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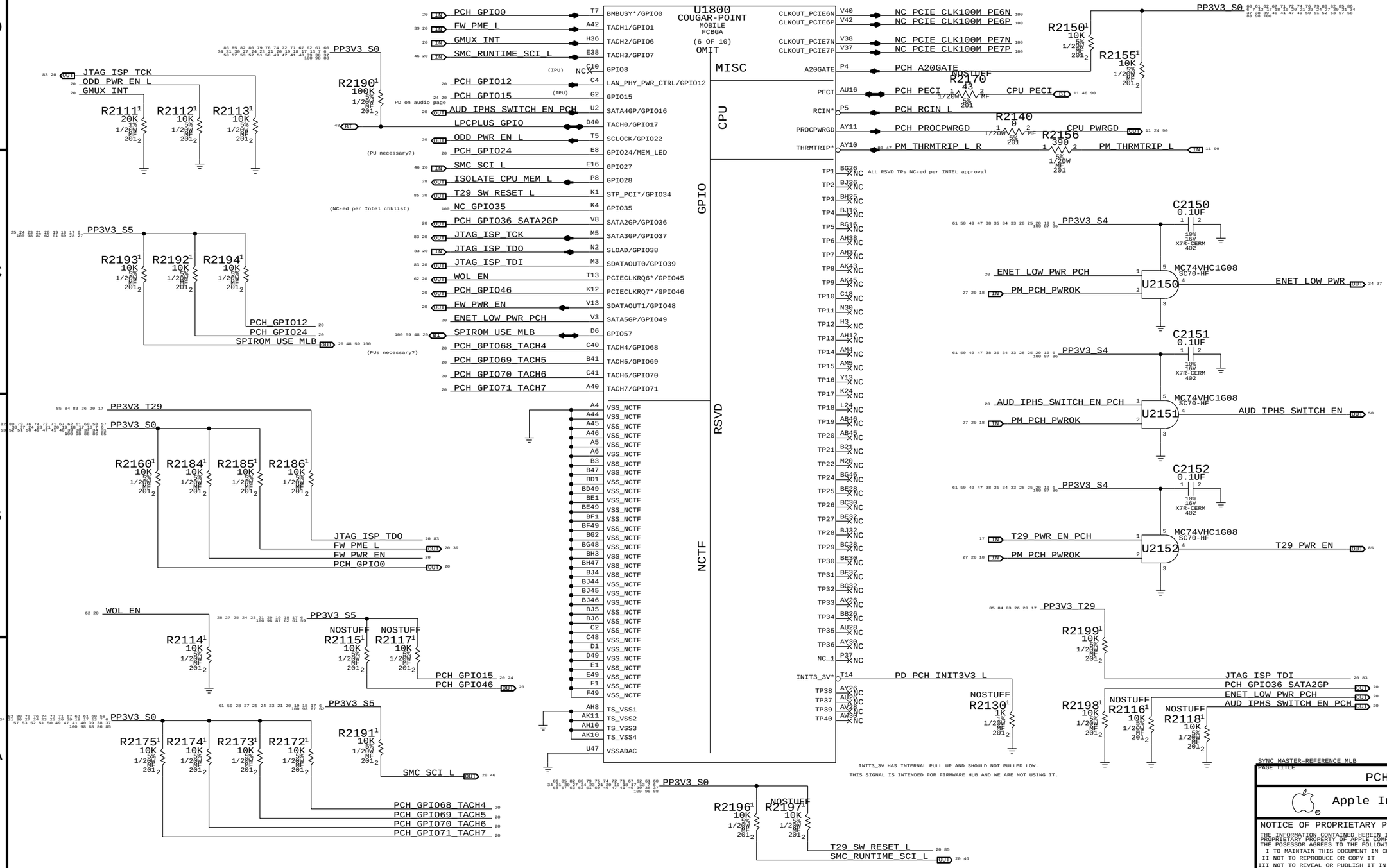

SYNC MASTER=REFERENCE_MLB SYNC DATE=12/07/2016

PAGE TITLE: PCH MISC

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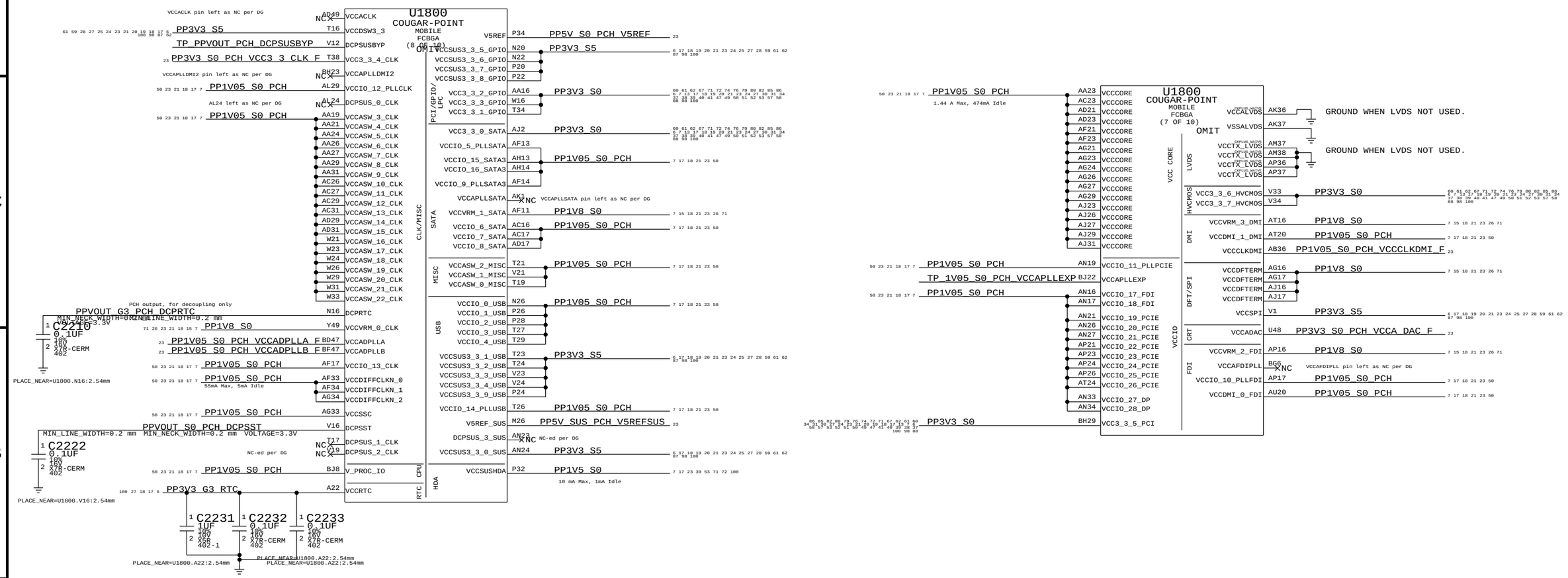

PAGE TITLE

PCH POWER

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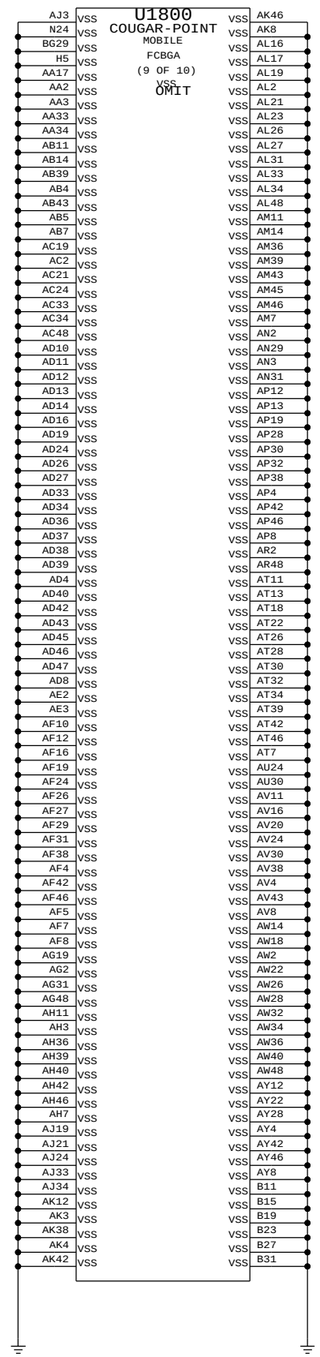

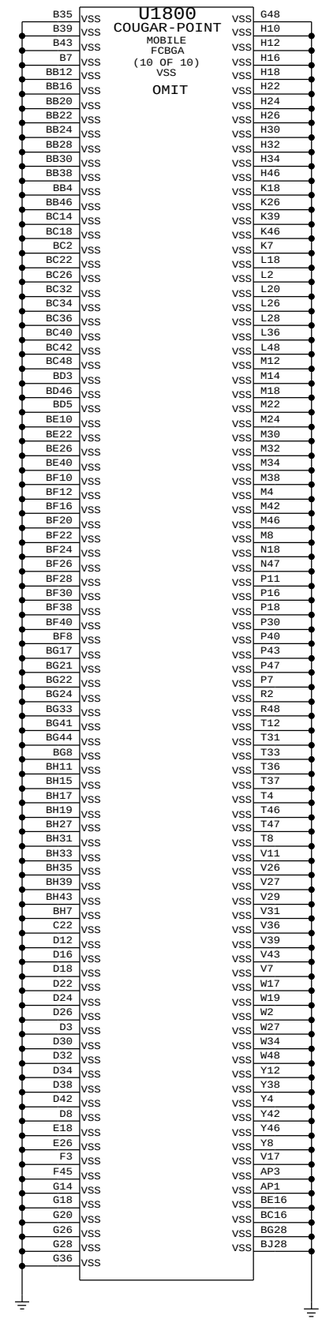

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

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PCH GROUNDS

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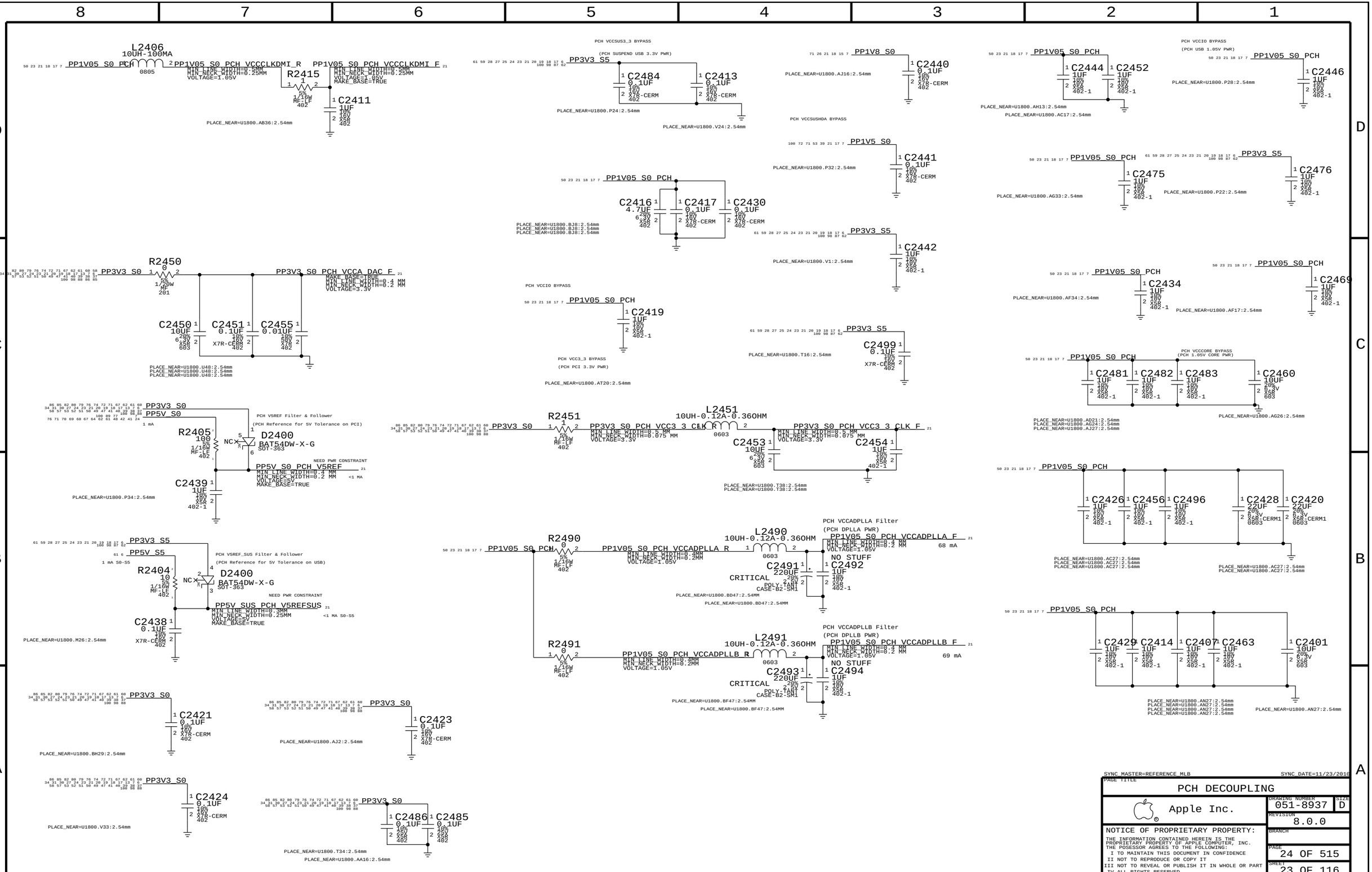
L2406
10UH-100MA
0805
PP1V05_S0_PCH
PP1V05_S0_PCH_VCCCLKDMI_R
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.05V
PP1V05_S0_PCH_VCCCLKDMI_F
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
R2415
C2411
1UF
PLACE_NEAR=U1800.AB36:2.54mm
PCH VCCSUS3_3 BYPASS
(PCH SUSPEND USB 3.3V PWR)
PP3V3_S5
C2484
C2413
PLACE_NEAR=U1800.P24:2.54mm
PLACE_NEAR=U1800.V24:2.54mm
PP1V8_S0
C2440
PLACE_NEAR=U1800.AJ16:2.54mm
PCH VCCSUSHDA BYPASS
PP1V5_S0
C2441
PLACE_NEAR=U1800.P32:2.54mm
PP1V05_S0_PCH
C2444
C2452
PLACE_NEAR=U1800.AH13:2.54mm
PLACE_NEAR=U1800.AC17:2.54mm
PCH VCCIO BYPASS
(PCH USB 1.05V PWR)
C2446
PLACE_NEAR=U1800.P28:2.54mm
C2416
4.7UF
C2417
C2430
PLACE_NEAR=U1800.BJ8:2.54mm
PLACE_NEAR=U1800.BJ8:2.54mm
PLACE_NEAR=U1800.BJ8:2.54mm
C2475
PLACE_NEAR=U1800.AG33:2.54mm
C2476
PLACE_NEAR=U1800.P22:2.54mm
PP3V3_S5
C2442
PLACE_NEAR=U1800.V1:2.54mm
R2450
PP3V3_S0
PP3V3_S0_PCH_VCCA_DAC_F
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
C2450
10UF
C2451
0.1UF
C2455
0.01UF
PLACE_NEAR=U1800.U48:2.54mm
PLACE_NEAR=U1800.U48:2.54mm
PLACE_NEAR=U1800.U48:2.54mm
PCH VCCIO BYPASS
PP1V05_S0_PCH
C2419
1UF
PCH VCC3_3 BYPASS
(PCH PCI 3.3V PWR)
PLACE_NEAR=U1800.AT20:2.54mm
C2434
PLACE_NEAR=U1800.AF34:2.54mm
C2469
PLACE_NEAR=U1800.AF17:2.54mm
C2499
0.1UF
PLACE_NEAR=U1800.T16:2.54mm
PCH VCCCORE BYPASS
(PCH 1.05V CORE PWR)
C2481
C2482
C2483
C2460
10UF
PLACE_NEAR=U1800.AD21:2.54mm
PLACE_NEAR=U1800.AG24:2.54mm
PLACE_NEAR=U1800.AJ27:2.54mm
PLACE_NEAR=U1800.AG26:2.54mm
PP3V3_S0
PP5V_S0
PCH V5REF Filter & Follower
(PCH Reference for 5V Tolerance on PCI)
R2405
100
D2400
BAT54DW-X-G
SOT-363
NEED PWR CONSTRAINT
PP5V_S0_PCH_V5REF
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE
<1 MA
C2439
1UF
PLACE_NEAR=U1800.P34:2.54mm
R2451
PP3V3_S0_PCH_VCC3_3_CLK_R
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=3.3V
L2451
10UH-0.12A-0.36OHM
0603
PP3V3_S0_PCH_VCC3_3_CLK_F
C2453
10UF
C2454
1UF
PLACE_NEAR=U1800.T38:2.54mm
PLACE_NEAR=U1800.T38:2.54mm
PP1V05_S0_PCH
C2426
C2456
C2496
C2428
22UF
C2420
22UF
PLACE_NEAR=U1800.AC27:2.54mm
PLACE_NEAR=U1800.AC27:2.54mm
PLACE_NEAR=U1800.AC27:2.54mm
PLACE_NEAR=U1800.AC27:2.54mm
PLACE_NEAR=U1800.AC27:2.54mm
PP3V3_S5
PP5V_S5
PCH V5REF_SUS Filter & Follower
(PCH Reference for 5V Tolerance on USB)
R2404
D2400
BAT54DW-X-G
SOT-363
NEED PWR CONSTRAINT
PP5V_SUS_PCH_V5REFSUS
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=5V
MAKE_BASE=TRUE
<1 MA S0-S5
C2438
0.1UF
PLACE_NEAR=U1800.M26:2.54mm
R2490
PP1V05_S0_PCH
PP1V05_S0_PCH_VCCADPLLA_R
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.05V
L2490
10UH-0.12A-0.36OHM
0603
PCH VCCADPLLA Filter
(PCH DPLLA PWR)
PP1V05_S0_PCH_VCCADPLLA_F
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
68 mA
C2491
220UF
CRITICAL
POLY-TANT
CASE-B2-SM1
NO STUFF
C2492
1UF
PLACE_NEAR=U1800.BD47:2.54MM
PLACE_NEAR=U1800.BD47:2.54MM
R2491
PP1V05_S0_PCH_VCCADPLLB_R
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.05V
L2491
10UH-0.12A-0.36OHM
0603
PCH VCCADPLLB Filter
(PCH DPLLB PWR)
PP1V05_S0_PCH_VCCADPLLB_F
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
69 mA
C2493
220UF
C2494
1UF
PLACE_NEAR=U1800.BF47:2.54MM
PLACE_NEAR=U1800.BF47:2.54MM
PP1V05_S0_PCH
C2429
C2414
C2407
C2463
C2401
10UF
PLACE_NEAR=U1800.AN27:2.54mm
PLACE_NEAR=U1800.AN27:2.54mm
PLACE_NEAR=U1800.AN27:2.54mm
PLACE_NEAR=U1800.AN27:2.54mm
PLACE_NEAR=U1800.AN27:2.54mm
PP3V3_S0
C2421
0.1UF
PLACE_NEAR=U1800.BH29:2.54mm
C2423
PLACE_NEAR=U1800.AJ2:2.54mm
C2424
PLACE_NEAR=U1800.V33:2.54mm
C2486
C2485
PLACE_NEAR=U1800.T34:2.54mm
PLACE_NEAR=U1800.AA16:2.54mm
SYNC_MASTER=REFERENCE_MLB
SYNC_DATE=11/23/2016
PAGE TITLE
PCH DECOUPLING
Apple Inc.
DRAWING NUMBER
051-8937
SIZE
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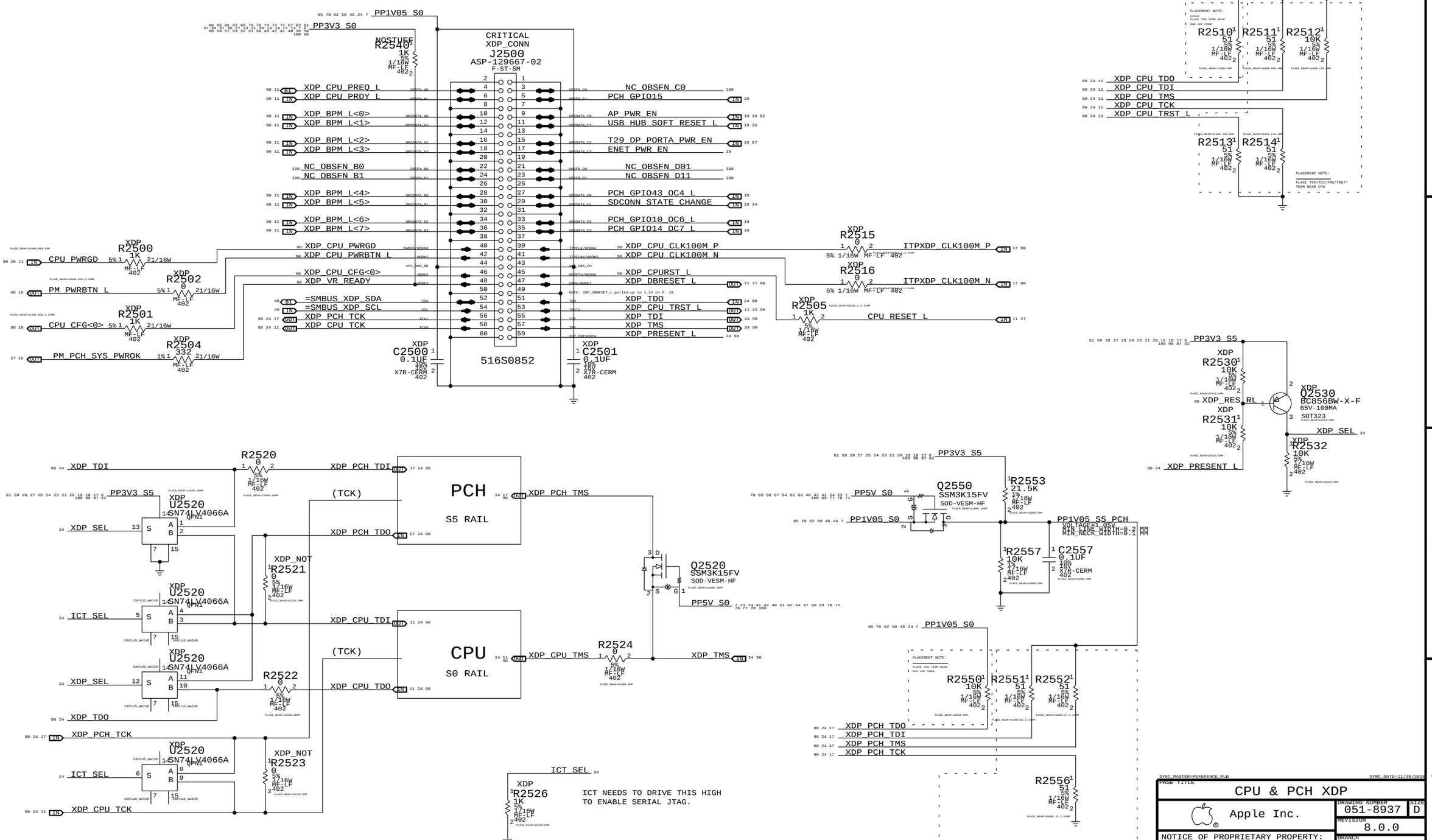
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

USE WITH 920-0620 ADAPTER BOARD TO SUPPORT CPU, PCH DEBUGGING.



SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/30/2010

PAGE TITLE: CPU & PCH XDP

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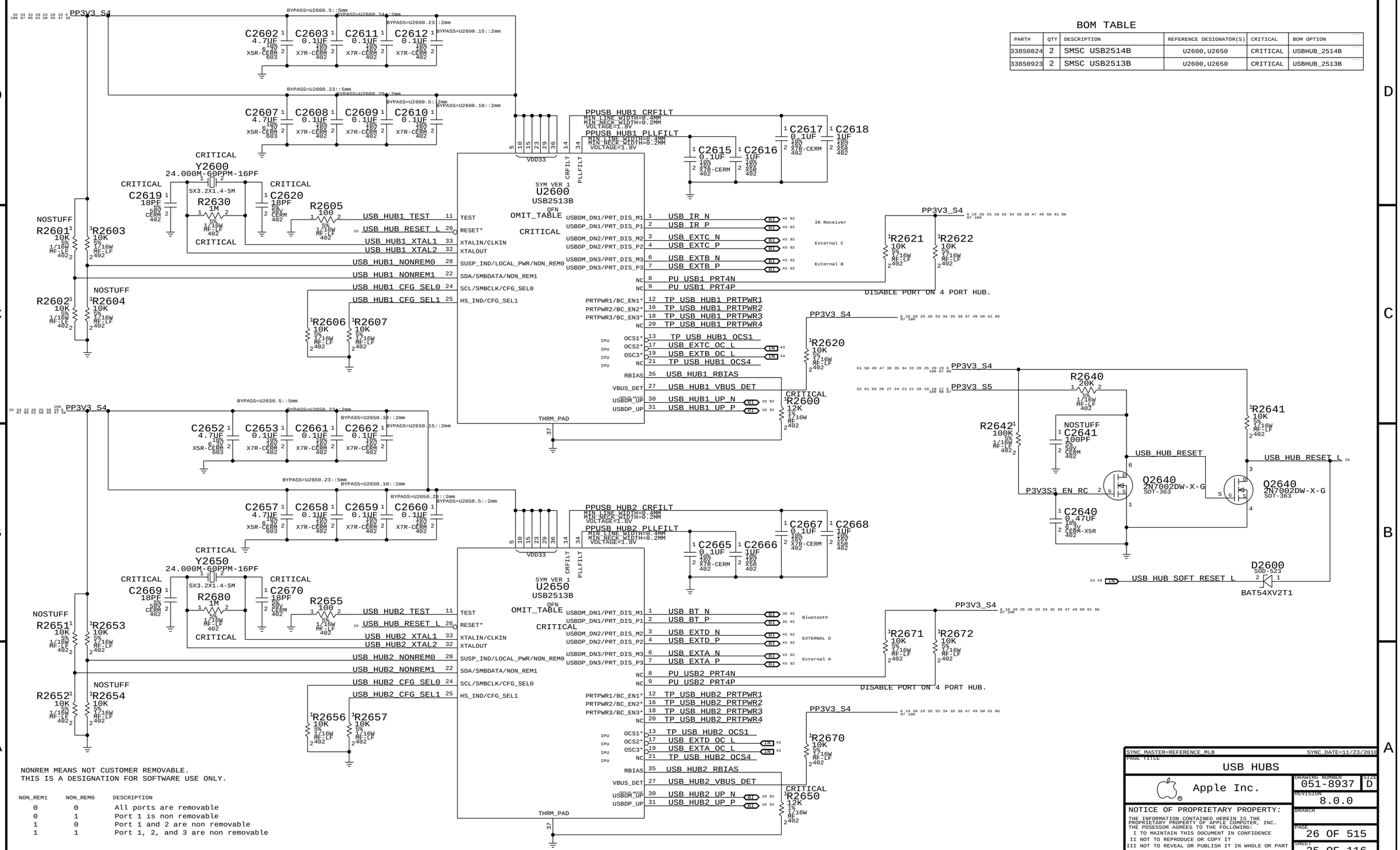

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0824	2	SMSC USB2514B	U2600,U2650	CRITICAL	USBHUB_2514B
338S0923	2	SMSC USB2513B	U2600,U2650	CRITICAL	USBHUB_2513B

NONREM MEANS NOT CUSTOMER REMOVABLE.
THIS IS A DESIGNATION FOR SOFTWARE USE ONLY.

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2016

PAGE TITLE: USB HUBS

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REVISION: 8.0.0

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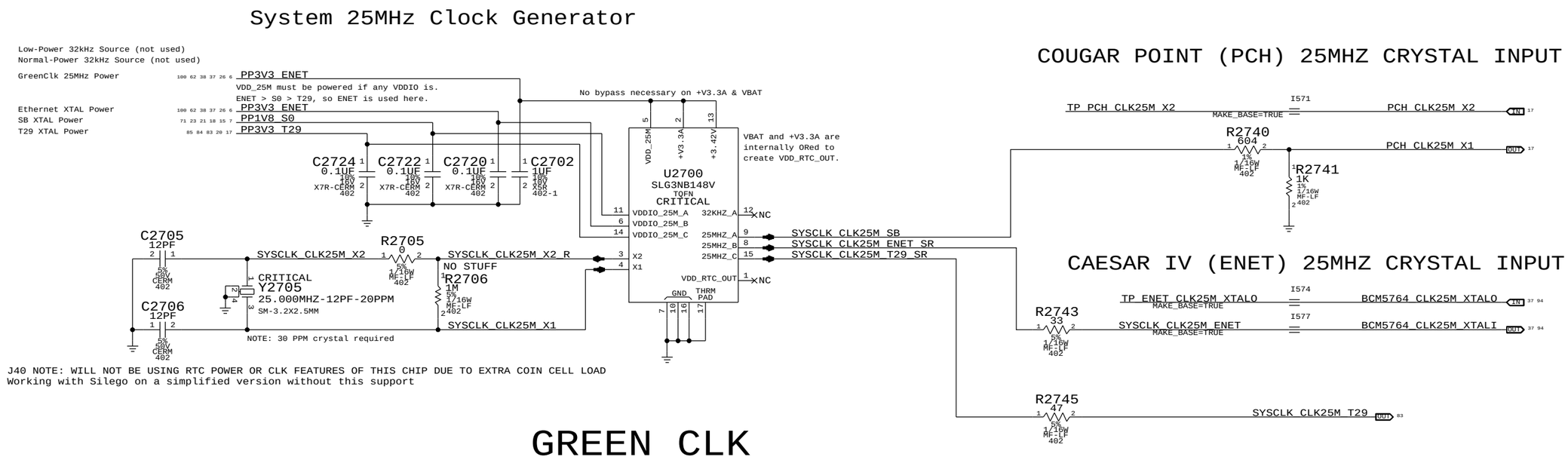

SYNC_MASTER=J40S SYNC_DATE=11/21/2012

PAGE TITLE

CLOCKS, CRYSTALS

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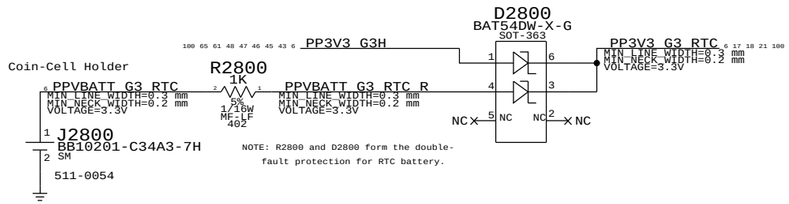
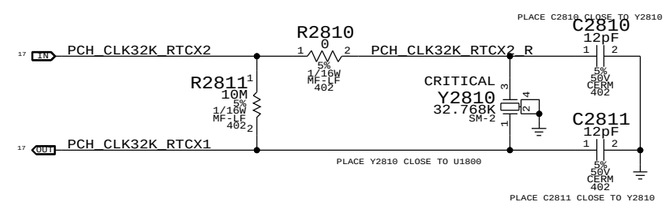
RTC Power Sources

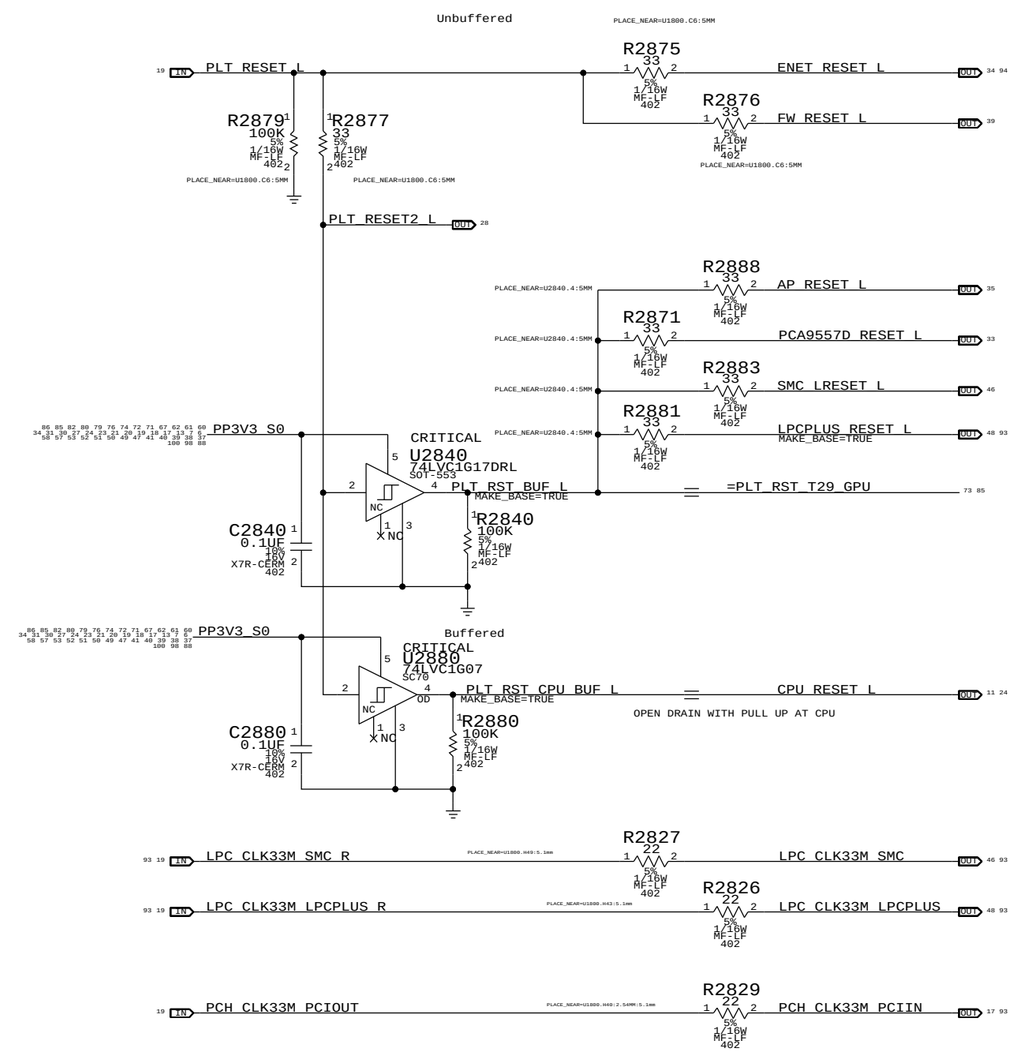


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
742-0062	1	BAT,COIN,LICF,BR2032,3V,190MAH	BAT	CRITICAL	

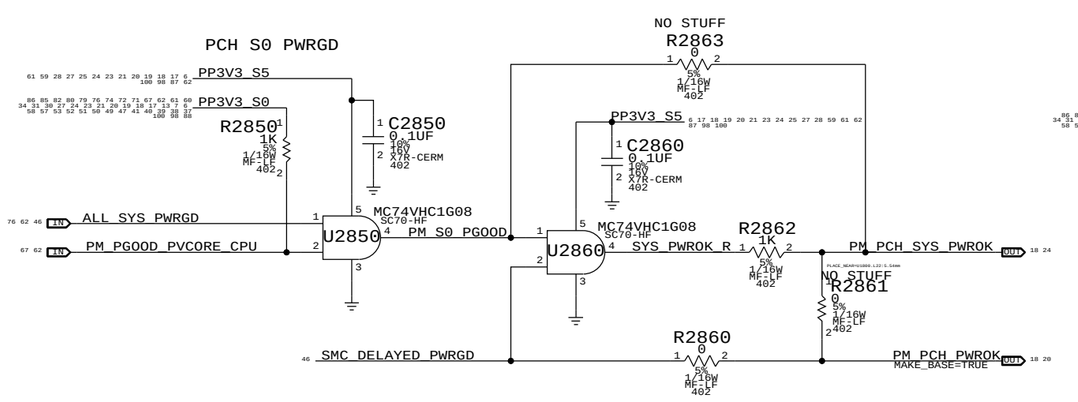
PCH RTC Crystal



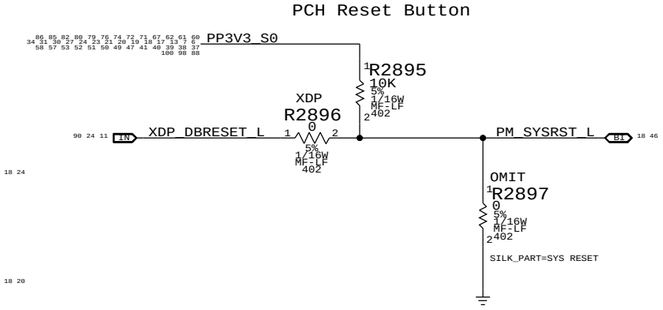
Platform Reset Connections



PCH S0 PWRGD



PCH Reset Button



SYNC_MASTER=J40G SYNC_DATE=12/13/2012

PAGE TITLE

RTC SUPPORT, RESETS

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DRAWING NUMBER 051-8937 SIZE D

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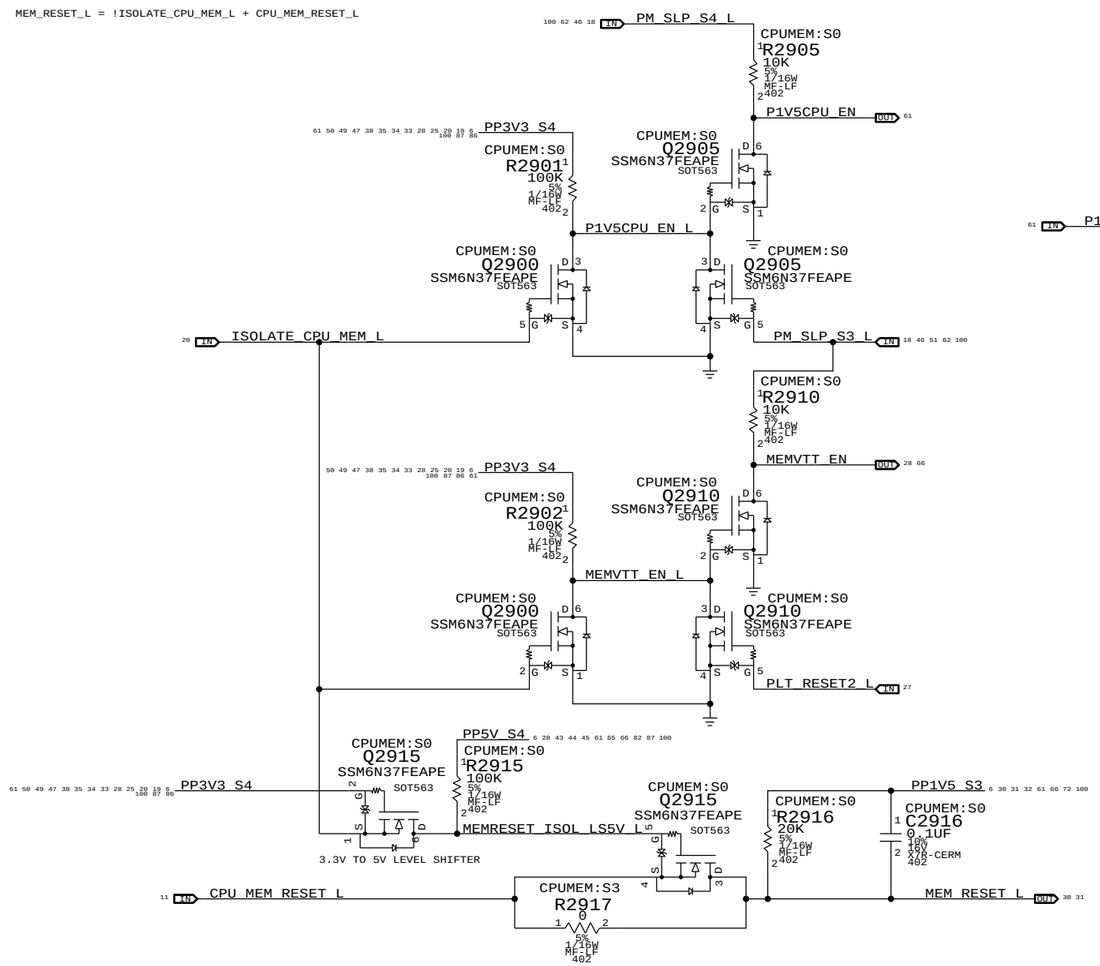
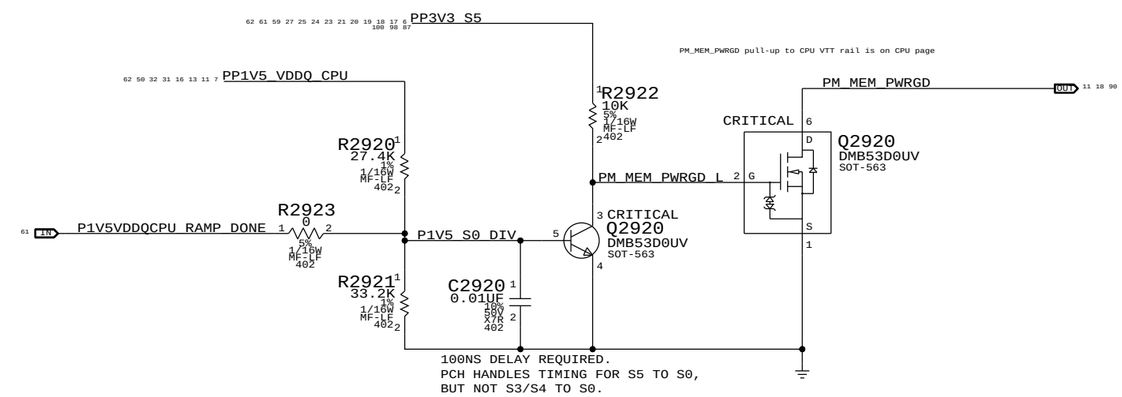
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

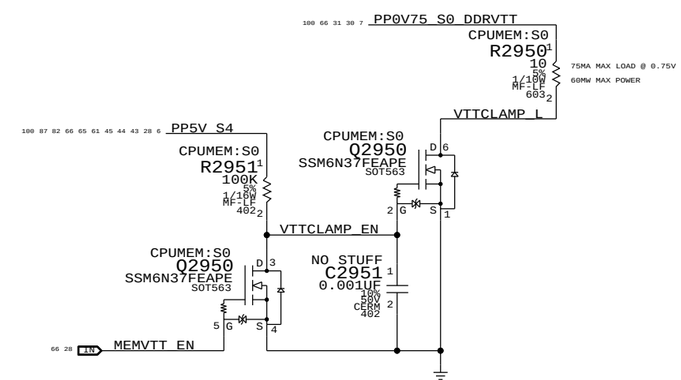


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
	1	0	1	1	1	1	1	1
to	2	0	0	1	1	1	0	1
	3	0	0	0	1	X	0	0
S3	4	0	0	1	1	X	0	1
	5	0	1	1	1	0 (*)	1	1
to	6	0	1	1	1	1	1	1
S0	7	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE
CPU Memory S3 Support

Apple Inc.

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SANDYBRIDGE CPU DOES NOT USE DATA MASK (DM) BITS.
PER PDG, TIE DM BITS TO GND.

Host Partition A 0 -> SO-DIMM A 0

MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=MEM_A_DQS_P<7>	B1 30
MEM_A_DQS_N<0>	MAKE_BASE=TRUE	=MEM_A_DQS_N<7>	B1 30
	MAKE_BASE=TRUE	=MEM_A_DM<7>	OUT 30
MEM_A_DQ<0>	MAKE_BASE=TRUE	=MEM_A_DQ<63>	B1 30
MEM_A_DQ<1>	MAKE_BASE=TRUE	=MEM_A_DQ<62>	B1 30
MEM_A_DQ<2>	MAKE_BASE=TRUE	=MEM_A_DQ<60>	B1 30
MEM_A_DQ<3>	MAKE_BASE=TRUE	=MEM_A_DQ<61>	B1 30
MEM_A_DQ<4>	MAKE_BASE=TRUE	=MEM_A_DQ<59>	B1 30
MEM_A_DQ<5>	MAKE_BASE=TRUE	=MEM_A_DQ<58>	B1 30
MEM_A_DQ<6>	MAKE_BASE=TRUE	=MEM_A_DQ<57>	B1 30
MEM_A_DQ<7>	MAKE_BASE=TRUE	=MEM_A_DQ<56>	B1 30

Host Partition A 1 -> SO-DIMM A 1

MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=MEM_A_DQS_P<6>	B1 30
MEM_A_DQS_N<1>	MAKE_BASE=TRUE	=MEM_A_DQS_N<6>	B1 30
		=MEM_A_DM<6>	OUT 30
MEM_A_DQ<8>		=MEM_A_DQ<55>	B1 30
MEM_A_DQ<9>	MAKE_BASE=TRUE	=MEM_A_DQ<54>	B1 30
MEM_A_DQ<10>	MAKE_BASE=TRUE	=MEM_A_DQ<53>	B1 30
MEM_A_DQ<11>	MAKE_BASE=TRUE	=MEM_A_DQ<52>	B1 30
MEM_A_DQ<12>	MAKE_BASE=TRUE	=MEM_A_DQ<51>	B1 30
MEM_A_DQ<13>	MAKE_BASE=TRUE	=MEM_A_DQ<50>	B1 30
MEM_A_DQ<14>	MAKE_BASE=TRUE	=MEM_A_DQ<49>	B1 30
MEM_A_DQ<15>	MAKE_BASE=TRUE	=MEM_A_DQ<48>	B1 30

Host Partition A 2 -> SO-DIMM A 2

MEM_A_DQS_P<2>	MAKE_BASE=TRUE	=MEM_A_DQS_P<5>	B1 30
MEM_A_DQS_N<2>	MAKE_BASE=TRUE	=MEM_A_DQS_N<5>	B1 30
	MAKE_BASE=TRUE	=MEM_A_DM<5>	OUT 30
MEM_A_DQ<16>		=MEM_A_DQ<47>	B1 30
MEM_A_DQ<17>	MAKE_BASE=TRUE	=MEM_A_DQ<46>	B1 30
MEM_A_DQ<18>	MAKE_BASE=TRUE	=MEM_A_DQ<45>	B1 30
MEM_A_DQ<19>	MAKE_BASE=TRUE	=MEM_A_DQ<44>	B1 30
MEM_A_DQ<20>	MAKE_BASE=TRUE	=MEM_A_DQ<43>	B1 30
MEM_A_DQ<21>	MAKE_BASE=TRUE	=MEM_A_DQ<42>	B1 30
MEM_A_DQ<22>	MAKE_BASE=TRUE	=MEM_A_DQ<41>	B1 30
MEM_A_DQ<23>	MAKE_BASE=TRUE	=MEM_A_DQ<40>	B1 30

Host Partition A 3 -> SO-DIMM A 3

MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=MEM_A_DQS_P<4>	B1 30
MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=MEM_A_DQS_N<4>	B1 30
		=MEM_A_DM<4>	OUT 30
MEM_A_DQ<24>		=MEM_A_DQ<39>	B1 30
MEM_A_DQ<25>	MAKE_BASE=TRUE	=MEM_A_DQ<38>	B1 30
MEM_A_DQ<26>	MAKE_BASE=TRUE	=MEM_A_DQ<37>	B1 30
MEM_A_DQ<27>	MAKE_BASE=TRUE	=MEM_A_DQ<36>	B1 30
MEM_A_DQ<28>	MAKE_BASE=TRUE	=MEM_A_DQ<35>	B1 30
MEM_A_DQ<29>	MAKE_BASE=TRUE	=MEM_A_DQ<34>	B1 30
MEM_A_DQ<30>	MAKE_BASE=TRUE	=MEM_A_DQ<33>	B1 30
MEM_A_DQ<31>	MAKE_BASE=TRUE	=MEM_A_DQ<32>	B1 30

Host Partition A 4 -> SO-DIMM A 4

MEM_A_DQS_P<4>	MAKE_BASE=TRUE	=MEM_A_DQS_P<3>	B1 30
MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=MEM_A_DQS_N<3>	B1 30
	MAKE_BASE=TRUE	=MEM_A_DM<3>	OUT 30
MEM_A_DQ<32>		=MEM_A_DQ<31>	B1 30
MEM_A_DQ<33>	MAKE_BASE=TRUE	=MEM_A_DQ<30>	B1 30
MEM_A_DQ<34>	MAKE_BASE=TRUE	=MEM_A_DQ<29>	B1 30
MEM_A_DQ<35>	MAKE_BASE=TRUE	=MEM_A_DQ<28>	B1 30
MEM_A_DQ<36>	MAKE_BASE=TRUE	=MEM_A_DQ<27>	B1 30
MEM_A_DQ<37>	MAKE_BASE=TRUE	=MEM_A_DQ<26>	B1 30
MEM_A_DQ<38>	MAKE_BASE=TRUE	=MEM_A_DQ<25>	B1 30
MEM_A_DQ<39>	MAKE_BASE=TRUE	=MEM_A_DQ<24>	B1 30

Host Partition A 5 -> SO-DIMM A 5

MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=MEM_A_DQS_P<2>	B1 30
MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=MEM_A_DQS_N<2>	B1 30
	MAKE_BASE=TRUE	=MEM_A_DM<2>	OUT 30
MEM_A_DQ<40>		=MEM_A_DQ<23>	B1 30
MEM_A_DQ<41>	MAKE_BASE=TRUE	=MEM_A_DQ<22>	B1 30
MEM_A_DQ<42>	MAKE_BASE=TRUE	=MEM_A_DQ<21>	B1 30
MEM_A_DQ<43>	MAKE_BASE=TRUE	=MEM_A_DQ<20>	B1 30
MEM_A_DQ<44>	MAKE_BASE=TRUE	=MEM_A_DQ<19>	B1 30
MEM_A_DQ<45>	MAKE_BASE=TRUE	=MEM_A_DQ<18>	B1 30
MEM_A_DQ<46>	MAKE_BASE=TRUE	=MEM_A_DQ<17>	B1 30
MEM_A_DQ<47>	MAKE_BASE=TRUE	=MEM_A_DQ<16>	B1 30

Host Partition A 6 -> SO-DIMM A 6

MEM_A_DQS_P<6>	MAKE_BASE=TRUE	=MEM_A_DQS_P<1>	B1 30
MEM_A_DQS_N<6>	MAKE_BASE=TRUE	=MEM_A_DQS_N<1>	B1 30
	MAKE_BASE=TRUE	=MEM_A_DM<1>	OUT 30
MEM_A_DQ<48>		=MEM_A_DQ<15>	B1 30
MEM_A_DQ<49>	MAKE_BASE=TRUE	=MEM_A_DQ<14>	B1 30
MEM_A_DQ<50>	MAKE_BASE=TRUE	=MEM_A_DQ<13>	B1 30
MEM_A_DQ<51>	MAKE_BASE=TRUE	=MEM_A_DQ<12>	B1 30
MEM_A_DQ<52>	MAKE_BASE=TRUE	=MEM_A_DQ<11>	B1 30
MEM_A_DQ<53>	MAKE_BASE=TRUE	=MEM_A_DQ<10>	B1 30
MEM_A_DQ<54>	MAKE_BASE=TRUE	=MEM_A_DQ<9>	B1 30
MEM_A_DQ<55>	MAKE_BASE=TRUE	=MEM_A_DQ<8>	B1 30

Host Partition A 7 -> SO-DIMM A 7

MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=MEM_A_DQS_P<0>	B1 30
MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=MEM_A_DQS_N<0>	B1 30
	MAKE_BASE=TRUE	=MEM_A_DM<0>	OUT 30
MEM_A_DQ<56>		=MEM_A_DQ<7>	B1 30
MEM_A_DQ<57>	MAKE_BASE=TRUE	=MEM_A_DQ<6>	B1 30
MEM_A_DQ<58>	MAKE_BASE=TRUE	=MEM_A_DQ<5>	B1 30
MEM_A_DQ<59>	MAKE_BASE=TRUE	=MEM_A_DQ<4>	B1 30
MEM_A_DQ<60>	MAKE_BASE=TRUE	=MEM_A_DQ<3>	B1 30
MEM_A_DQ<61>	MAKE_BASE=TRUE	=MEM_A_DQ<2>	B1 30
MEM_A_DQ<62>	MAKE_BASE=TRUE	=MEM_A_DQ<1>	B1 30
MEM_A_DQ<63>	MAKE_BASE=TRUE	=MEM_A_DQ<0>	B1 30

Host Partition B 0 -> SO-DIMM B 0

MEM_B_DQS_P<0>	MAKE_BASE=TRUE	=MEM_B_DQS_P<7>	B1 31
MEM_B_DQS_N<0>	MAKE_BASE=TRUE	=MEM_B_DQS_N<7>	B1 31
	MAKE_BASE=TRUE	=MEM_B_DM<7>	OUT 31
MEM_B_DQ<0>		=MEM_B_DQ<63>	B1 31
MEM_B_DQ<1>	MAKE_BASE=TRUE	=MEM_B_DQ<62>	B1 31
MEM_B_DQ<2>	MAKE_BASE=TRUE	=MEM_B_DQ<60>	B1 31
MEM_B_DQ<3>	MAKE_BASE=TRUE	=MEM_B_DQ<61>	B1 31
MEM_B_DQ<4>	MAKE_BASE=TRUE	=MEM_B_DQ<59>	B1 31
MEM_B_DQ<5>	MAKE_BASE=TRUE	=MEM_B_DQ<58>	B1 31
MEM_B_DQ<6>	MAKE_BASE=TRUE	=MEM_B_DQ<57>	B1 31
MEM_B_DQ<7>	MAKE_BASE=TRUE	=MEM_B_DQ<56>	B1 31

Host Partition B 1 -> SO-DIMM B 2

MEM_B_DQS_P<1>	MAKE_BASE=TRUE	=MEM_B_DQS_P<6>	B1 31
MEM_B_DQS_N<1>	MAKE_BASE=TRUE	=MEM_B_DQS_N<6>	B1 31
	MAKE_BASE=TRUE	=MEM_B_DM<6>	OUT 31
MEM_B_DQ<8>		=MEM_B_DQ<55>	B1 31
MEM_B_DQ<9>	MAKE_BASE=TRUE	=MEM_B_DQ<54>	B1 31
MEM_B_DQ<10>	MAKE_BASE=TRUE	=MEM_B_DQ<53>	B1 31
MEM_B_DQ<11>	MAKE_BASE=TRUE	=MEM_B_DQ<52>	B1 31
MEM_B_DQ<12>	MAKE_BASE=TRUE	=MEM_B_DQ<51>	B1 31
MEM_B_DQ<13>	MAKE_BASE=TRUE	=MEM_B_DQ<50>	B1 31
MEM_B_DQ<14>	MAKE_BASE=TRUE	=MEM_B_DQ<49>	B1 31
MEM_B_DQ<15>	MAKE_BASE=TRUE	=MEM_B_DQ<48>	B1 31

Host Partition B 2 -> SO-DIMM B 3

MEM_B_DQS_P<2>	MAKE_BASE=TRUE	=MEM_B_DQS_P<5>	B1 31
MEM_B_DQS_N<2>	MAKE_BASE=TRUE	=MEM_B_DQS_N<5>	B1 31
	MAKE_BASE=TRUE	=MEM_B_DM<5>	OUT 31
MEM_B_DQ<16>		=MEM_B_DQ<47>	B1 31
MEM_B_DQ<17>	MAKE_BASE=TRUE	=MEM_B_DQ<46>	B1 31
MEM_B_DQ<18>	MAKE_BASE=TRUE	=MEM_B_DQ<45>	B1 31
MEM_B_DQ<19>	MAKE_BASE=TRUE	=MEM_B_DQ<44>	B1 31
MEM_B_DQ<20>	MAKE_BASE=TRUE	=MEM_B_DQ<43>	B1 31
MEM_B_DQ<21>	MAKE_BASE=TRUE	=MEM_B_DQ<42>	B1 31
MEM_B_DQ<22>	MAKE_BASE=TRUE	=MEM_B_DQ<41>	B1 31
MEM_B_DQ<23>	MAKE_BASE=TRUE	=MEM_B_DQ<40>	B1 31

Host Partition B 3 -> SO-DIMM B 1

MEM_B_DQS_P<3>	MAKE_BASE=TRUE	=MEM_B_DQS_P<4>	B1 31
MEM_B_DQS_N<3>	MAKE_BASE=TRUE	=MEM_B_DQS_N<4>	B1 31
		=MEM_B_DM<4>	OUT 31
MEM_B_DQ<24>		=MEM_B_DQ<39>	B1 31
MEM_B_DQ<25>	MAKE_BASE=TRUE	=MEM_B_DQ<38>	B1 31
MEM_B_DQ<26>	MAKE_BASE=TRUE	=MEM_B_DQ<37>	B1 31
MEM_B_DQ<27>	MAKE_BASE=TRUE	=MEM_B_DQ<36>	B1 31
MEM_B_DQ<28>	MAKE_BASE=TRUE	=MEM_B_DQ<35>	B1 31
MEM_B_DQ<29>	MAKE_BASE=TRUE	=MEM_B_DQ<34>	B1 31
MEM_B_DQ<30>	MAKE_BASE=TRUE	=MEM_B_DQ<33>	B1 31
MEM_B_DQ<31>	MAKE_BASE=TRUE	=MEM_B_DQ<32>	B1 31

Host Partition B 4 -> SO-DIMM B 4

MEM_B_DQS_P<4>	MAKE_BASE=TRUE	=MEM_B_DQS_P<3>	B1 31
MEM_B_DQS_N<4>	MAKE_BASE=TRUE	=MEM_B_DQS_N<3>	B1 31
	MAKE_BASE=TRUE	=MEM_B_DM<3>	OUT 31
MEM_B_DQ<32>		=MEM_B_DQ<31>	B1 31
MEM_B_DQ<33>	MAKE_BASE=TRUE	=MEM_B_DQ<30>	B1 31
MEM_B_DQ<34>	MAKE_BASE=TRUE	=MEM_B_DQ<29>	B1 31
MEM_B_DQ<35>	MAKE_BASE=TRUE	=MEM_B_DQ<28>	B1 31
MEM_B_DQ<36>	MAKE_BASE=TRUE	=MEM_B_DQ<27>	B1 31
MEM_B_DQ<37>	MAKE_BASE=TRUE	=MEM_B_DQ<26>	B1 31
MEM_B_DQ<38>	MAKE_BASE=TRUE	=MEM_B_DQ<25>	B1 31
MEM_B_DQ<39>	MAKE_BASE=TRUE	=MEM_B_DQ<24>	B1 31

Host Partition B 5 -> SO-DIMM B 5

MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=MEM_B_DQS_P<2>	B1 31
MEM_B_DQS_N<5>	MAKE_BASE=TRUE	=MEM_B_DQS_N<2>	B1 31
	MAKE_BASE=TRUE	=MEM_B_DM<2>	OUT 31
MEM_B_DQ<40>		=MEM_B_DQ<23>	B1 31
MEM_B_DQ<41>	MAKE_BASE=TRUE	=MEM_B_DQ<22>	B1 31
MEM_B_DQ<42>	MAKE_BASE=TRUE	=MEM_B_DQ<21>	B1 31
MEM_B_DQ<43>	MAKE_BASE=TRUE	=MEM_B_DQ<20>	B1 31
MEM_B_DQ<44>	MAKE_BASE=TRUE	=MEM_B_DQ<19>	B1 31
MEM_B_DQ<45>	MAKE_BASE=TRUE	=MEM_B_DQ<18>	B1 31
MEM_B_DQ<46>	MAKE_BASE=TRUE	=MEM_B_DQ<17>	B1 31
MEM_B_DQ<47>	MAKE_BASE=TRUE	=MEM_B_DQ<16>	B1 31

Host Partition B 6 -> SO-DIMM B 6

MEM_B_DQS_P<6>	MAKE_BASE=TRUE	=MEM_B_DQS_P<1>	B1 31
MEM_B_DQS_N<6>	MAKE_BASE=TRUE	=MEM_B_DQS_N<1>	B1 31
	MAKE_BASE=TRUE	=MEM_B_DM<1>	OUT 31
MEM_B_DQ<48>		=MEM_B_DQ<15>	B1 31
MEM_B_DQ<49>	MAKE_BASE=TRUE	=MEM_B_DQ<14>	B1 31
MEM_B_DQ<50>	MAKE_BASE=TRUE	=MEM_B_DQ<13>	B1 31
MEM_B_DQ<51>	MAKE_BASE=TRUE	=MEM_B_DQ<12>	B1 31
MEM_B_DQ<52>	MAKE_BASE=TRUE	=MEM_B_DQ<11>	B1 31
MEM_B_DQ<53>	MAKE_BASE=TRUE	=MEM_B_DQ<10>	B1 31
MEM_B_DQ<54>	MAKE_BASE=TRUE	=MEM_B_DQ<9>	B1 31
MEM_B_DQ<55>	MAKE_BASE=TRUE	=MEM_B_DQ<8>	B1 31

Host Partition B 7 -> SO-DIMM B 7

MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=MEM_B_DQS_P<0>	B1 31
MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=MEM_B_DQS_N<0>	B1 31
	MAKE_BASE=TRUE	=MEM_B_DM<0>	OUT 31
MEM_B_DQ<56>		=MEM_B_DQ<7>	B1 31
MEM_B_DQ<57>	MAKE_BASE=TRUE	=MEM_B_DQ<6>	B1 31
MEM_B_DQ<58>	MAKE_BASE=TRUE	=MEM_B_DQ<5>	B1 31
MEM_B_DQ<59>	MAKE_BASE=TRUE	=MEM_B_DQ<4>	B1 31
MEM_B_DQ<60>	MAKE_BASE=TRUE	=MEM_B_DQ<3>	B1 31
MEM_B_DQ<61>	MAKE_BASE=TRUE	=MEM_B_DQ<2>	B1 31
MEM_B_DQ<62>	MAKE_BASE=TRUE	=MEM_B_DQ<1>	B1 31
MEM_B_DQ<63>	MAKE_BASE=TRUE	=MEM_B_DQ<0>	B1 31

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SO-DIMM Pinswaps

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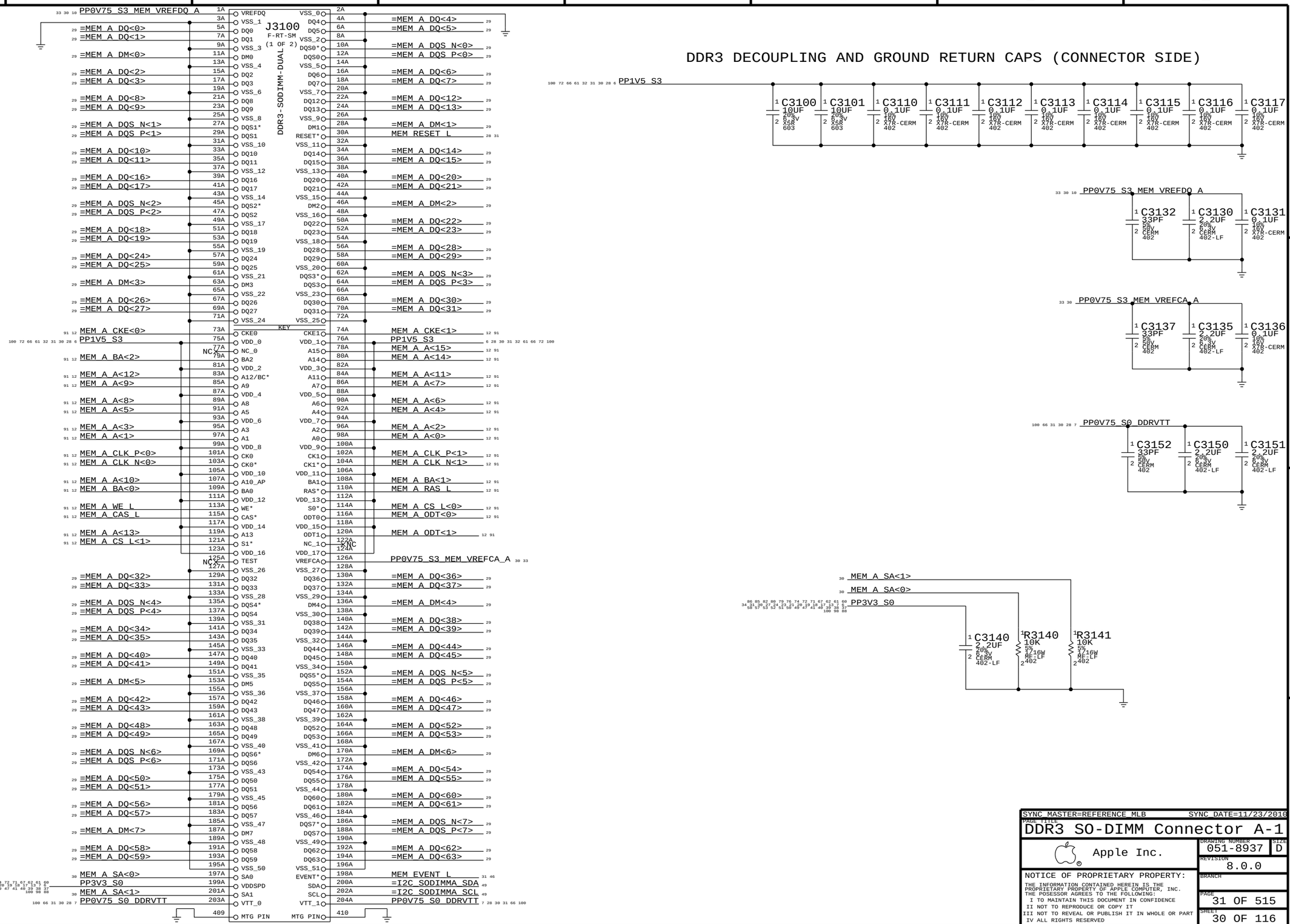
DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)



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DDR3 SO-DIMM Connector A-1

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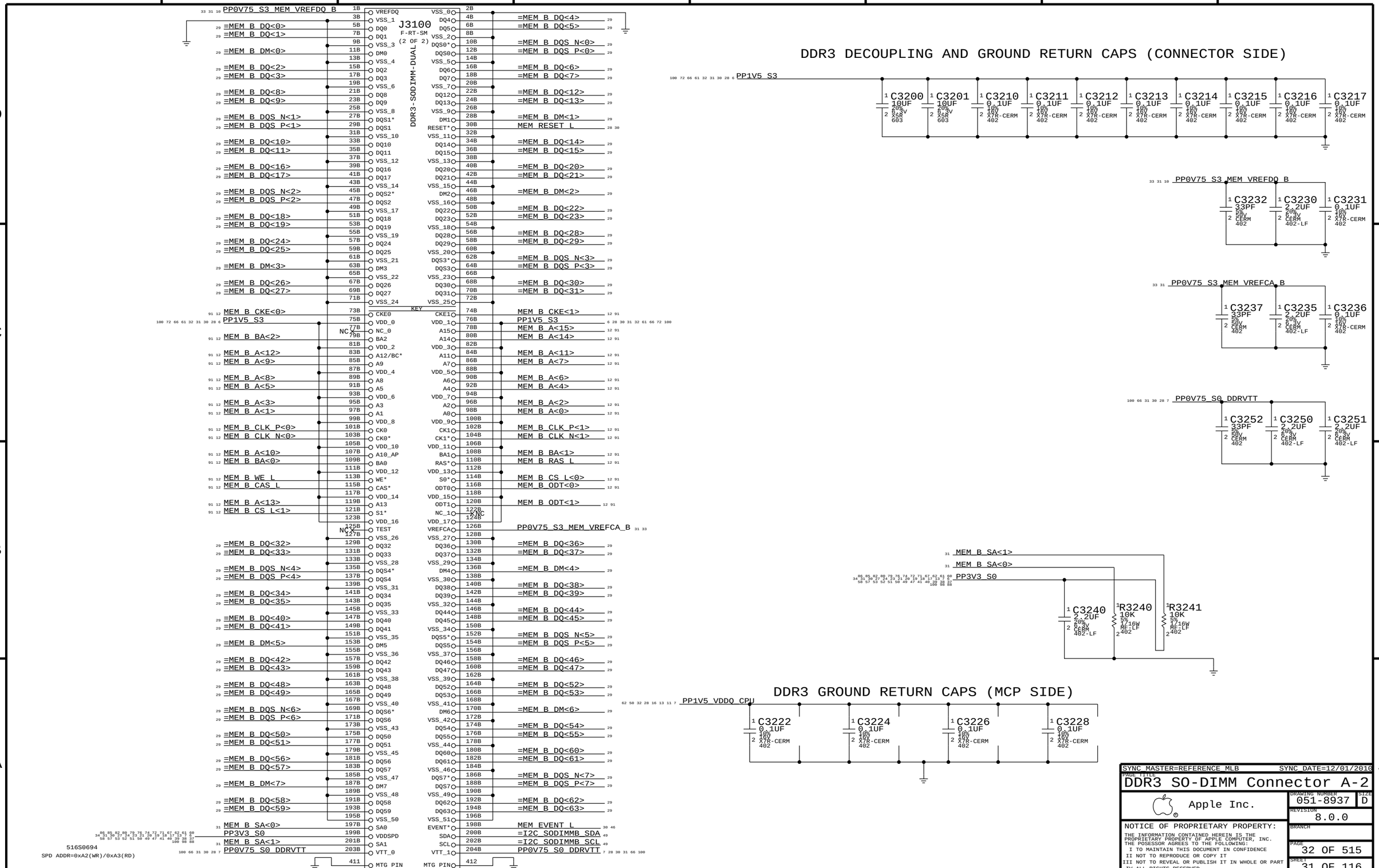
J3100
F-RT-SM
(2 OF 2)
DDR3-SODIMM-DUAL
KEY
PP0V75_S3_MEM_VREFDQ_B
PP1V5_S3
PP0V75_S3_MEM_VREFCA_B
PP0V75_S0_DDRVTT
PP3V3_S0
PP1V5_VDDQ_CPU
MEM_RESET_L
MEM_EVENT_L
=I2C_SODIMMB_SDA
=I2C_SODIMMB_SCL
DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)
C3200 10UF 20% 6.3V X5R 603
C3201 10UF 20% 6.3V X5R 603
C3210 0.1UF 10% 16V X7R-CERM 402
C3211 0.1UF 10% 16V X7R-CERM 402
C3212 0.1UF 10% 16V X7R-CERM 402
C3213 0.1UF 10% 16V X7R-CERM 402
C3214 0.1UF 10% 16V X7R-CERM 402
C3215 0.1UF 10% 16V X7R-CERM 402
C3216 0.1UF 10% 16V X7R-CERM 402
C3217 0.1UF 10% 16V X7R-CERM 402
C3232 33PF 5% 50V CERM 402
C3230 2.2UF 20% 6.3V CERM 402-LF
C3231 0.1UF 10% 16V X7R-CERM 402
C3237 33PF 5% 50V CERM 402
C3235 2.2UF 20% 6.3V CERM 402-LF
C3236 0.1UF 10% 16V X7R-CERM 402
C3252 33PF 5% 50V CERM 402
C3250 2.2UF 20% 6.3V CERM 402-LF
C3251 2.2UF 20% 6.3V CERM 402-LF
C3240 2.2UF 20% 6.3V CERM 402-LF
R3240 10K 5% 1/16W MF-LF 402
R3241 10K 5% 1/16W MF-LF 402
DDR3 GROUND RETURN CAPS (MCP SIDE)
C3222 0.1UF 10% 16V X7R-CERM 402
C3224 0.1UF 10% 16V X7R-CERM 402
C3226 0.1UF 10% 16V X7R-CERM 402
C3228 0.1UF 10% 16V X7R-CERM 402
516S0694
SPD ADDR=0xA2(WR)/0xA3(RD)
SYNC MASTER=REFERENCE_MLB
SYNC DATE=12/01/2010
PAGE TITLE
DDR3 SO-DIMM Connector A-2
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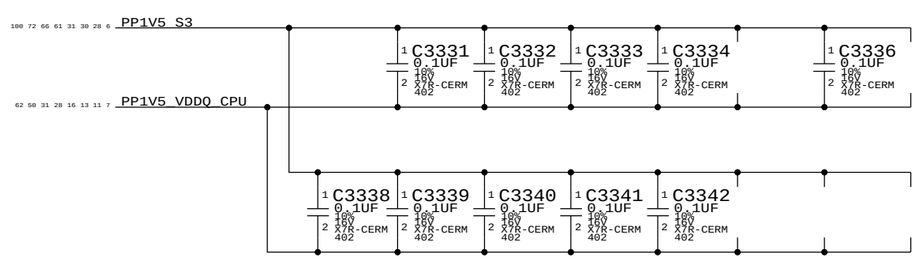

STICHING CAPS.

PLACE ACROSS PLANE SPLIT BETWEEN THESE RAIL
WHERE THE MEMORY ROUTES ARE.
EXTRAS CAN BE DELETED.

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DDR3 Support

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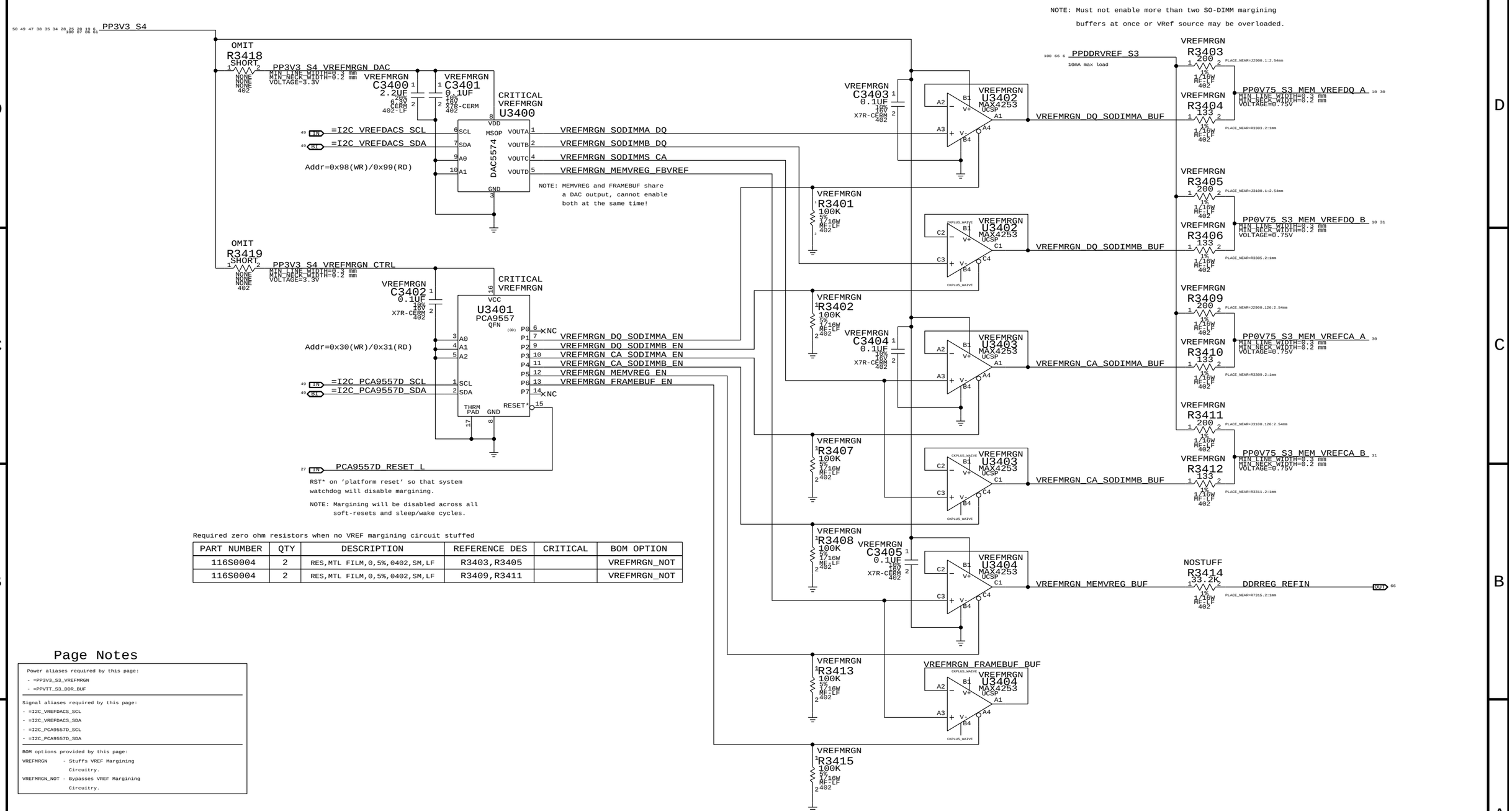

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3403,R3405		VREFMRGN_NOT
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3409,R3411		VREFMRGN_NOT

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN - Stuffs VREF Margining Circuitry.
VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+33uA - -33uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE
FSB/DDR3/FRAMEBUF Vref Margining

Apple Inc.

DRAWING NUMBER 051-8937 SIZE D
REVISION 8.0.0
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Caesar IV Support

EMI CAPS

PLACE NEXT TO J3500

NOSTUFF C3511 10PF 5% 50V CERM 402 — SDCONN_CMD_R
NOSTUFF C3512 10PF 5% 50V CERM 402 — SDCONN_DATA_R<0>
NOSTUFF C3513 10PF 5% 50V CERM 402 — SDCONN_DATA_R<1>
NOSTUFF C3514 10PF 5% 50V CERM 402 — SDCONN_DATA_R<2>
NOSTUFF C3515 10PF 5% 50V CERM 402 — SDCONN_DATA_R<3>
NOSTUFF C3516 10PF 5% 50V CERM 402 — SDCONN_DATA_R<4>
NOSTUFF C3517 10PF 5% 50V CERM 402 — SDCONN_DATA_R<5>
NOSTUFF C3518 10PF 5% 50V CERM 402 — SDCONN_DATA_R<6>
NOSTUFF C3519 10PF 5% 50V CERM 402 — SDCONN_DATA_R<7>
NOSTUFF C3520 10PF 5% 50V CERM 402 — SDCONN_WP
NOSTUFF C3521 10PF 5% 50V CERM 402 — SDCONN_DETECT

RESISTER ON FERRITE PADS!!

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0004	3	RES,ZERO OHM,0402	L3540,L3541,L3550	
152S1491	1	IND,WW,43NH,5%,100MA,0402	L3551	

TPS2065-1 HAS ACTIVE LOAD DISCHARGE SO R3505 IS NOSTUFF.

1.0A LIMIT

U3500 TPS2065-1 CRITICAL — IN0, IN1, DGN, OUT0, OUT1, OUT2, EN, OC*, THRM PAD, GND PAD

PP3V3_S0 — C3501 10UF 20% 6.3V X5R 603; C3500 0.1UF 10% 16V X7R-CERM 402; R3502 10K 5% 1/16W MF-LF 402 — PU_SDCONN_OC_L

ENET_CR_PWREN

MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_SW_SD_PWR — C3507 10UF 20% 6.3V X5R 603; C3505 0.1UF 10% 16V X7R-CERM 402; NOSTUFF R3505 39.2K 1% 1/16W MF-LF 402

RESISTER ON FERRITE PADS!!
PLACE AT SOURCE.

SDCONN_CLK — OMIT_TABLE L3540 10NH-300MA 0402 — SDCONNF_CLK_FF
NOSTUFF C3542 15PF 1% 50V C0G 402; NOSTUFF C3541 15PF 1% 50V C0G 402

OMIT_TABLE L3550 13NH-430MA 0402 — SDCONNF_CLK
OMIT_TABLE L3551 68NH-140MA 0402 — SDCONN_CLK_FF
NOSTUFF C3551 15PF 1% 50V C0G 402; NOSTUFF C3550 22PF 5% 50V CERM 402

RESISTER ON FERRITE PADS!!
PLACE AT CONNECTOR.

SDCONN_CMD	R3555	10
SDCONN_DATA<0>	R3560	10
SDCONN_DATA<1>	R3561	10
SDCONN_DATA<2>	R3562	10
SDCONN_DATA<3>	R3563	10
SDCONN_DATA<4>	R3564	10
SDCONN_DATA<5>	R3565	10
SDCONN_DATA<6>	R3566	10
SDCONN_DATA<7>	R3567	10

5% 1/16W MF-LF 402

CRITICAL J3500 SD-CARD-K40-K41 F-RT-TH — 516-0230

Pin	Signal
3	VSS
6	VSS
5	CLK
2	CMD
7	DAT0
8	DAT1
9	DAT2
1	CD/DAT3
10	DAT4
11	DAT5
12	DAT6
13	DAT7
14	CARD_DETECT_SW (NC SWITCH)
15	CARD_DETECT_GND
16	WRITE_PROTECT_SW
4	VDD
17	SHLD_PIN
18	SHLD_PIN
19	SHLD_PIN
20	SHLD_PIN

SDCONN_CLK_R
SDCONN_CMD_R
SDCONN_DATA_R<0>
SDCONN_DATA_R<1>
SDCONN_DATA_R<2>
SDCONN_DATA_R<3>
SDCONN_DATA_R<4>
SDCONN_DATA_R<5>
SDCONN_DATA_R<6>
SDCONN_DATA_R<7>
SDCONN_DETECT
SDCONN_WP

SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.

PP3V3_S4 — C3530 1UF 10% 10V X5R 402-1

CRITICAL U3530 SLG4AP014V TDFN — VDD, LOW_PWR, RST_IN*, DET_IN (IPU), GND, THRM PAD, RST LOGIC, DLY, DET, RST_OUT* (OD), DET_CHNGD* (OD), DET_OUT

ENET_LOW_PWR — SLG_ENET_RESET_R_L — R3514 0 5% 1/16W MF-LF 402 — CIV_ENET_RESET_L

ENET_RESET_L — R3511 0 5% 1/16W MF-LF 402 — SLG_ENET_RESET_L
-> FROM PCH GPIO

NOSTUFF R3510 10K 5% 1/16W MF-LF 402

SDCONN_DETECT_L — SDCONN_STATE_CHANGE_S1R — NOSTUFF R3531 0 5% 1/16W MF-LF 402 — SDCONN_STATE_CHANGE
-> TO PCH GPIO

ENET_CR_DETECT_L
-> TO ENET CHIP

PP3V3_S4 — R3530 100K 5% 1/16W MF-LF 402 — Q3530 SSM3K15FV SOD-VESM-HF — SDCONN_DETECT
FROM SD CONN ->

*** Need to confirm with SW whether LATCH is required.
(SDCONN_STATE_RST_L will be required with LATCH)

DLY block is 20ms nominal
When ENET_LOW_PWR deasserts, RST_OUT# deasserts for >80ms, then asserts for 10ms regradless of RST_IN# state. Otherwise RST_OUT# follows RST_IN#

NOSTUFF R3512 0 5% 1/16W MF-LF 402

CRITICAL C3535 1UF 10% 10V X5R 402-1

CRITICAL U3535 SLG4AP014V TDFN — VDD, LOW_PWR, RST_IN*, DET_IN (IPU), GND, THRM PAD, RST LOGIC, DLY, DET, RST_OUT* (OD), DET_CHNGD* (OD), DET_OUT — NC, NC

SDCONN_STATE_CHANGE_S2R — R3535 0 5% 1/16W MF-LF 402

WE WANT SDCONN_STATE_CHANGE TO WORK THE SAME IN S0 AS IN S3/4.
COPY CIRCUIT BUT TIE THE RST_IN* LOW.
WE CAN SWITCH BACK TO SINGLE PART WHEN THE PART IS CHANGED.

SYNC_MASTER=REFERENCE_MLB — SYNC_DATE=12/03/2010

PAGE TITLE: SD CARD READER

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REVISION: 8.0.0
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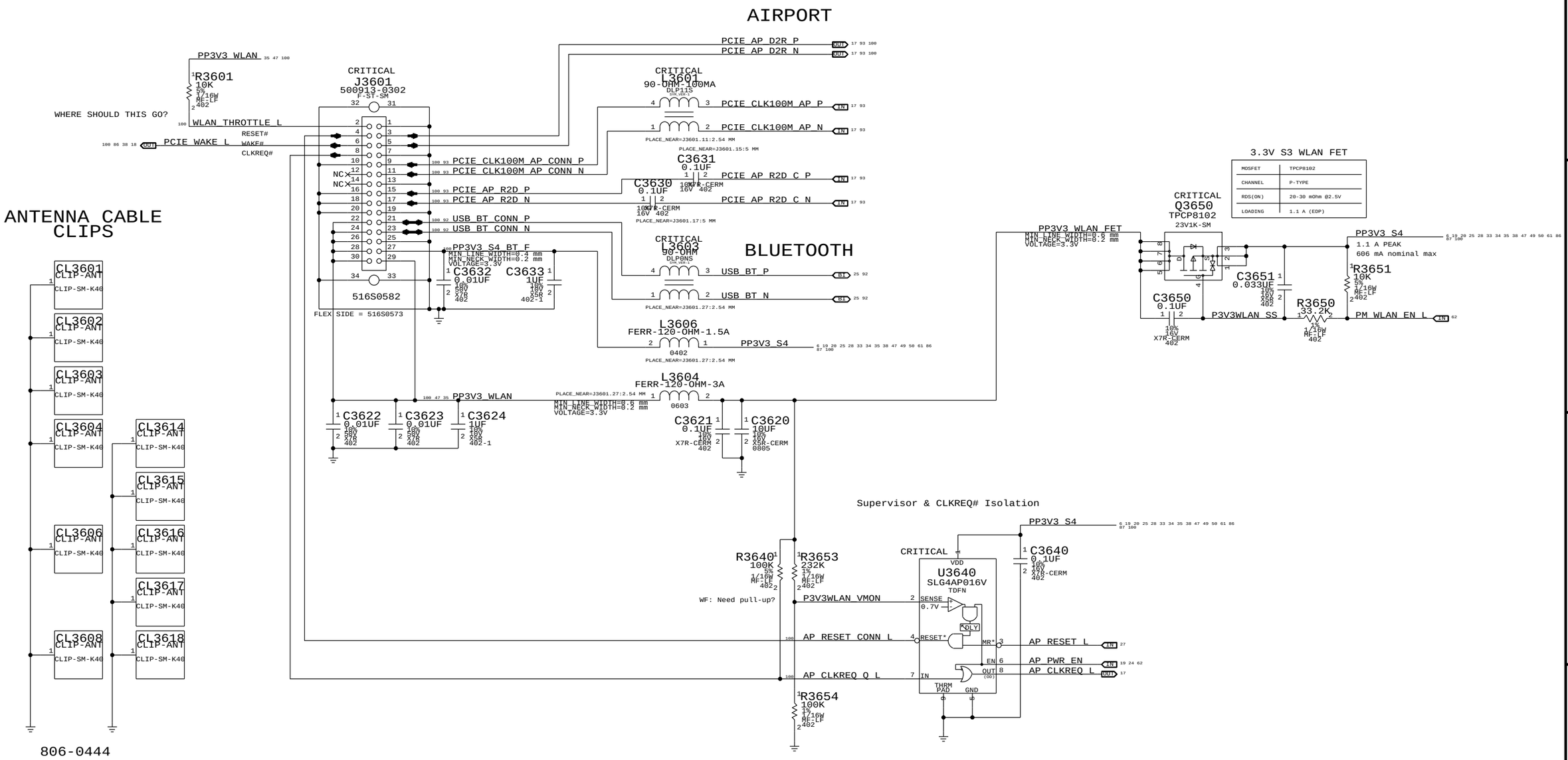

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE: WIRELESS,BT CONNECTOR

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REVISION: 8.0.0

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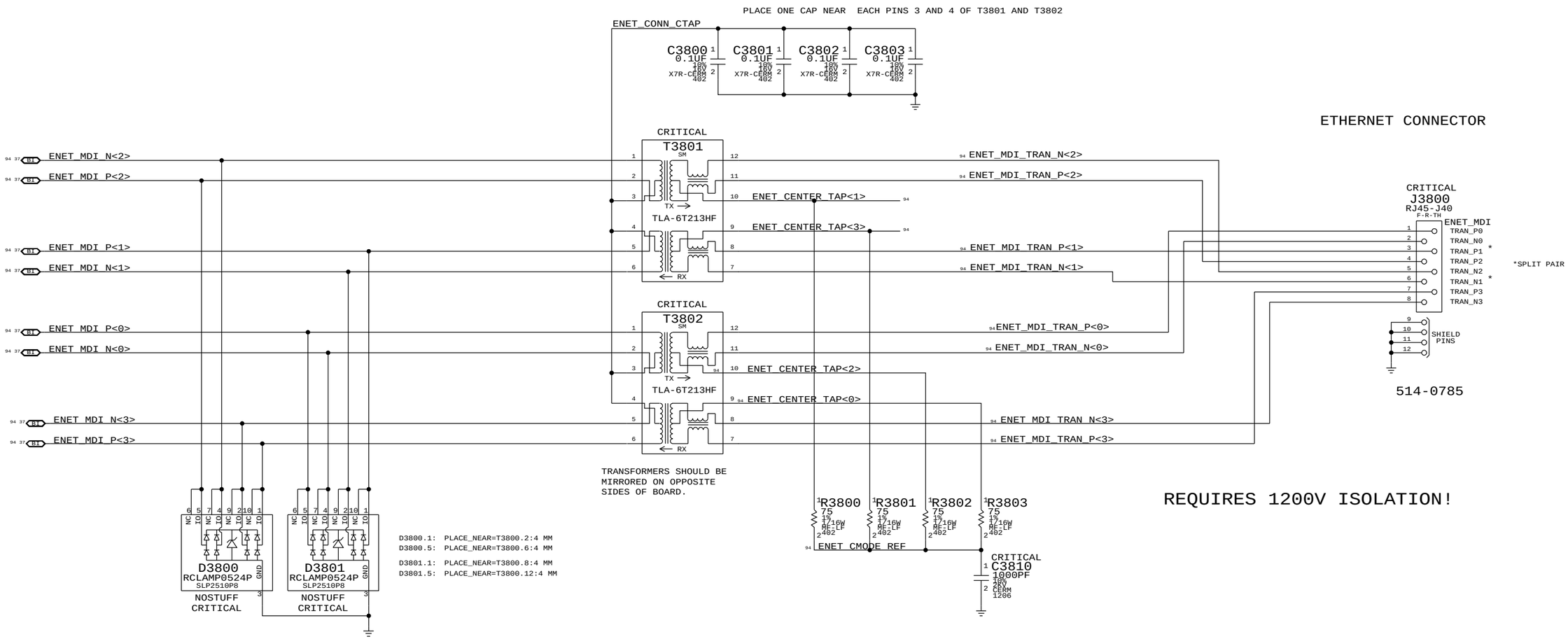

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PAGE TITLE
ETHERNET CONNECTOR

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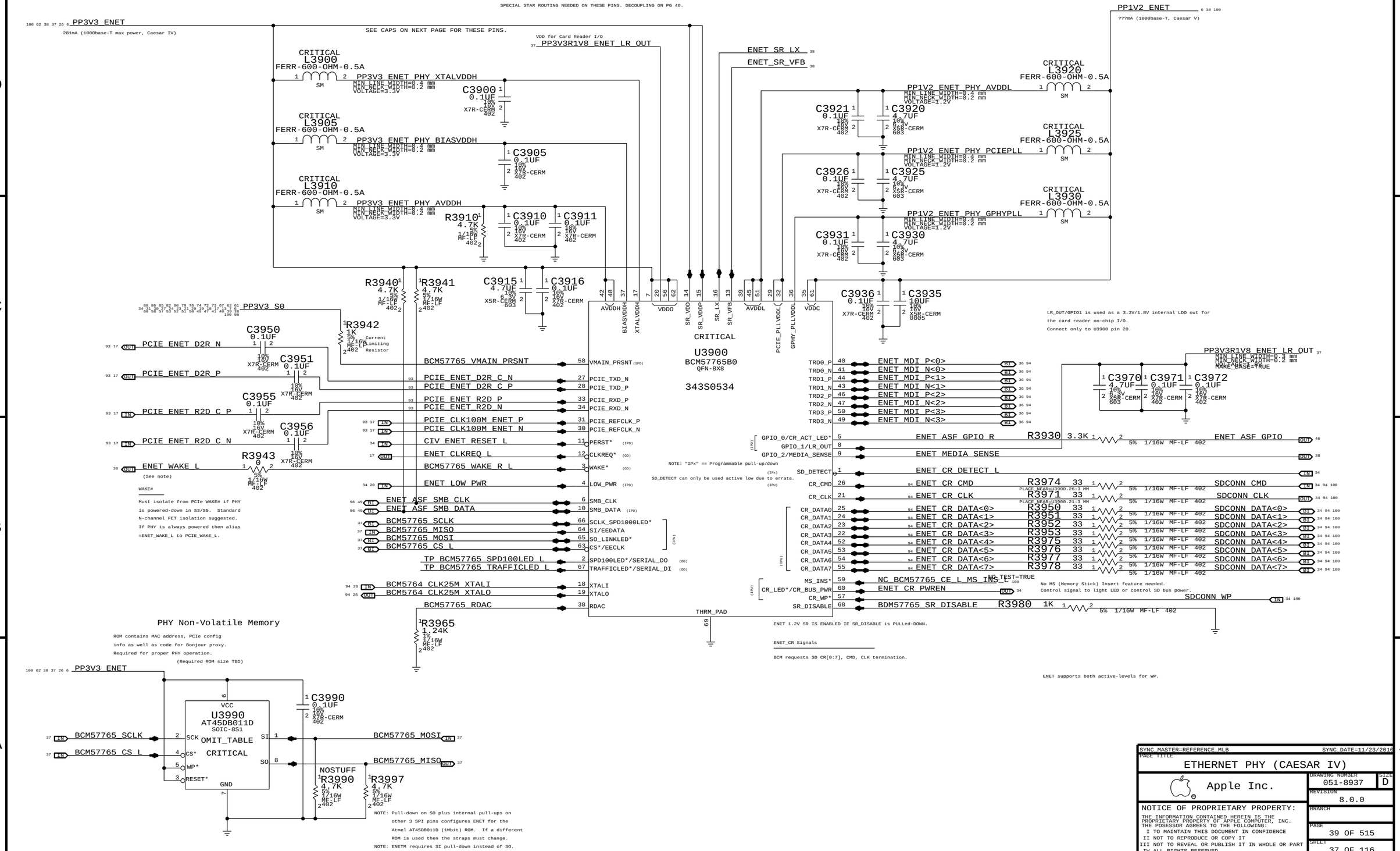
BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
IF ENABLED: SR_VDD/SR_VDDP CONNECT TO PP3V3_ENET (ADD BYPASSING), LX CONNECTS TO INDUCTOR.
SPECIAL STAR ROUTING NEEDED ON THESE PINS. DECOUPLING ON PG 40.



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PAGE TITLE
ETHERNET PHY (CAESAR IV)

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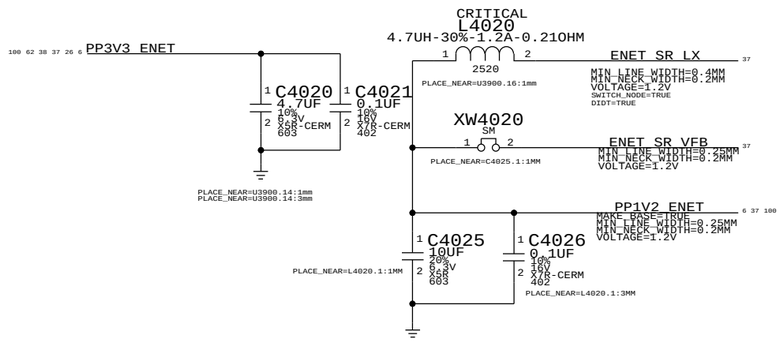
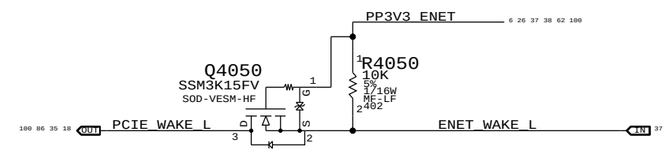
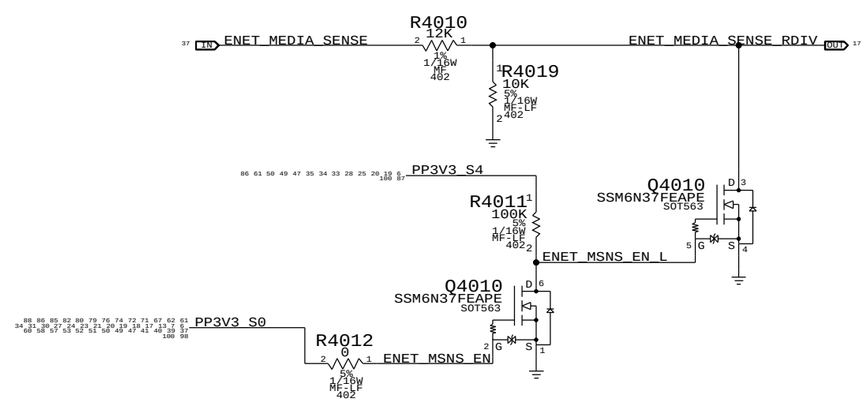
CAESAR IV 1.2V INT.VR CMPTS



Ethernet WAKE# Isolation





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PAGE TITLE

ETHERNET SUPPORT

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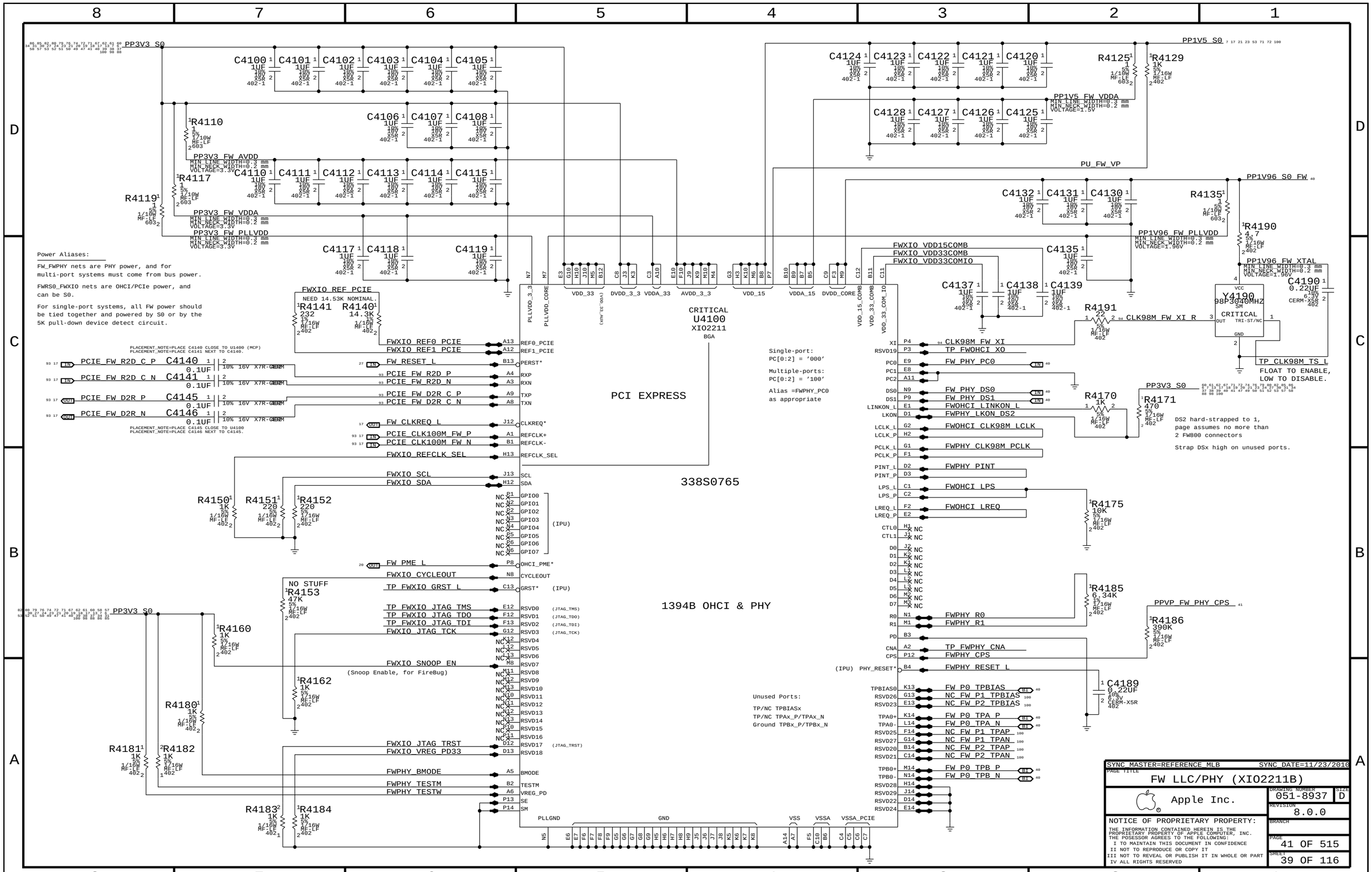
PP3V3_S0
PP1V5_S0
PP1V5_FW_VDDA
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
PU_FW_VP
PP1V96_S0_FW
PP1V96_FW_PLLVDD
VOLTAGE=1.96V
PP1V96_FW_XTAL
PP3V3_FW_AVDD
VOLTAGE=3.3V
PP3V3_FW_VDDA
PP3V3_FW_PLLVDD
Power Aliases:
FW_FWPHY nets are PHY power, and for multi-port systems must come from bus power.
FWRS0_FWXIO nets are OHCI/PCIe power, and can be S0.
For single-port systems, all FW power should be tied together and powered by S0 or by the 5K pull-down device detect circuit.
FWXIO_REF_PCIE
NEED 14.53K NOMINAL.
PLACEMENT_NOTE=PLACE C4140 CLOSE TO U1400 (MCP)
PLACEMENT_NOTE=PLACE C4141 NEXT TO C4140.
PLACEMENT_NOTE=PLACE C4145 CLOSE TO U4100
PLACEMENT_NOTE=PLACE C4146 NEXT TO C4145.
PCIE_FW_R2D_C_P
PCIE_FW_R2D_C_N
PCIE_FW_D2R_P
PCIE_FW_D2R_N
FW_RESET_L
FW_CLKREQ_L
PCIE_CLK100M_FW_P
PCIE_CLK100M_FW_N
FWXIO_REFCLK_SEL
FWXIO_SCL
FWXIO_SDA
FW_PME_L
FWXIO_CYCLEOUT
TP_FWXIO_GRST_L
TP_FWXIO_JTAG_TMS
TP_FWXIO_JTAG_TDO
TP_FWXIO_JTAG_TDI
FWXIO_JTAG_TCK
FWXIO_SNOOP_EN
(Snoop Enable, for FireBug)
FWXIO_JTAG_TRST
FWXIO_VREG_PD33
FWPHY_BMODE
FWPHY_TESTM
FWPHY_TESTW
NO STUFF
CRITICAL
U4100
XIO2211
BGA
PCI EXPRESS
338S0765
1394B OHCI & PHY
Single-port:
PC[0:2] = '000'
Multiple-ports:
PC[0:2] = '100'
Alias =FWPHY_PC0
as appropriate
Unused Ports:
TP/NC TPBIASx
TP/NC TPAx_P/TPAx_N
Ground TPBx_P/TPBx_N
FWXIO_VDD15COMB
FWXIO_VDD33COMB
FWXIO_VDD33COMIO
CLK98M_FW_XI
CLK98M_FW_XI_R
TP_FWOHCI_XO
FW_PHY_PC0
FW_PHY_DS0
FW_PHY_DS1
FWOHCI_LINKON_L
FWPHY_LKON_DS2
FWOHCI_CLK98M_LCLK
FWPHY_CLK98M_PCLK
FWPHY_PINT
FWOHCI_LPS
FWOHCI_LREQ
FWPHY_R0
FWPHY_R1
TP_FWPHY_CNA
FWPHY_CPS
FWPHY_RESET_L
FW_P0_TPBIAS
NC_FW_P1_TPBIAS
NC_FW_P2_TPBIAS
FW_P0_TPA_P
FW_P0_TPA_N
NC_FW_P1_TPAP
NC_FW_P1_TPAN
NC_FW_P2_TPAP
NC_FW_P2_TPAN
FW_P0_TPB_P
FW_P0_TPB_N
Y4190
98P3040MHZ
CRITICAL
TP_CLK98M_TS_L
FLOAT TO ENABLE, LOW TO DISABLE.
DS2 hard-strapped to 1, page assumes no more than 2 FW800 connectors
Strap DSx high on unused ports.
PPVP_FW_PHY_CPS
SYNC MASTER=REFERENCE_MLB
SYNC DATE=11/23/2010
PAGE TITLE
FW LLC/PHY (XIO2211B)
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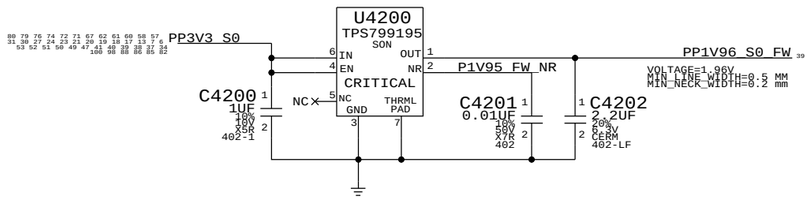
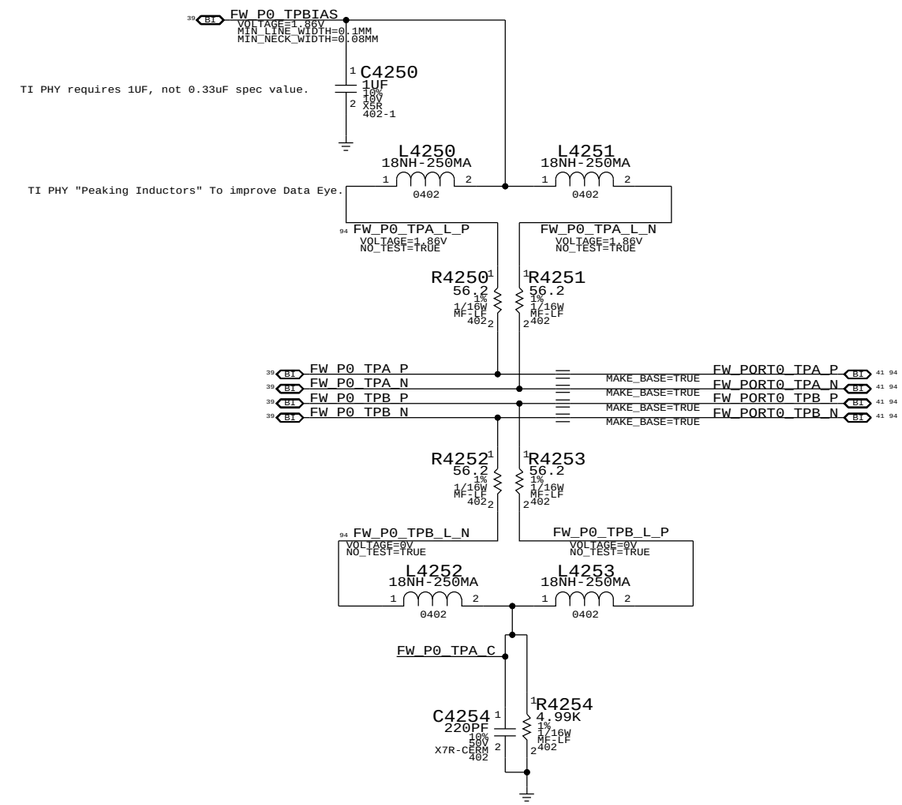
1394 PHY 1.95V SUPPLY

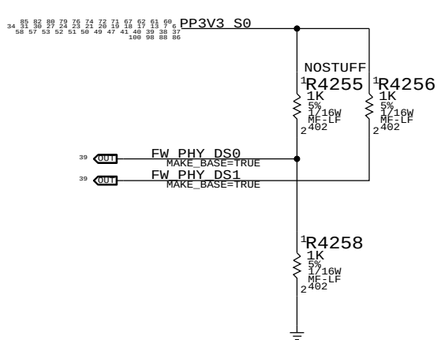


Termination

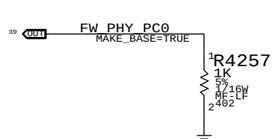
PLACE CLOSE TO FIREWIRE PHY (U4100)



1394 PHY STRAPPING OPTIONS



THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED.NO STUFF MEANS THAT IT IS IN BILINGUL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE.



THIS IS NOW ONE PORT ONLY AND HAVE POWER CODE "000"

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PAGE TITLE: FW: 1394B MISC

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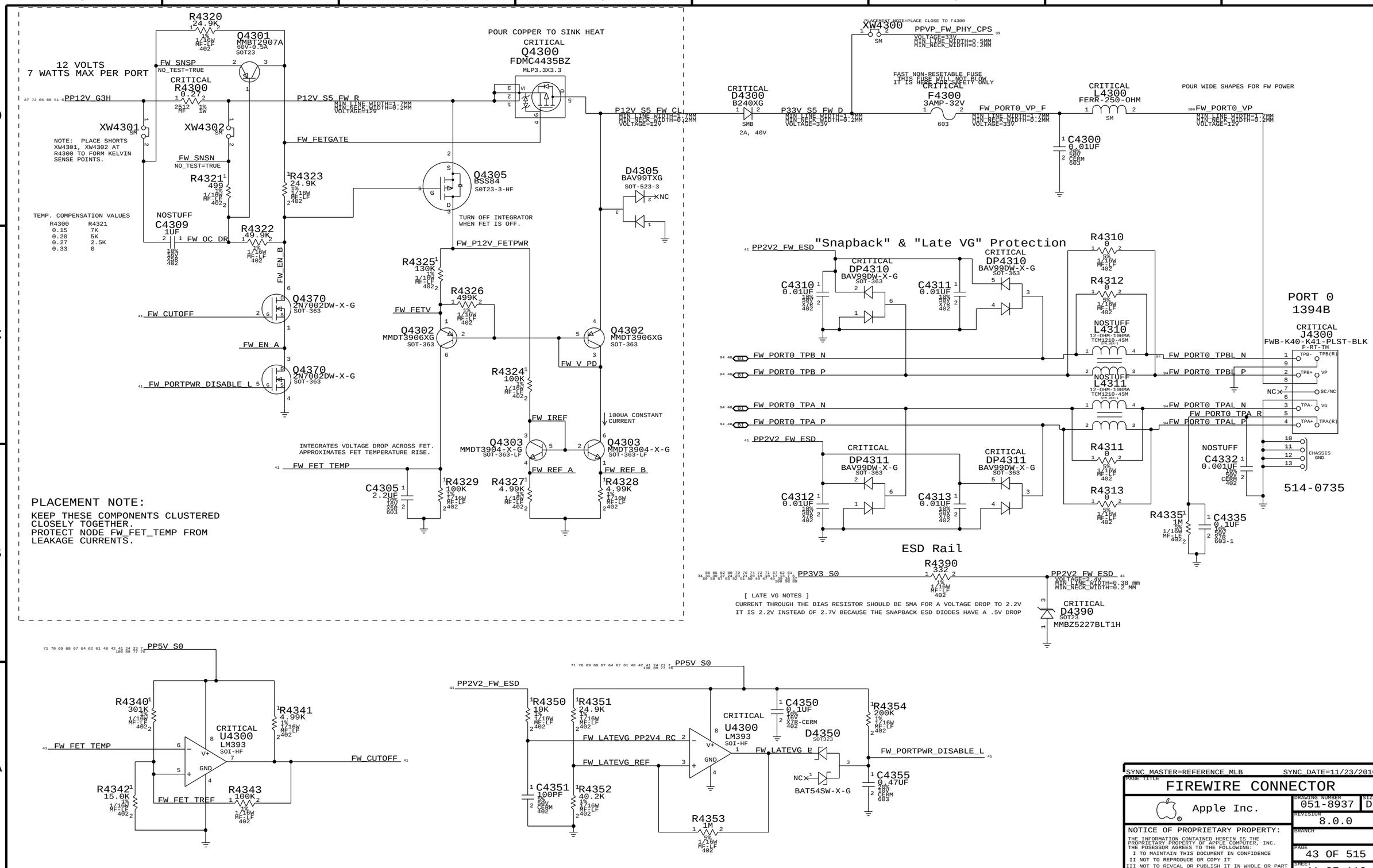

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PAGE TITLE

FIREWIRE CONNECTOR

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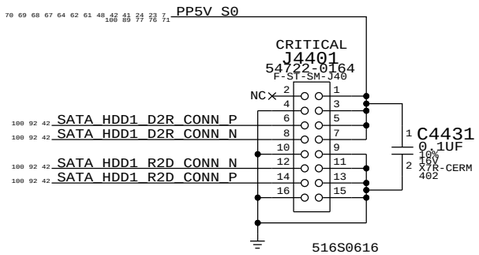
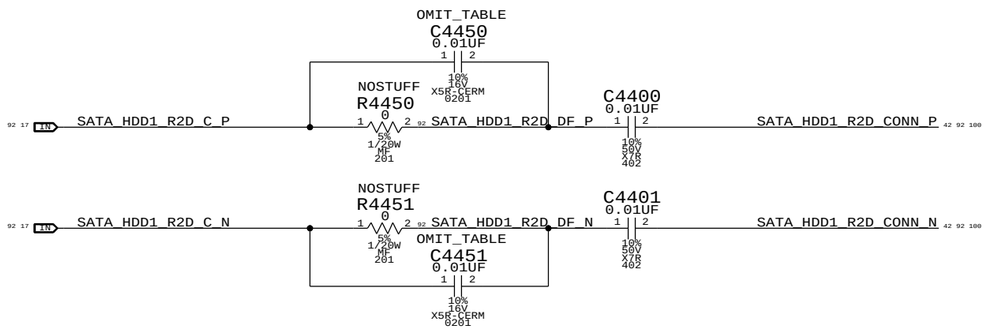
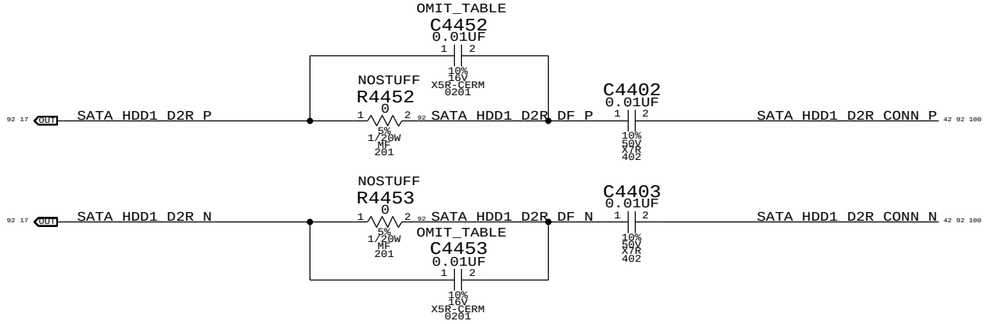
SATA CONNECTOR (HDD1)

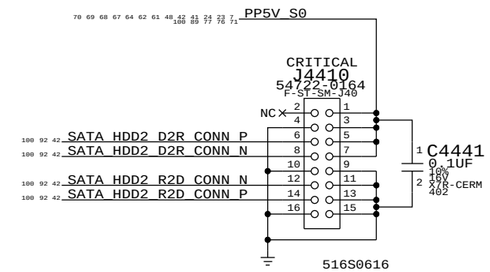


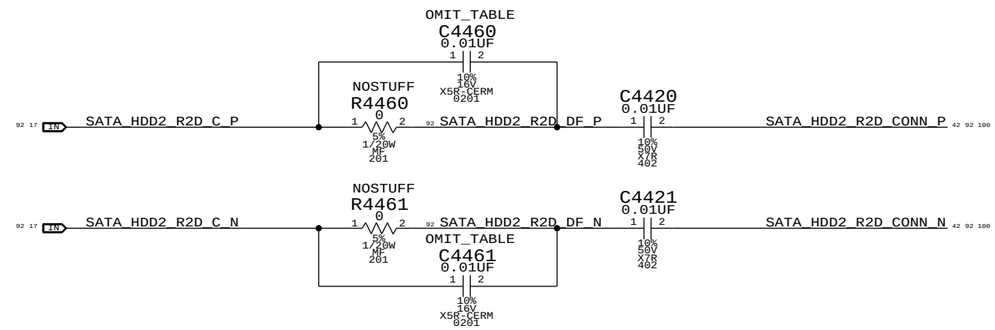


RESISTER ON CAP PADS!!

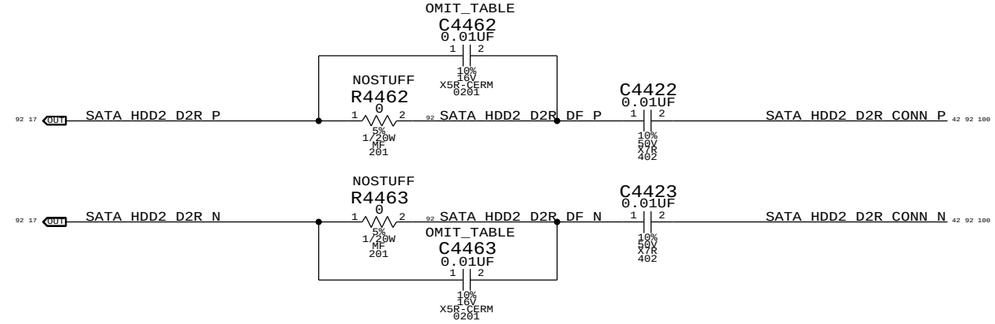


SATA CONNECTOR (HDD2)





RESISTER ON CAP PADS!!



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
117S0002	4	RES,ZERO OHM,0201	C4450,C4451,C4452,C4453	
117S0002	4	RES,ZERO OHM,0201	C4460,C4461,C4462,C4463	

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE
HDD SATA CONNECTORS

Apple Inc.

DRAWING NUMBER 051-8937 SIZE D

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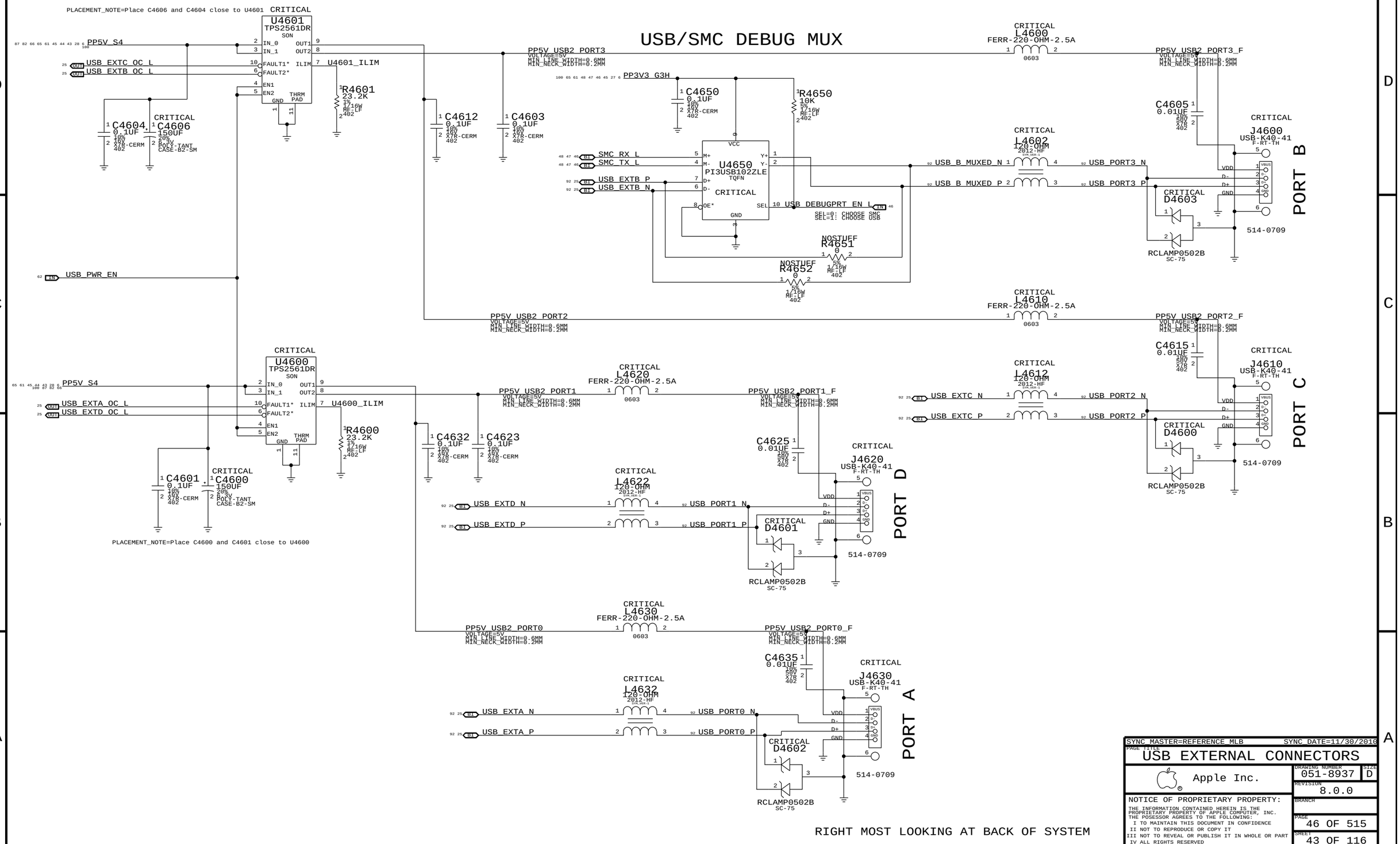
USB/SMC DEBUG MUX



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PAGE TITLE
USB EXTERNAL CONNECTORS

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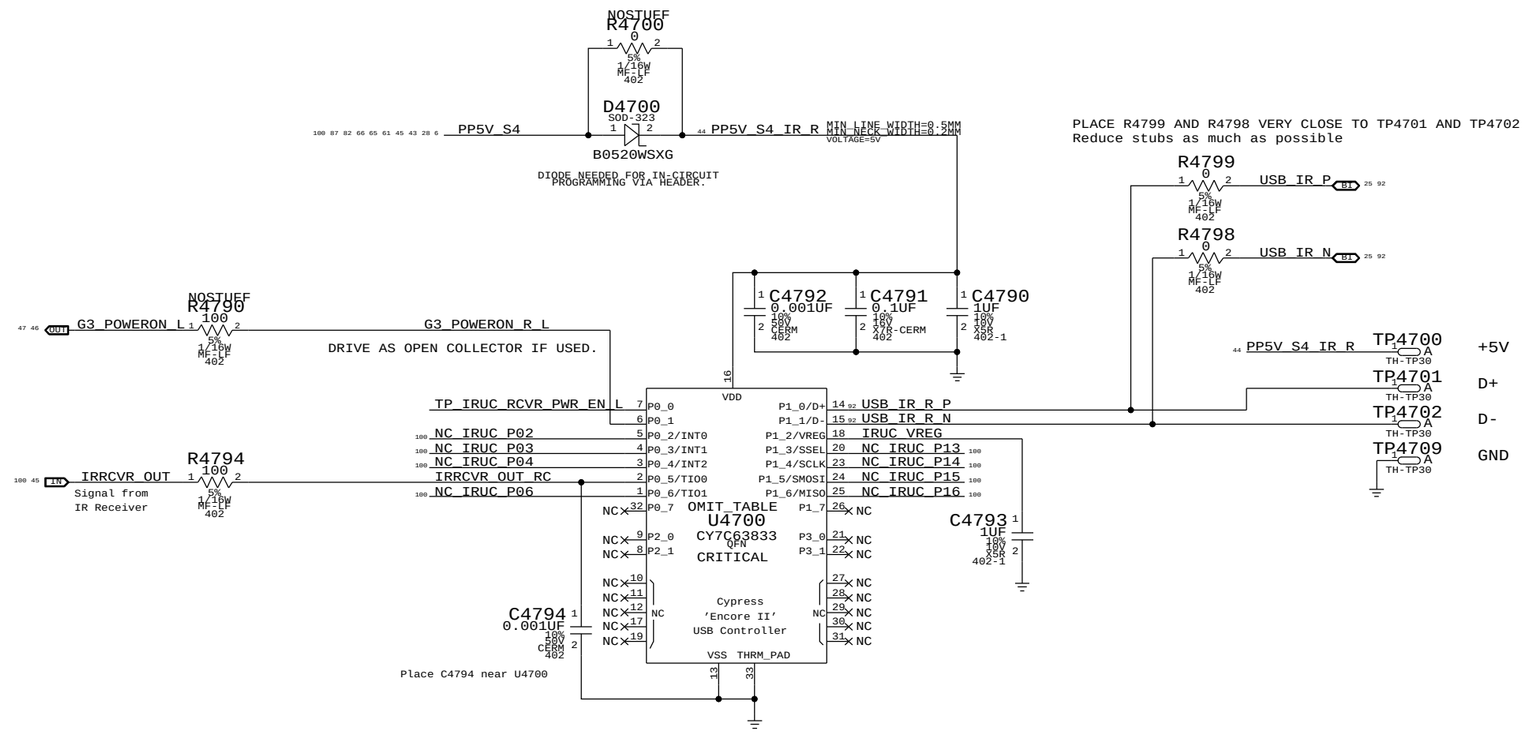
IR Controller



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PAGE TITLE

IR CONTROLLER

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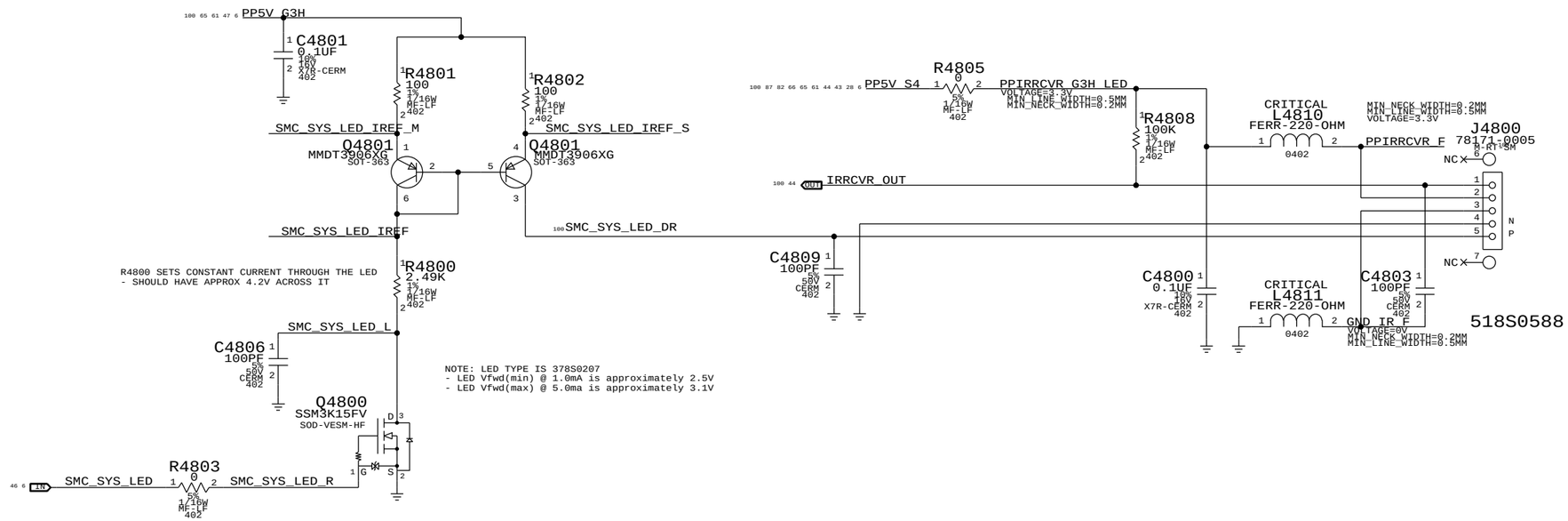
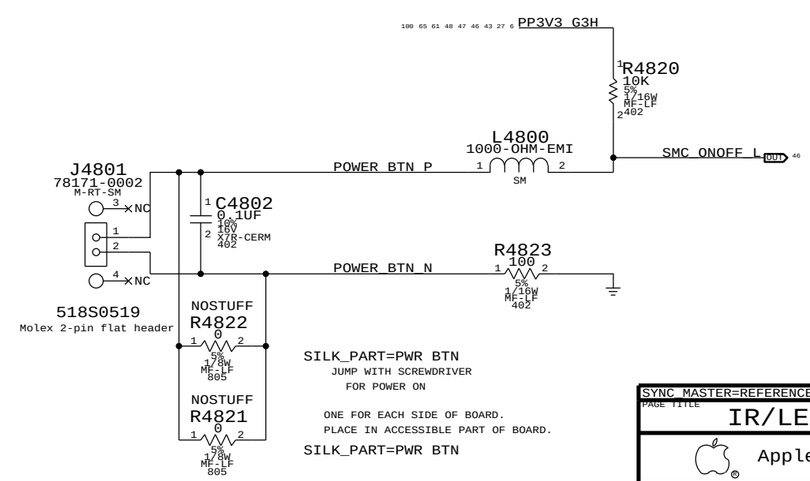
IR/LED BOARD CONNECTOR



SIL LED DRIVE CIRCUIT

Power Button Header



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PAGE TITLE

IR/LED, PWR BTTN

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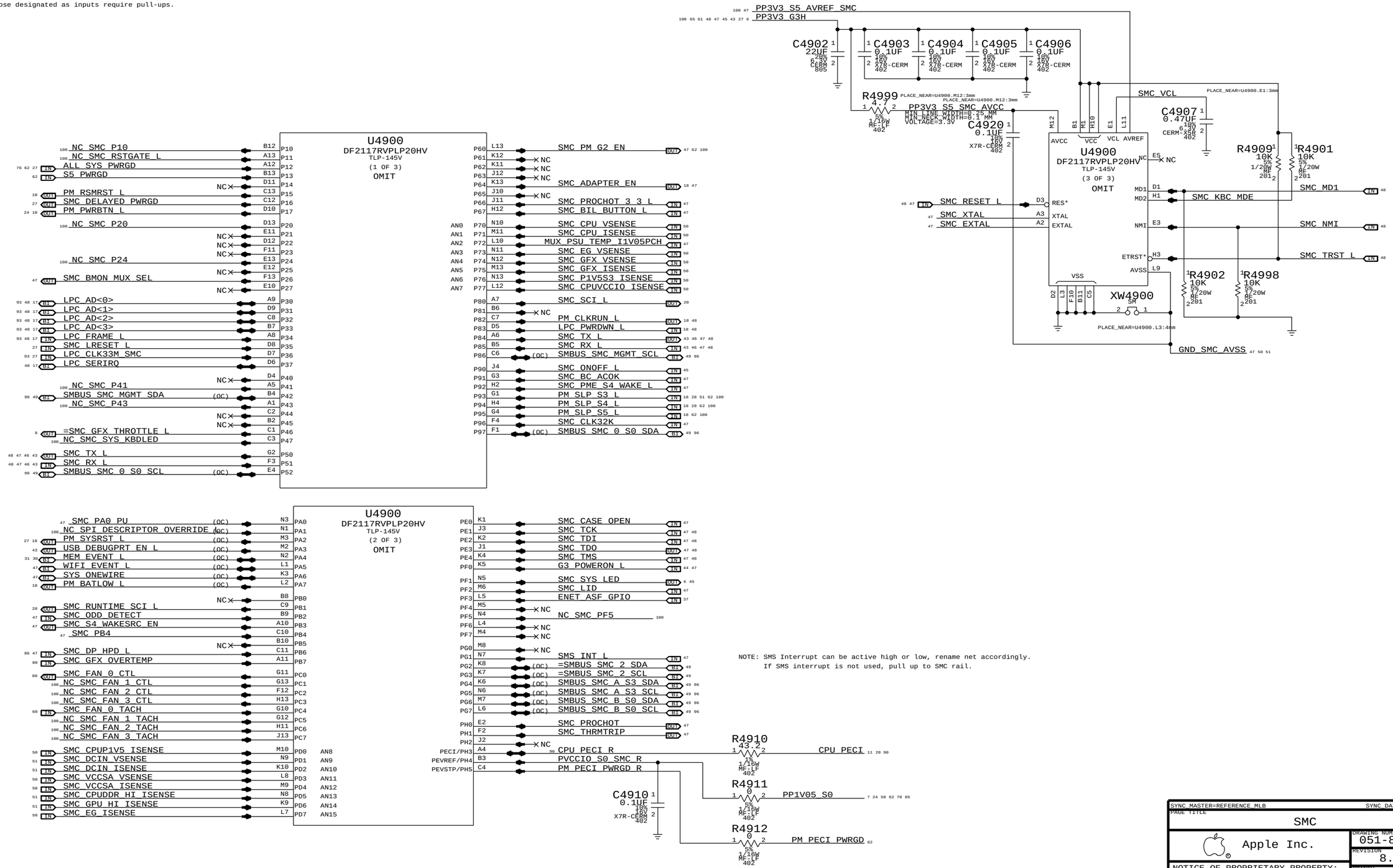
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=12/10/2010

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER: 051-8937 SIZE: D

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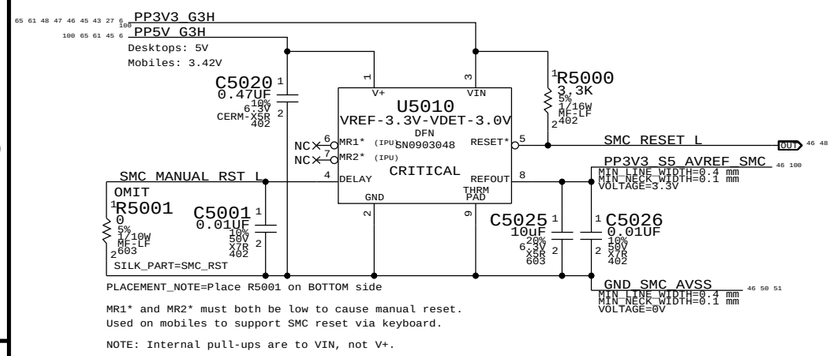
SMC Reset "Button", Supervisor & AVREF Supply

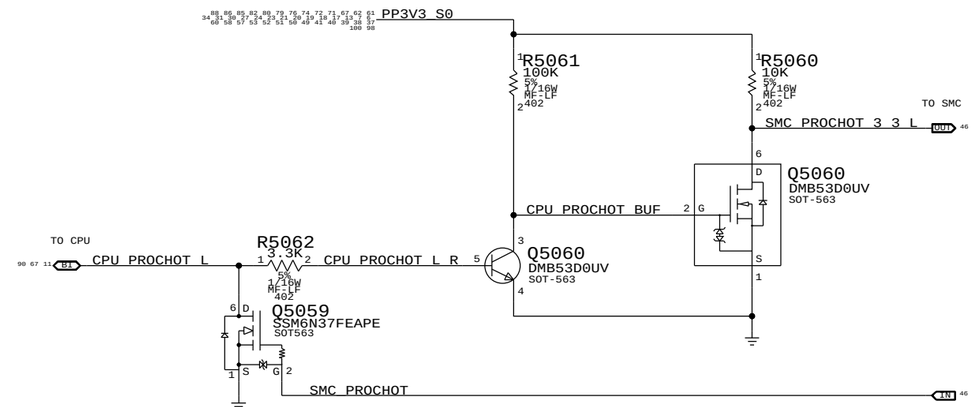


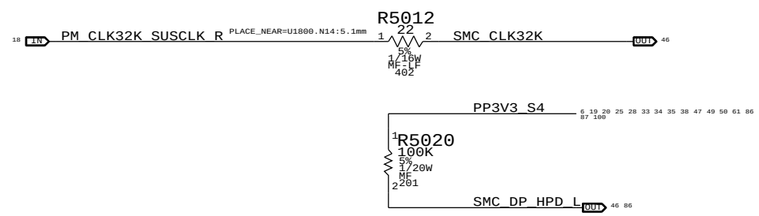
PLACEMENT_NOTE=Place R5001 on BOTTOM side

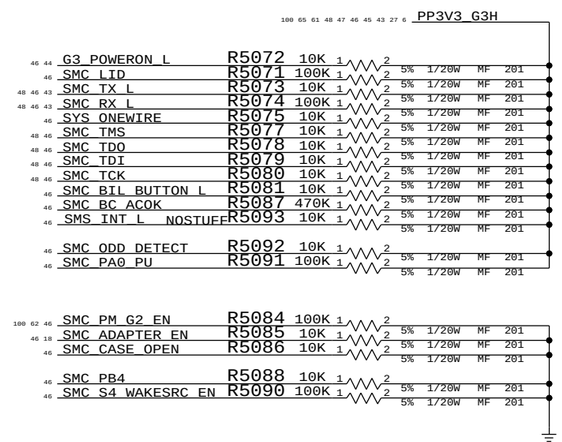
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

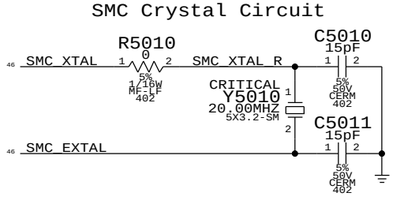
SMC FSB to 3.3V Level Shifting

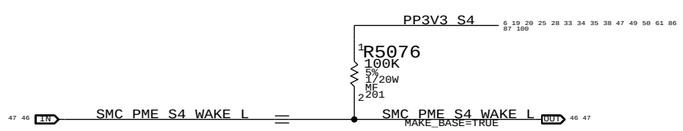


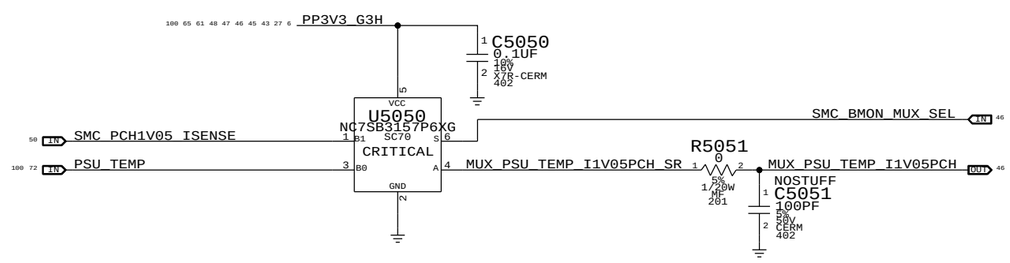




SMC Crystal Circuit







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PAGE TITLE: SMC Support

Apple Inc.

DRAWING NUMBER: 051-8937 SIZE: D

REVISION: 8.0.0

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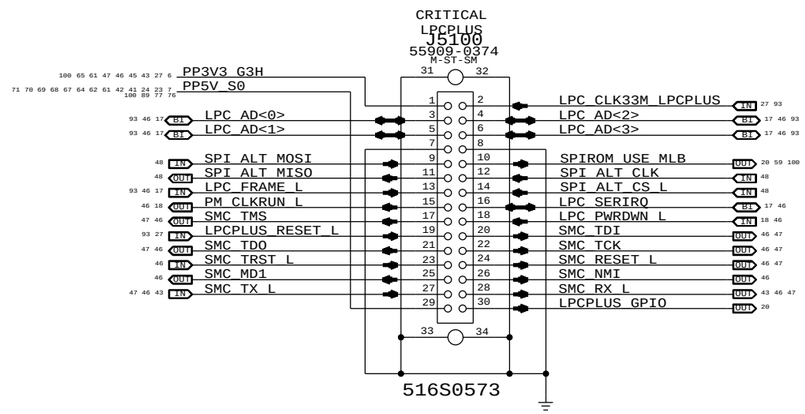
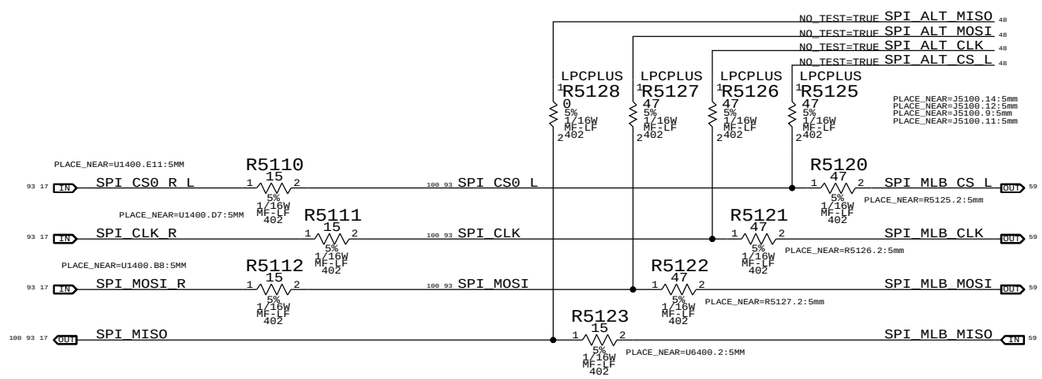
MATT CARD
LPC+SPI Connector



SPI Bus Series Termination



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PAGE TITLE
LPC+ Debug Connector

Apple Inc.

DRAWING NUMBER 051-8937 SIZE D

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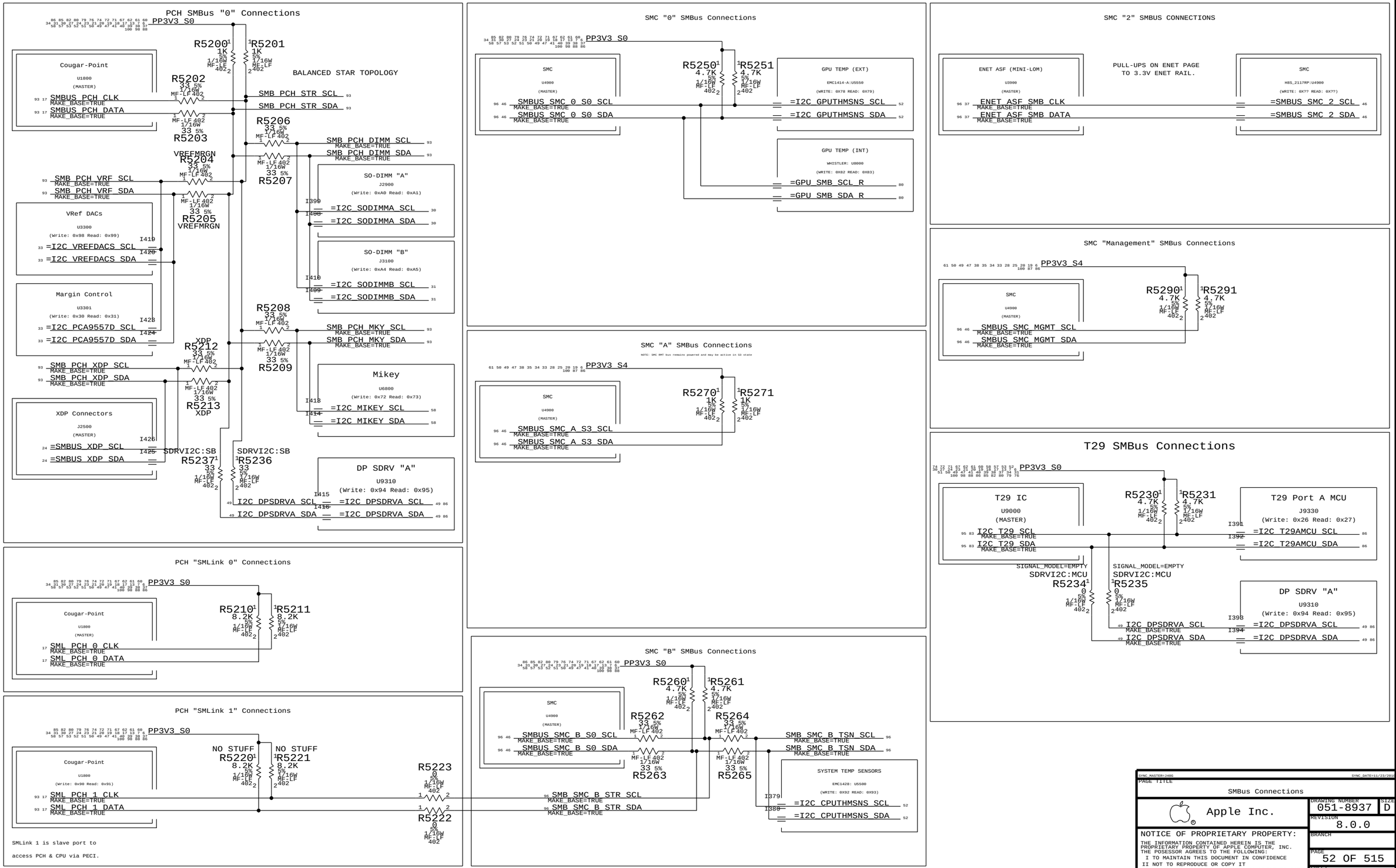
PCH SMBus "0" Connections
PP3V3_S0
R5200 1K 5% 1/16W MF-LF 402
R5201 1K 5% 1/16W MF-LF 402
BALANCED STAR TOPOLOGY
Cougar-Point U1800 (MASTER)
SMBUS_PCH_CLK MAKE_BASE=TRUE
SMBUS_PCH_DATA MAKE_BASE=TRUE
R5202 33 5% 1/16W MF-LF 402
R5203 33 5% 1/16W MF-LF 402
SMB_PCH_STR_SCL
SMB_PCH_STR_SDA
R5206 33 5% 1/16W MF-LF 402
R5207 33 5% 1/16W MF-LF 402
SMB_PCH_DIMM_SCL MAKE_BASE=TRUE
SMB_PCH_DIMM_SDA MAKE_BASE=TRUE
VREFMRGN
R5204 33 5% 1/16W MF-LF 402
SMB_PCH_VRF_SCL MAKE_BASE=TRUE
SMB_PCH_VRF_SDA MAKE_BASE=TRUE
R5205 33 5% 1/16W MF-LF 402
VREFMRGN
VRef DACs U3300 (Write: 0x98 Read: 0x99)
=I2C_VREFDACS_SCL
=I2C_VREFDACS_SDA
SO-DIMM "A" J2900 (Write: 0xA0 Read: 0xA1)
=I2C_SODIMMA_SCL
=I2C_SODIMMA_SDA
SO-DIMM "B" J3100 (Write: 0xA4 Read: 0xA5)
=I2C_SODIMMB_SCL
=I2C_SODIMMB_SDA
Margin Control U3301 (Write: 0x30 Read: 0x31)
=I2C_PCA9557D_SCL
=I2C_PCA9557D_SDA
R5208 33 5% 1/16W MF-LF 402
R5209 33 5% 1/16W MF-LF 402
SMB_PCH_MKY_SCL MAKE_BASE=TRUE
SMB_PCH_MKY_SDA MAKE_BASE=TRUE
XDP
R5212 33 5% 1/16W MF-LF 402
R5213 33 5% 1/16W MF-LF 402
XDP
SMB_PCH_XDP_SCL MAKE_BASE=TRUE
SMB_PCH_XDP_SDA MAKE_BASE=TRUE
Mikey U6800 (Write: 0x72 Read: 0x73)
=I2C_MIKEY_SCL
=I2C_MIKEY_SDA
XDP Connectors J2500 (MASTER)
=SMBUS_XDP_SCL
=SMBUS_XDP_SDA
SDRVI2C:SB
R5237 33 5% 1/16W MF-LF 402
R5236 33 5% 1/16W MF-LF 402
SDRVI2C:SB
DP SDRV "A" U9310 (Write: 0x94 Read: 0x95)
=I2C_DPSDRVA_SCL
=I2C_DPSDRVA_SDA
SMC "0" SMBus Connections
PP3V3_S0
SMC U4900 (MASTER)
SMBUS_SMC_0_S0_SCL MAKE_BASE=TRUE
SMBUS_SMC_0_S0_SDA MAKE_BASE=TRUE
R5250 4.7K 5% 1/16W MF-LF 402
R5251 4.7K 5% 1/16W MF-LF 402
GPU TEMP (EXT) EMC1414-A:U5550 (WRITE: 0X78 READ: 0X79)
=I2C_GPUTHMSNS_SCL
=I2C_GPUTHMSNS_SDA
GPU TEMP (INT) WHISTLER: U8000 (WRITE: 0X82 READ: 0X83)
=GPU_SMB_SCL_R
=GPU_SMB_SDA_R
SMC "2" SMBUS CONNECTIONS
ENET ASF (MINI-LOM) U3900 (MASTER)
ENET_ASF_SMB_CLK MAKE_BASE=TRUE
ENET_ASF_SMB_DATA MAKE_BASE=TRUE
PULL-UPS ON ENET PAGE TO 3.3V ENET RAIL.
SMC H8S_2117RP:U4900 (WRITE: 0X?? READ: 0X??)
=SMBUS_SMC_2_SCL
=SMBUS_SMC_2_SDA
SMC "Management" SMBus Connections
PP3V3_S4
SMC U4900 (MASTER)
SMBUS_SMC_MGMT_SCL MAKE_BASE=TRUE
SMBUS_SMC_MGMT_SDA MAKE_BASE=TRUE
R5290 4.7K 5% 1/16W MF-LF 402
R5291 4.7K 5% 1/16W MF-LF 402
SMC "A" SMBus Connections
NOTE: SMC RMT bus remains powered and may be active in S3 state
PP3V3_S4
SMC U4900 (MASTER)
SMBUS_SMC_A_S3_SCL MAKE_BASE=TRUE
SMBUS_SMC_A_S3_SDA MAKE_BASE=TRUE
R5270 1K 5% 1/16W MF-LF 402
R5271 1K 5% 1/16W MF-LF 402
T29 SMBus Connections
PP3V3_S0
T29 IC U9000 (MASTER)
I2C_T29_SCL MAKE_BASE=TRUE
I2C_T29_SDA MAKE_BASE=TRUE
R5230 4.7K 5% 1/16W MF-LF 402
R5231 4.7K 5% 1/16W MF-LF 402
T29 Port A MCU J9330 (Write: 0x26 Read: 0x27)
=I2C_T29AMCU_SCL
=I2C_T29AMCU_SDA
SIGNAL_MODEL=EMPTY
SDRVI2C:MCU
R5234 0 5% 1/16W MF-LF 402
R5235 0 5% 1/16W MF-LF 402
DP SDRV "A" U9310 (Write: 0x94 Read: 0x95)
I2C_DPSDRVA_SCL MAKE_BASE=TRUE
I2C_DPSDRVA_SDA MAKE_BASE=TRUE
=I2C_DPSDRVA_SCL
=I2C_DPSDRVA_SDA
PCH "SMLink 0" Connections
PP3V3_S0
Cougar-Point U1800 (MASTER)
SML_PCH_0_CLK MAKE_BASE=TRUE
SML_PCH_0_DATA MAKE_BASE=TRUE
R5210 8.2K 5% 1/16W MF-LF 402
R5211 8.2K 5% 1/16W MF-LF 402
PCH "SMLink 1" Connections
PP3V3_S0
Cougar-Point U1800 (Write: 0x90 Read: 0x91)
SML_PCH_1_CLK MAKE_BASE=TRUE
SML_PCH_1_DATA MAKE_BASE=TRUE
NO STUFF
R5220 8.2K 5% 1/16W MF-LF 402
NO STUFF
R5221 8.2K 5% 1/16W MF-LF 402
R5223 0 5% 1/16W MF-LF 402
R5222 0 5% 1/16W MF-LF 402
SMB_SMC_B_STR_SCL MAKE_BASE=TRUE
SMB_SMC_B_STR_SDA MAKE_BASE=TRUE
SMLink 1 is slave port to
access PCH & CPU via PECI.
SMC "B" SMBus Connections
PP3V3_S0
SMC U4900 (MASTER)
SMBUS_SMC_B_S0_SCL MAKE_BASE=TRUE
SMBUS_SMC_B_S0_SDA MAKE_BASE=TRUE
R5260 4.7K 5% 1/16W MF-LF 402
R5261 4.7K 5% 1/16W MF-LF 402
R5262 33 5% 1/16W MF-LF 402
R5263 33 5% 1/16W MF-LF 402
R5264 33 5% 1/16W MF-LF 402
R5265 33 5% 1/16W MF-LF 402
SMB_SMC_B_TSN_SCL MAKE_BASE=TRUE
SMB_SMC_B_TSN_SDA MAKE_BASE=TRUE
SYSTEM TEMP SENSORS EMC1428: U5500 (WRITE: 0X92 READ: 0X93)
=I2C_CPUTHMSNS_SCL
=I2C_CPUTHMSNS_SDA
SYNC_MASTER=J40G
SYNC_DATE=11/23/201
PAGE TITLE
SMBus Connections
Apple Inc.
DRAWING NUMBER 051-8937
SIZE D
REVISION 8.0.0
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PAGE 52 OF 515
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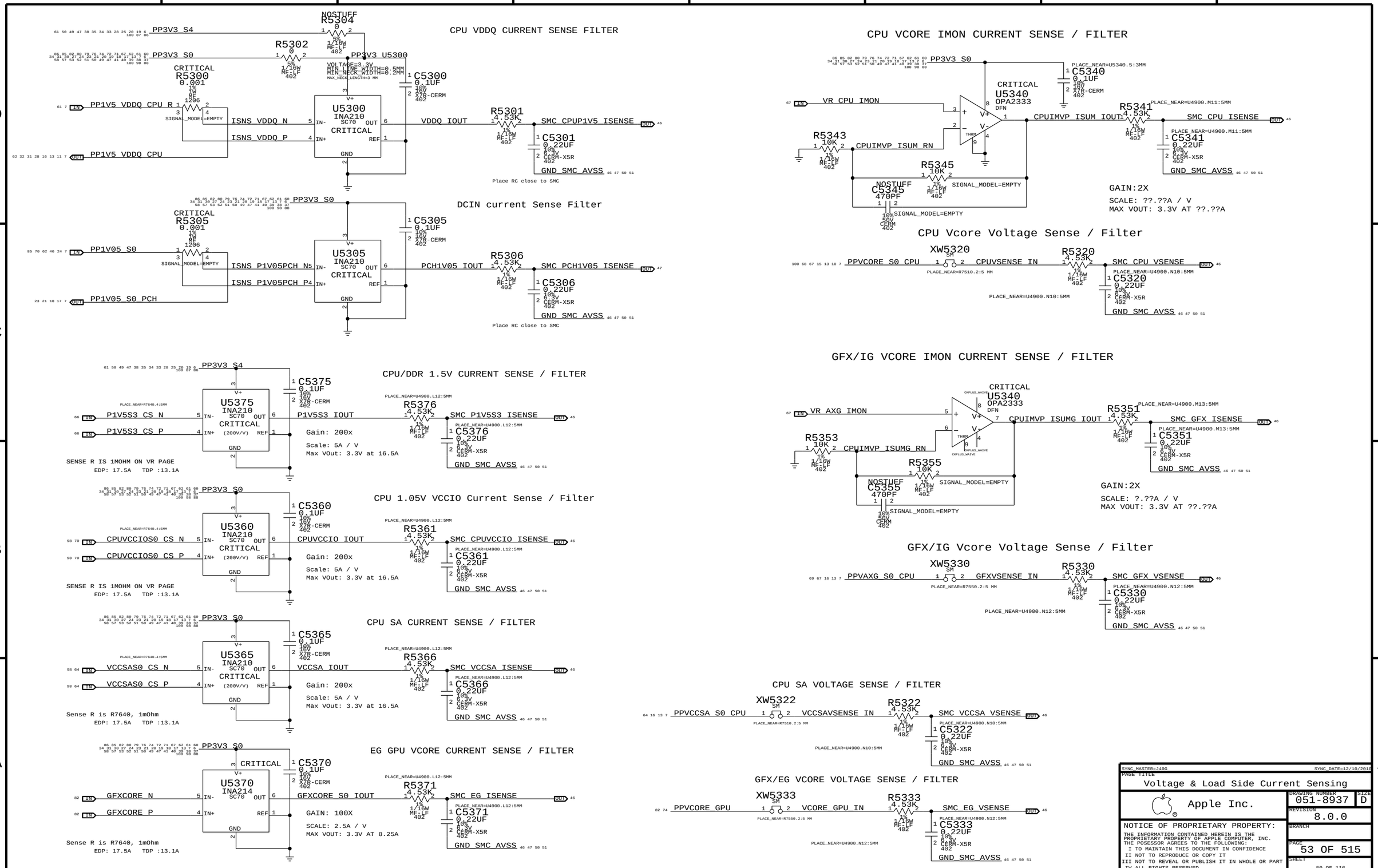
CPU VDDQ CURRENT SENSE FILTER
PP3V3_S4
PP3V3_S0
NOSTUFF R5304 0 5% 1/16W MF-LF 402
R5302 0 5% 1/16W MF-LF 402
PP3V3_U5300
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
MAX_NECK_LENGTH=3 MM
CRITICAL R5300 0.001 1% 1W MF 1206
PP1V5_VDDQ_CPU_R
SIGNAL_MODEL=EMPTY
ISNS_VDDQ_N
ISNS_VDDQ_P
PP1V5_VDDQ_CPU
U5300 INA210 SC70 CRITICAL
VDDQ_IOUT
C5300 0.1UF 10% 16V X7R-CERM 402
R5301 4.53K 1% 1/16W MF-LF 402
SMC_CPUP1V5_ISENSE
C5301 0.22UF 10% 6.3V CERM-X5R 402
GND_SMC_AVSS
Place RC close to SMC
DCIN current Sense Filter
PP3V3_S0
CRITICAL R5305 0.001 1% 1W MF 1206
PP1V05_S0
ISNS_P1V05PCH_N
ISNS_P1V05PCH_P
PP1V05_S0_PCH
U5305 INA210 SC70 CRITICAL
PCH1V05_IOUT
C5305 0.1UF 10% 16V X7R-CERM 402
R5306 4.53K 1% 1/16W MF-LF 402
SMC_PCH1V05_ISENSE
C5306 0.22UF 10% 6.3V CERM-X5R 402
GND_SMC_AVSS
Place RC close to SMC
CPU/DDR 1.5V CURRENT SENSE / FILTER
PP3V3_S4
C5375 0.1UF 10% 16V X7R-CERM 402
U5375 INA210 SC70 CRITICAL (200V/V)
P1V5S3_CS_N
P1V5S3_CS_P
P1V5S3_IOUT
R5376 4.53K 1% 1/16W MF-LF 402
SMC_P1V5S3_ISENSE
C5376 0.22UF 10% 6.3V CERM-X5R 402
GND_SMC_AVSS
Gain: 200x
Scale: 5A / V
Max VOut: 3.3V at 16.5A
SENSE R IS 1MOHM ON VR PAGE
EDP: 17.5A TDP :13.1A
CPU 1.05V VCCIO Current Sense / Filter
PP3V3_S0
C5360 0.1UF 10% 16V X7R-CERM 402
U5360 INA210 SC70 CRITICAL (200V/V)
CPUVCCIOS0_CS_N
CPUVCCIOS0_CS_P
CPUVCCIO_IOUT
R5361 4.53K 1% 1/16W MF-LF 402
SMC_CPUVCCIO_ISENSE
C5361 0.22UF 10% 6.3V CERM-X5R 402
GND_SMC_AVSS
Gain: 200x
Scale: 5A / V
Max VOut: 3.3V at 16.5A
SENSE R IS 1MOHM ON VR PAGE
EDP: 17.5A TDP :13.1A
CPU SA CURRENT SENSE / FILTER
PP3V3_S0
C5365 0.1UF 10% 16V X7R-CERM 402
U5365 INA210 SC70 CRITICAL (200V/V)
VCCSAS0_CS_N
VCCSAS0_CS_P
VCCSA_IOUT
R5366 4.53K 1% 1/16W MF-LF 402
SMC_VCCSA_ISENSE
C5366 0.22UF 10% 6.3V CERM-X5R 402
GND_SMC_AVSS
Gain: 200x
Scale: 5A / V
Max VOut: 3.3V at 16.5A
Sense R is R7640, 1mOhm
EDP: 17.5A TDP :13.1A
EG GPU VCORE CURRENT SENSE / FILTER
PP3V3_S0
CRITICAL
C5370 0.1UF 10% 16V X7R-CERM 402
U5370 INA214 SC70
GFXCORE_N
GFXCORE_P
GFXCORE_S0_IOUT
R5371 4.53K 1% 1/16W MF-LF 402
SMC_EG_ISENSE
C5371 0.22UF 10% 6.3V CERM-X5R 402
GND_SMC_AVSS
GAIN: 100X
SCALE: 2.5A / V
MAX VOUT: 3.3V AT 8.25A
Sense R is R7640, 1mOhm
EDP: 17.5A TDP :13.1A
CPU VCORE IMON CURRENT SENSE / FILTER
PP3V3_S0
PLACE_NEAR=U5340.5:3MM
C5340 0.1UF 10% 16V X7R-CERM 402
CRITICAL U5340 OPA2333 DFN
VR_CPU_IMON
CPUIMVP_ISUM_IOUT
R5341 4.53K 1% 1/16W MF-LF 402
PLACE_NEAR=U4900.M11:5MM
SMC_CPU_ISENSE
PLACE_NEAR=U4900.M11:5MM
C5341 0.22UF 10% 6.3V CERM-X5R 402
GND_SMC_AVSS
R5343 10K 1% 1/16W MF-LF 402
CPUIMVP_ISUM_RN
R5345 10K 1% 1/16W MF-LF 402
SIGNAL_MODEL=EMPTY
NOSTUFF C5345 470PF 10% 50V CERM 402
SIGNAL_MODEL=EMPTY
GAIN:2X
SCALE: ??.??A / V
MAX VOUT: 3.3V AT ??.??A
CPU Vcore Voltage Sense / Filter
XW5320 SM
PPVCORE_S0_CPU
PLACE_NEAR=R7510.2:5 MM
CPUVSENSE_IN
R5320 4.53K 1% 1/16W MF-LF 402
SMC_CPU_VSENSE
PLACE_NEAR=U4900.N10:5MM
C5320 0.22UF 10% 6.3V CERM-X5R 402
GND_SMC_AVSS
PLACE_NEAR=U4900.N10:5MM
GFX/IG VCORE IMON CURRENT SENSE / FILTER
CRITICAL U5340 OPA2333 DFN
VR_AXG_IMON
CPUIMVP_ISUMG_IOUT
R5351 4.53K 1% 1/16W MF-LF 402
PLACE_NEAR=U4900.M13:5MM
SMC_GFX_ISENSE
PLACE_NEAR=U4900.M13:5MM
C5351 0.22UF 10% 6.3V CERM-X5R 402
GND_SMC_AVSS
R5353 10K 1% 1/16W MF-LF 402
CPUIMVP_ISUMG_RN
R5355 10K 1% 1/16W MF-LF 402
SIGNAL_MODEL=EMPTY
NOSTUFF C5355 470PF 10% 50V CERM 402
SIGNAL_MODEL=EMPTY
GAIN:2X
SCALE: ?.??A / V
MAX VOUT: 3.3V AT ??.??A
GFX/IG Vcore Voltage Sense / Filter
XW5330 SM
PPVAXG_S0_CPU
PLACE_NEAR=R7550.2:5 MM
GFXVSENSE_IN
R5330 4.53K 1% 1/16W MF-LF 402
SMC_GFX_VSENSE
PLACE_NEAR=U4900.N12:5MM
C5330 0.22UF 10% 6.3V CERM-X5R 402
GND_SMC_AVSS
PLACE_NEAR=U4900.N12:5MM
CPU SA VOLTAGE SENSE / FILTER
XW5322 SM
PPVCCSA_S0_CPU
PLACE_NEAR=R7510.2:5 MM
VCCSAVSENSE_IN
R5322 4.53K 1% 1/16W MF-LF 402
SMC_VCCSA_VSENSE
PLACE_NEAR=U4900.N10:5MM
C5322 0.22UF 10% 6.3V CERM-X5R 402
GND_SMC_AVSS
PLACE_NEAR=U4900.N10:5MM
GFX/EG VCORE VOLTAGE SENSE / FILTER
XW5333 SM
PPVCORE_GPU
PLACE_NEAR=R7550.2:5 MM
VCORE_GPU_IN
R5333 4.53K 1% 1/16W MF-LF 402
SMC_EG_VSENSE
PLACE_NEAR=U4900.N12:5MM
C5333 0.22UF 10% 6.3V CERM-X5R 402
GND_SMC_AVSS
PLACE_NEAR=U4900.N12:5MM
SYNC_MASTER=J40G
SYNC_DATE=12/10/2010
PAGE TITLE
Voltage & Load Side Current Sensing
Apple Inc.
DRAWING NUMBER 051-8937
SIZE D
REVISION 8.0.0
BRANCH
PAGE 53 OF 515
SHEET 50 OF 116
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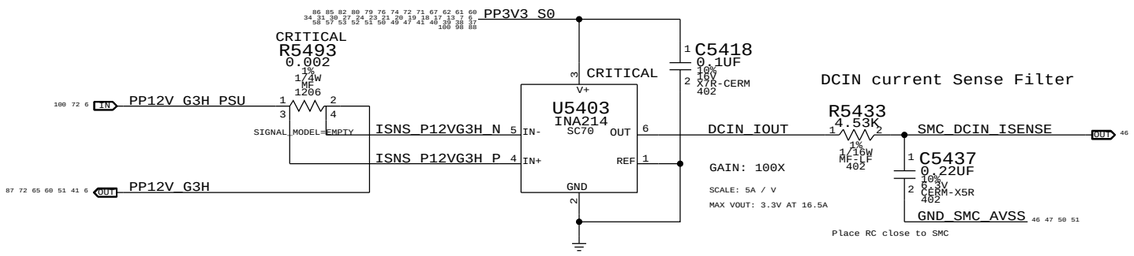
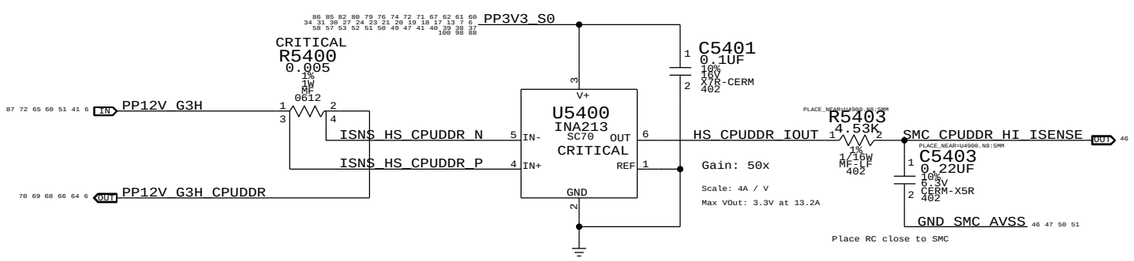
J40I, J40S, AND J40

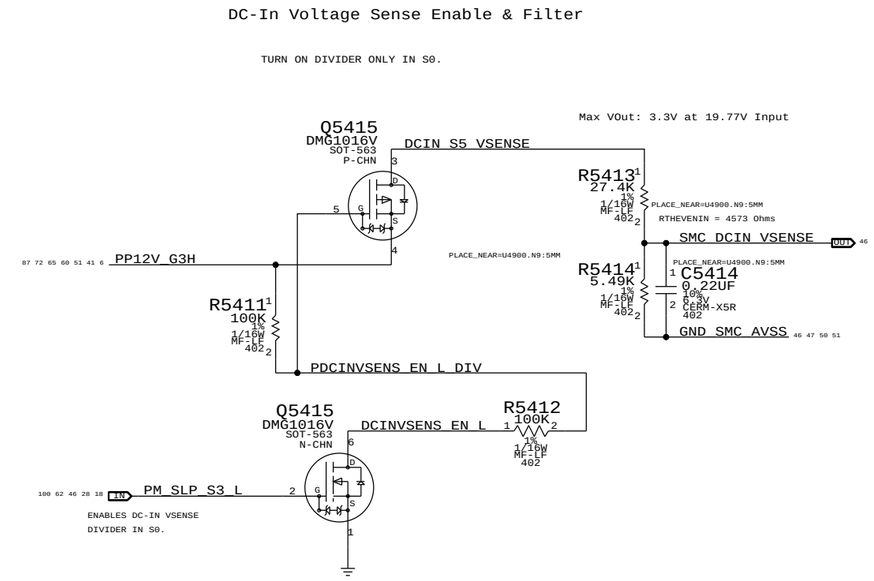
PSU CURRENT SENSE



CPU / DDR HIGH SIDE CURRENT SENSE / FILTER

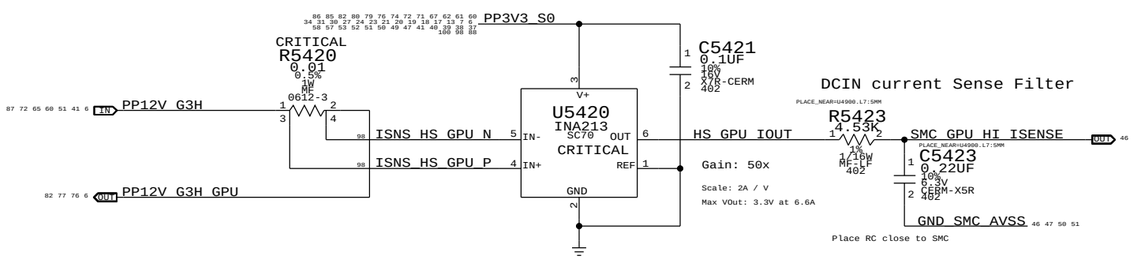


DC-In Voltage Sense Enable & Filter



J40G ONLY

EXTERNAL GPU HIGH SIDE CURRENT SENSE / FILTER



SYNC_MASTER=J40G	SYNC_DATE=11/23/2012
PAGE TITLE: High Side Current Sensing	
Apple Inc.	DRAWING NUMBER: 051-8937 SIZE: D
	REVISION: 8.0.0
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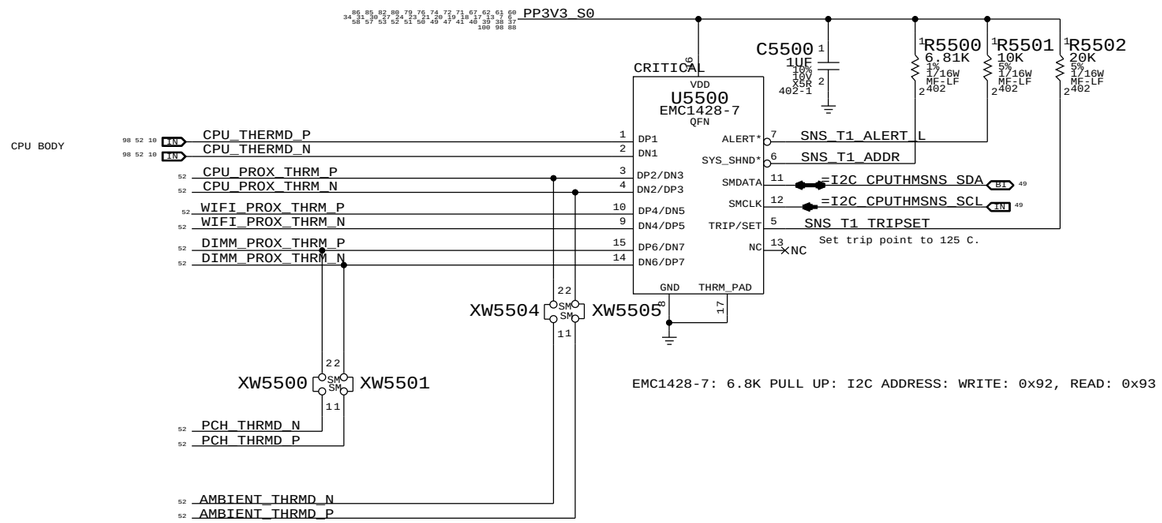
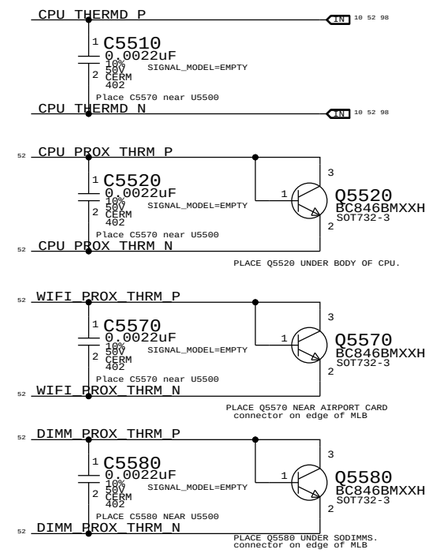
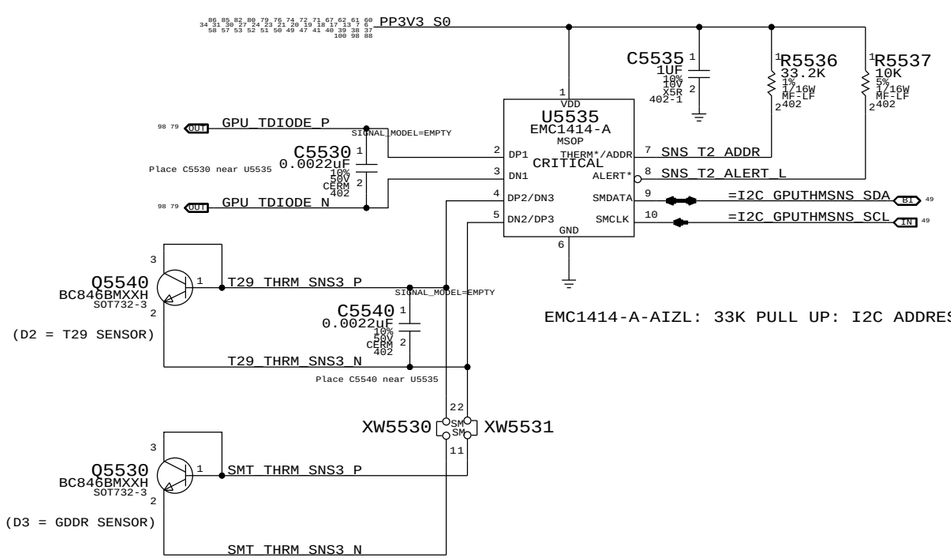


EMC1428-7: 6.8K PULL UP: I2C ADDRESS: WRITE: 0x92, READ: 0x93



GPU DIE/T29/GPU PROXIMITY THERMAL SENSORS



EMC1414-A-AIZL: 33K PULL UP: I2C ADDRESS: WRITE: 0x78, READ: 0x79

SYNC_MASTER=J40G SYNC_DATE=12/09/2016

PAGE TITLE

THERMAL SENSORS

Apple Inc.

DRAWING NUMBER 051-8937 SIZE D

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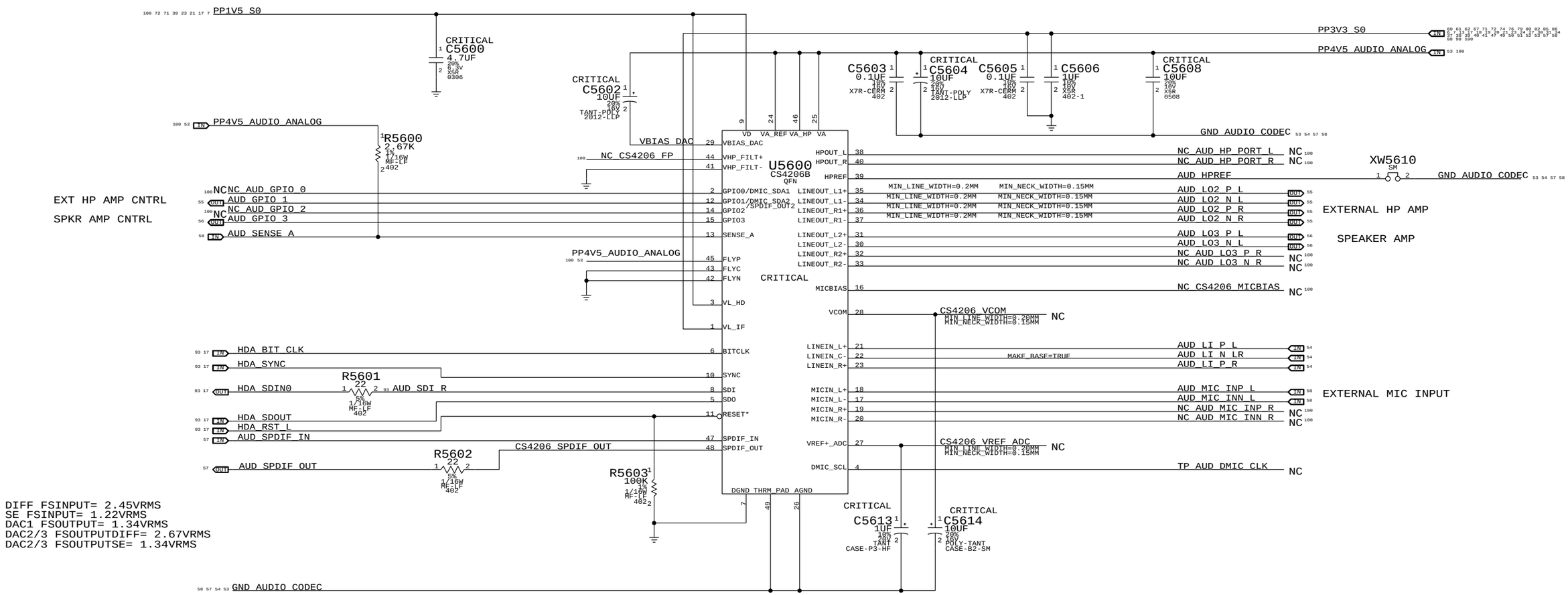
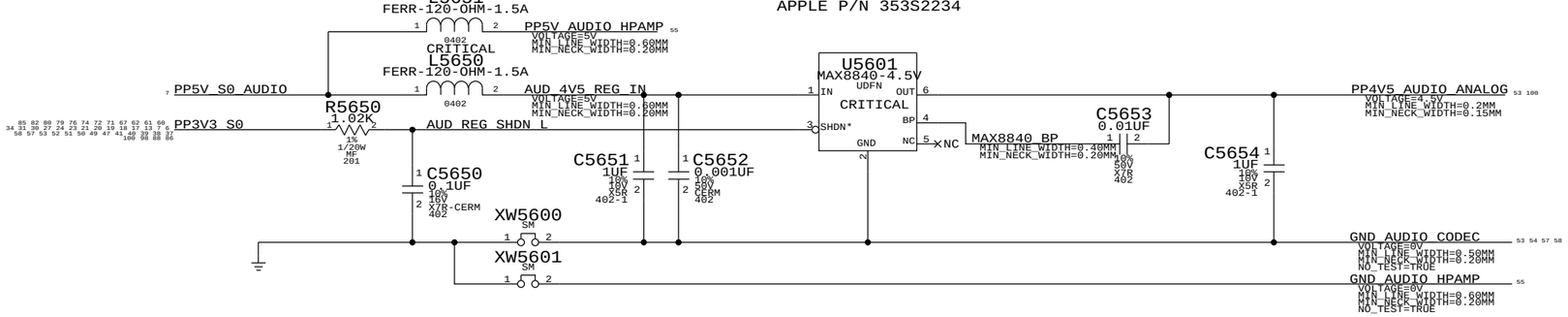
AUDIO CODEC
APPLE P/N 353S3199



DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

AUDIO 4.5V REGULATOR
APPLE P/N 353S2234



SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE: AUDIO:CODEC

Apple Inc.

DRAWING NUMBER: 051-8937 SIZE: D

REVISION: 8.0.0

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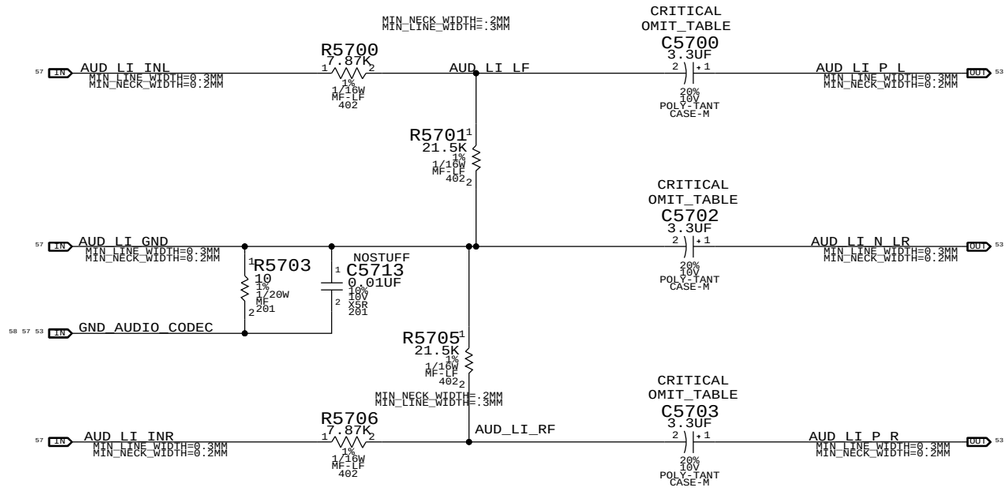
CODEC Nom SE RIN = 20K OHMS
FC = 5 HZ Max
VIN = 2VRMS, CODEC VIN = 1.14 VRMS
NET RIN = 18K OHMS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
128S0309	3	CAP,TANT,POLY,4.7UF,20%,10V,SMD	C5700,C5702,C5703	CRITICAL	?

SYNC MASTER=REFERENCE_MLB SYNC DATE=11/23/2010

PAGE TITLE
AUDIO:LINE-IN

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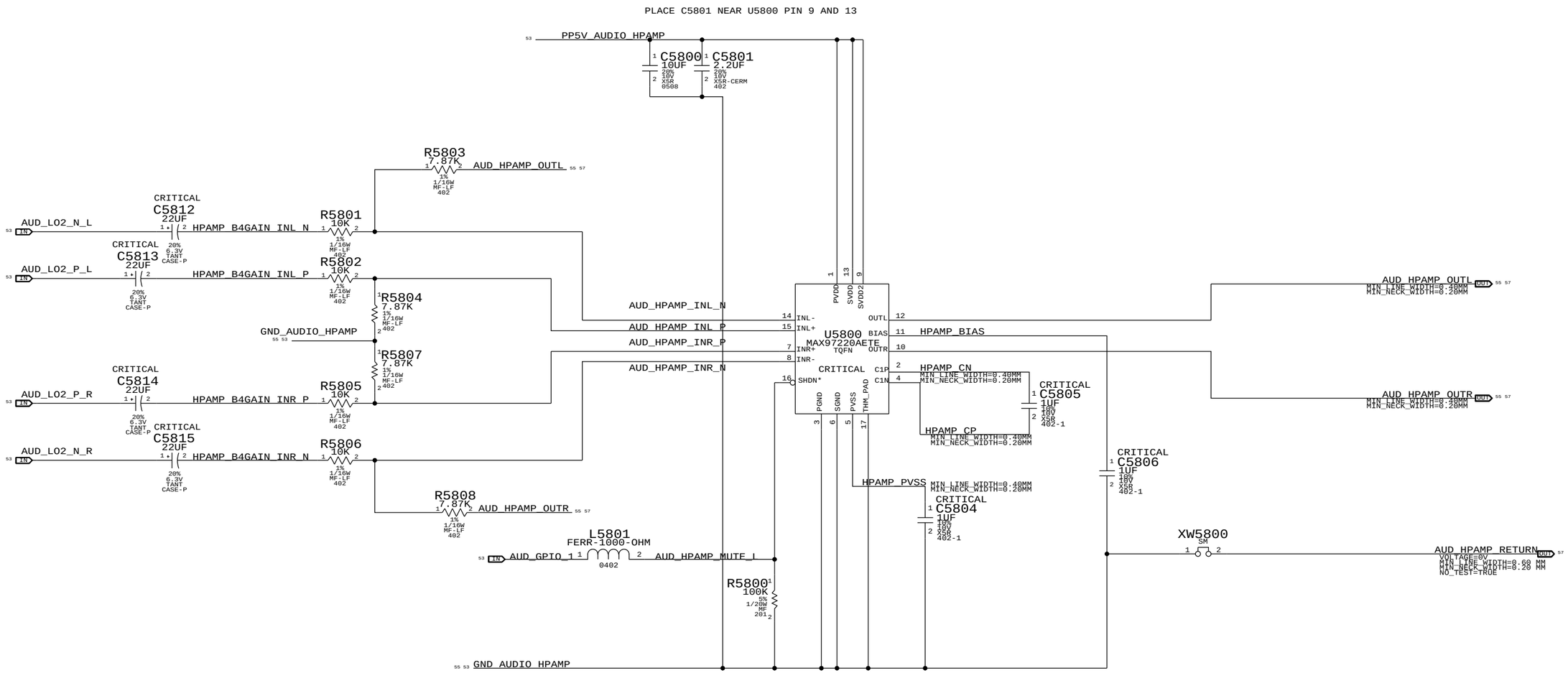
HEADPHONE AMPLIFIER (MAX97220A)

APN:353S3081

VOLTAGE GAIN:-2DB.TO GET 2VRMS FROM 2.67VRMS



DAC FILTER: @ 168KHZ

CODEC FILTER STOPBAND:26.256KHZ, ATTENUATION FROM STOPBAND TO 100KHZ IS 102DB

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE: AUDIO:HEADPHONE AMP

Apple Inc.

DRAWING NUMBER: 051-8937 SIZE: D

REVISION: 8.0.0

BRANCH:

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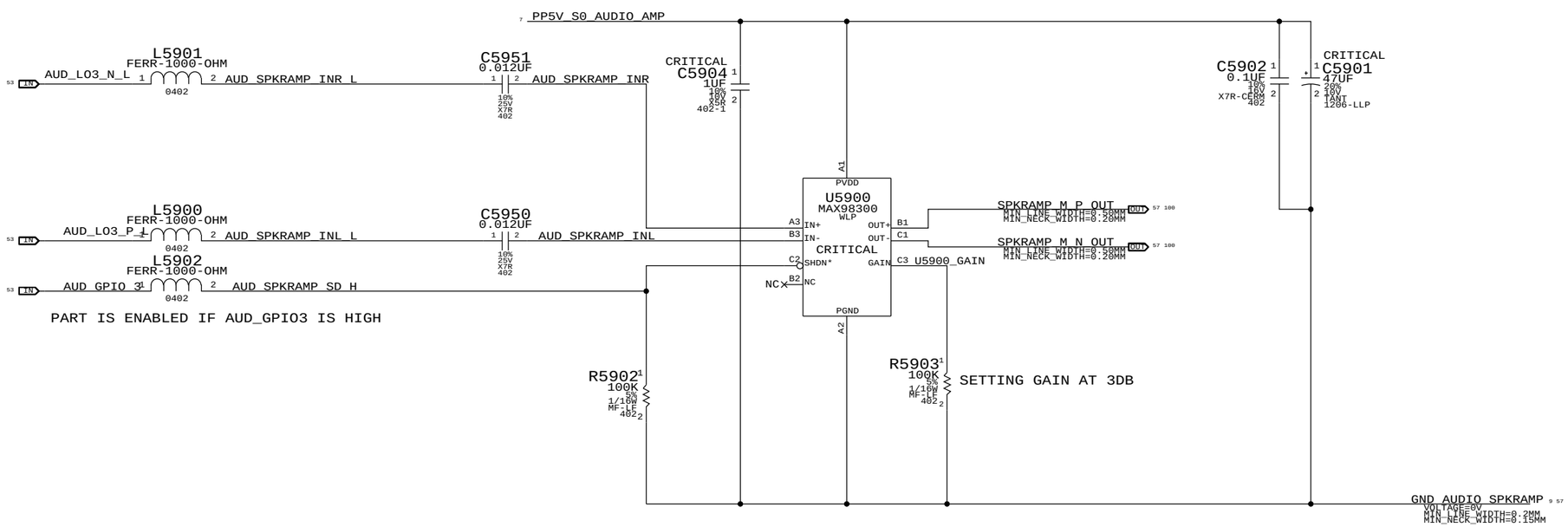
MONO SPEAKER AMPLIFIER

APN 353S2888

GAIN = 3 DB NOM TO ALLOW A LITTLE MORE THAN 1% THD POWER = 2.1W AT 4OHMS.

FC = 470 HZ. RIN AT 3DB IS 28K.



SYNC MASTER=REFERENCE_MLB	SYNC DATE=11/23/2010
PAGE TITLE: AUDIO:SPEAKER AMP	
Apple Inc.	DRAWING NUMBER: 051-8937 — SIZE: D
	REVISION: 8.0.0
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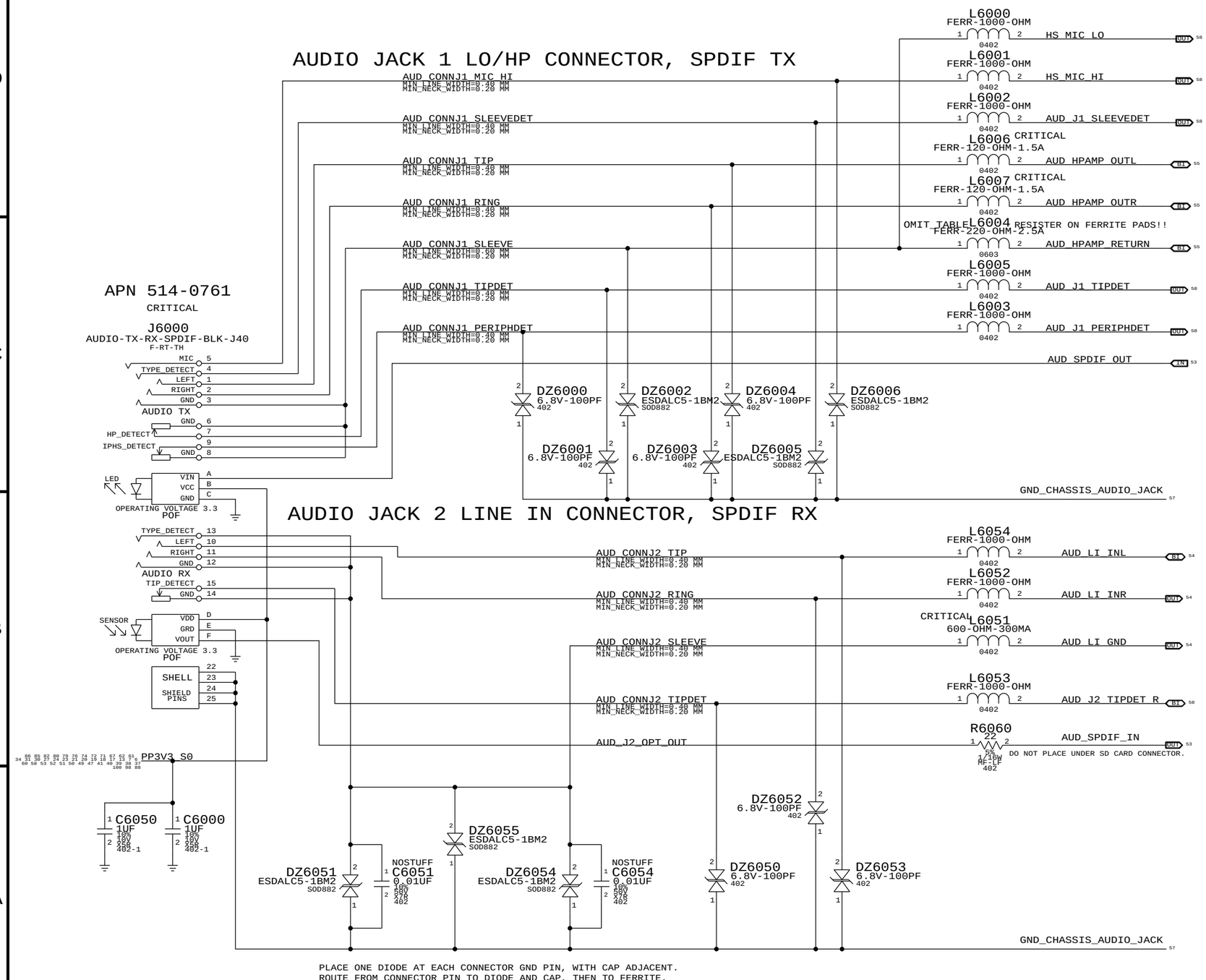
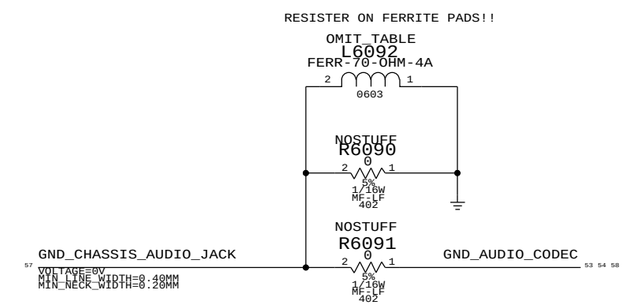
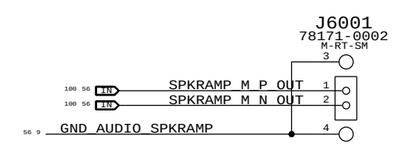


GROUND STUFF OPTIONS
PLACE CLOSE TO CONNECTORS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
113S0022	2	RES,ZERO OHM,0603	L6004,L6092	



SPEAKER CONNECTOR
APN 518S0519



SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE
AUDIO:JACKS

Apple Inc.

DRAWING NUMBER 051-8937 SIZE D

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MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2256

CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	~SHDN CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_1	0X0A(D)
SPEAKER 1	0X04 (4)	0X04 (04)	0X0B (11)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (08)	0X10 (16)	N/A	0X0D(B)

COUGAR POINT OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	~SHDN CONTROL	DET ASSIGNMENT
HDMI OUT	N/A	-	-	N/A	N/A

CODEC INPUT SIGNAL PATHS

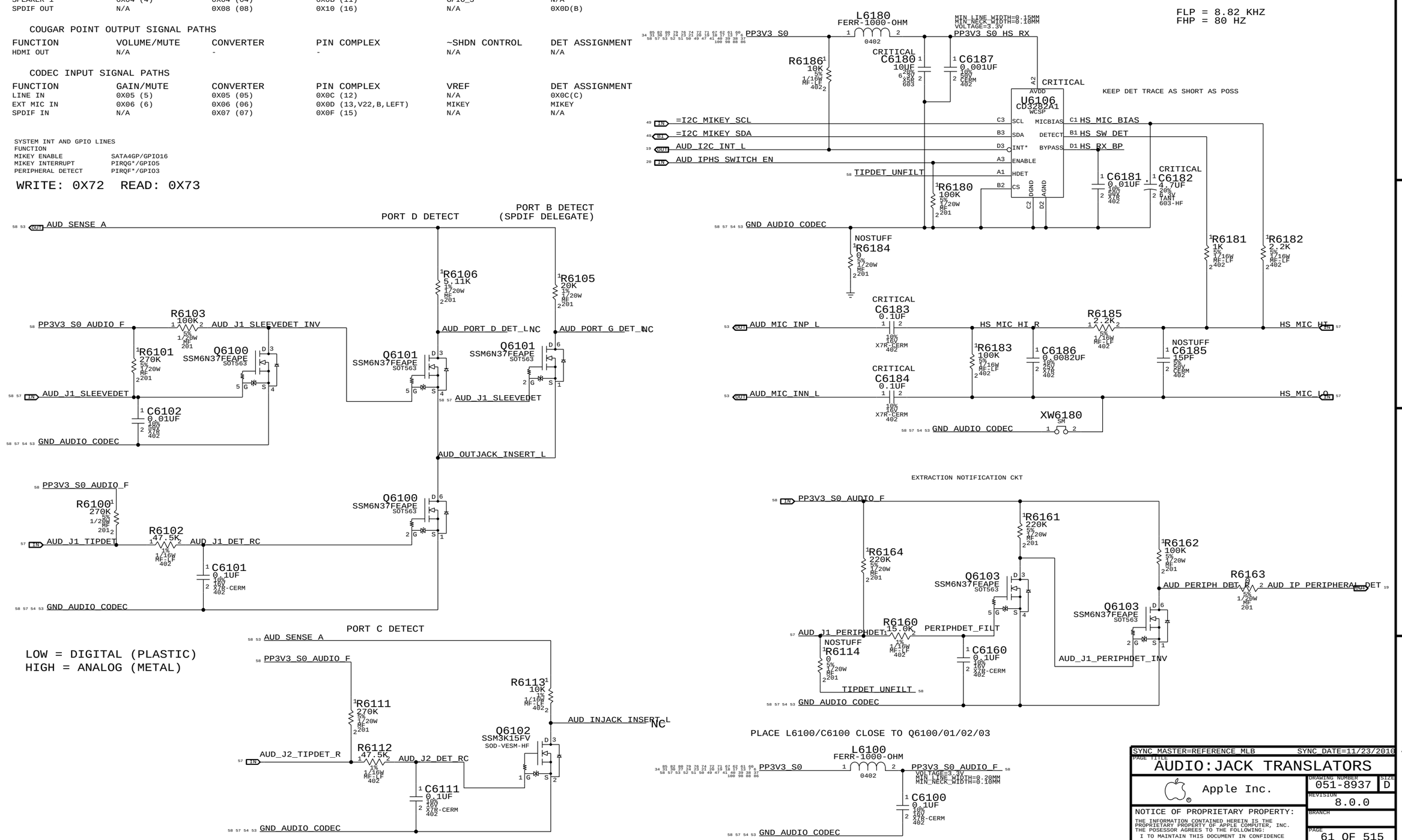
FUNCTION	GAIN/MUTE	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X05 (5)	0X05 (05)	0X0C (12)	N/A	0X0C(C)
EXT MIC IN	0X06 (6)	0X06 (06)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY
SPDIF IN	N/A	0X07 (07)	0X0F (15)	N/A	N/A

SYSTEM INT AND GPIO LINES

FUNCTION	
MIKEY ENABLE	SATA4GP/GPIO16
MIKEY INTERRUPT	PIRQG*/GPIO5
PERIPHERAL DETECT	PIRQF*/GPIO3

WRITE: 0X72 READ: 0X73

FLP = 8.82 KHZ
FHP = 80 HZ



SYNC MASTER=REFERENCE_MLB	SYNC DATE=11/23/2010
PAGE TITLE: AUDIO:JACK TRANSLATORS	
Apple Inc.	DRAWING NUMBER 051-8937 SIZE D
	REVISION 8.0.0
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	PAGE 61 OF 515
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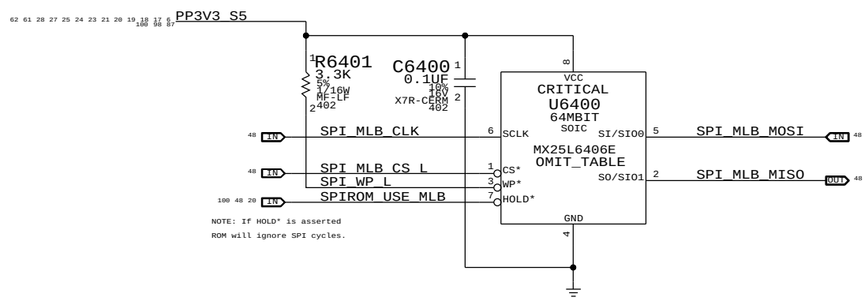

NOTE: If HOLD* is asserted
ROM will ignore SPI cycles.

SYNC MASTER=REFERENCE_MLB SYNC DATE=11/23/2010

PAGE TITLE
SPI BOOT ROM

Apple Inc.

DRAWING NUMBER 051-8937 SIZE D
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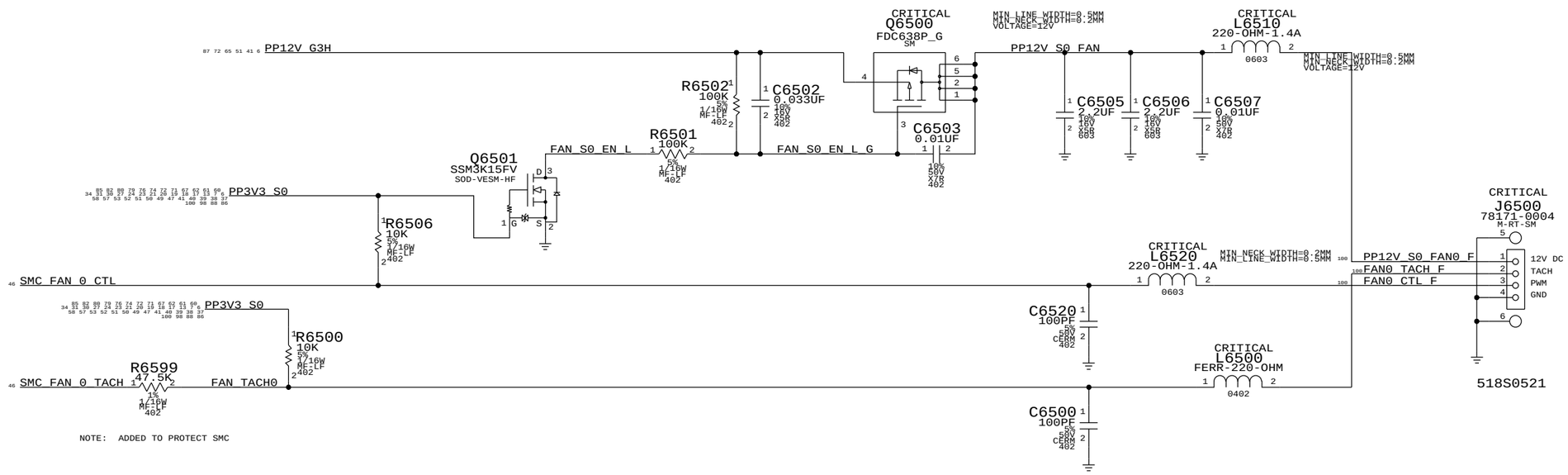
FAN CONTROL CIRCUIT



SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE
Fan Control Circuit

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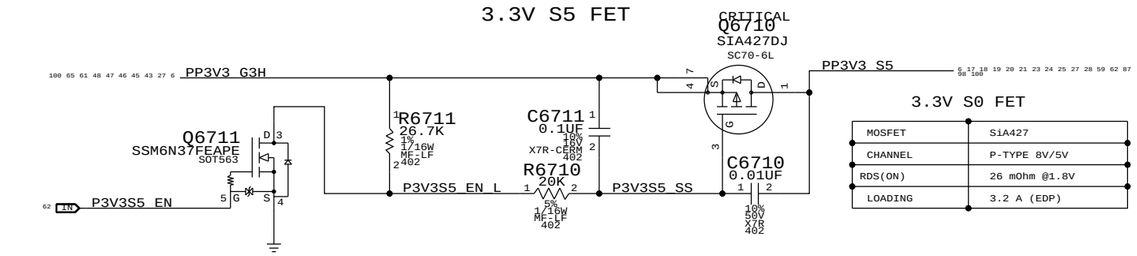
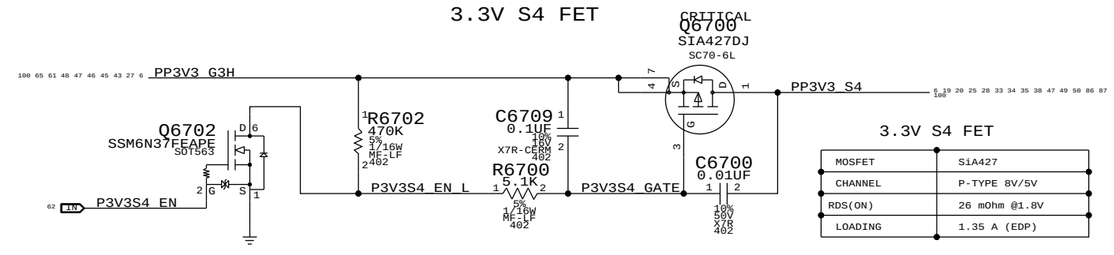


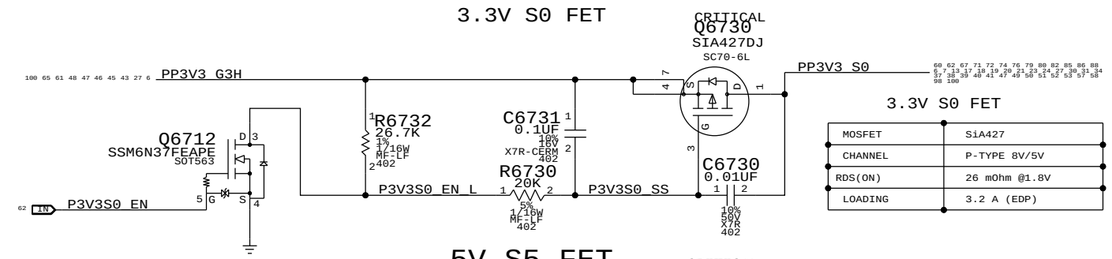
3.3V S0 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3.2 A (EDP)



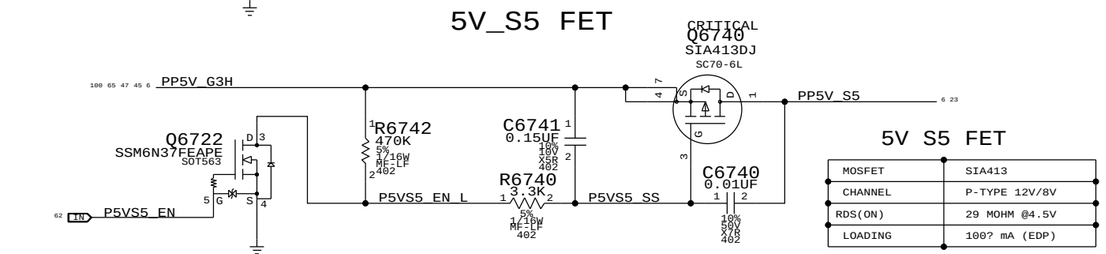
3.3V S4 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.35 A (EDP)



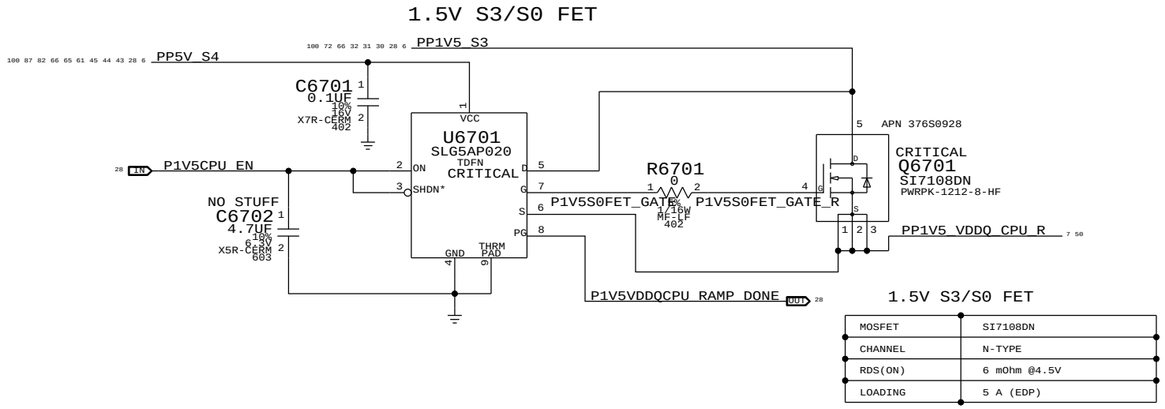
3.3V S0 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3.2 A (EDP)



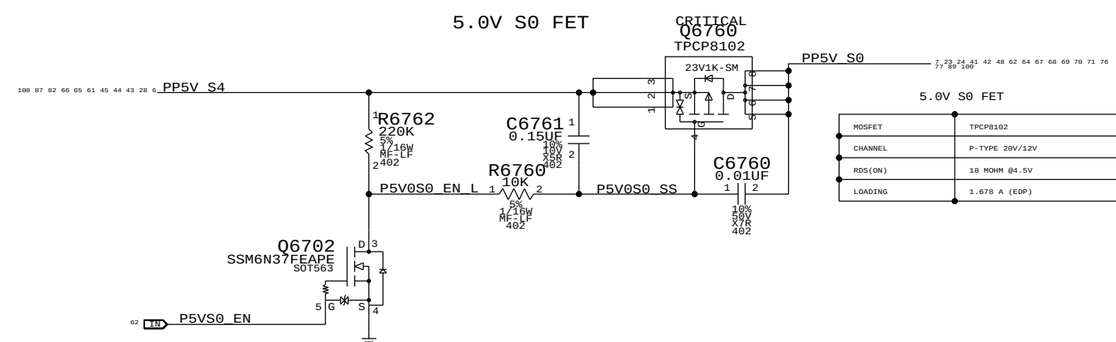
5V S5 FET

MOSFET	SIA413
CHANNEL	P-TYPE 12V/8V
RDS(ON)	29 MOHM @4.5V
LOADING	100? mA (EDP)



1.5V S3/S0 FET

MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	5 A (EDP)



5.0V S0 FET

MOSFET	TPCP8102
CHANNEL	P-TYPE 20V/12V
RDS(ON)	18 MOHM @4.5V
LOADING	1.678 A (EDP)

SYNC MASTER=REFERENCE_MLB SYNC DATE=12/13/2010

PAGE TITLE

Power FETs

Apple Inc.

DRAWING NUMBER 051-8937 SIZE D

REVISION 8.0.0

BRANCH

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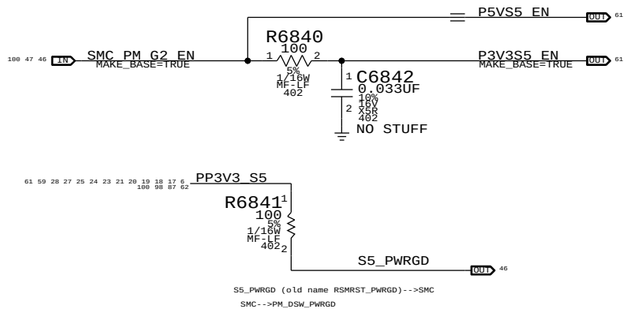
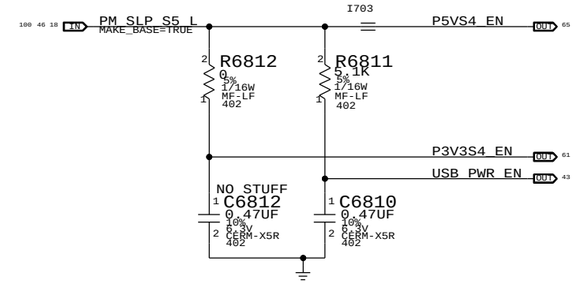
S5 Rail Enables & PGOOD



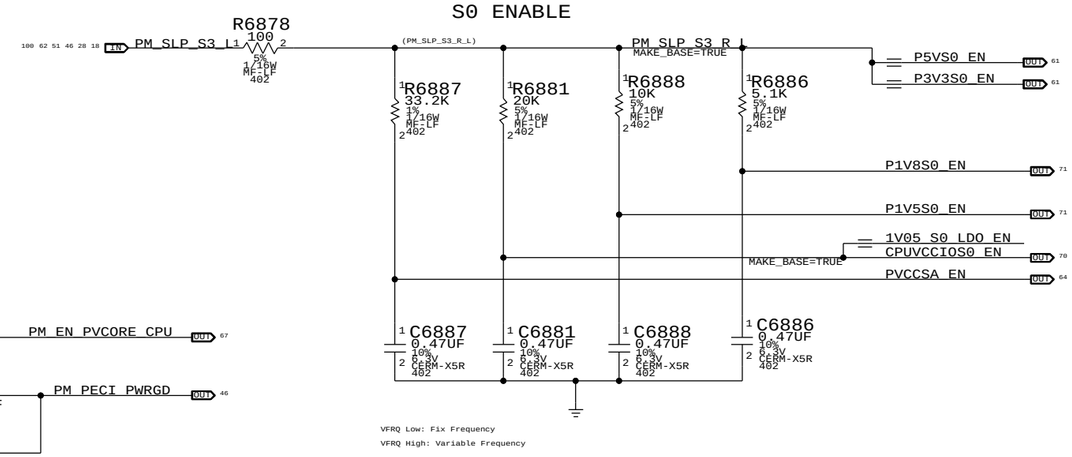
State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	1	0
Deep Sleep (S4)	1	1	0	0
STANDBY (S5)	1	0	0	0
AC POWER (G3HOT)	0	0	0	0

3.3V,5V S4 ENABLE

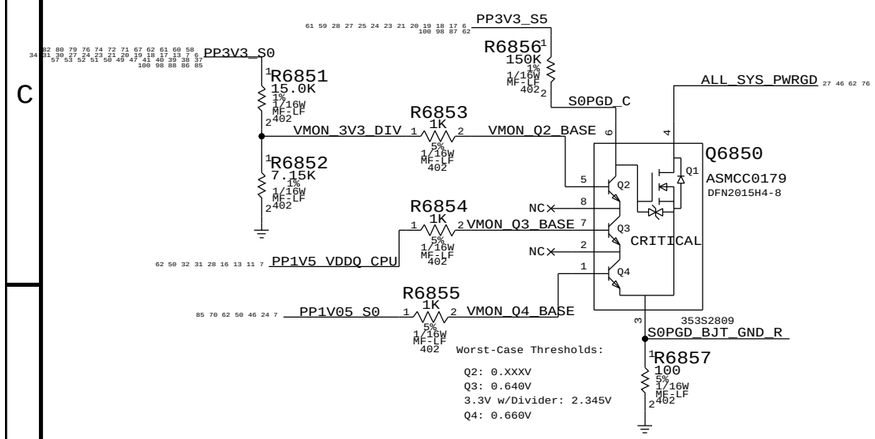


3.3V,5V S3 ENABLE

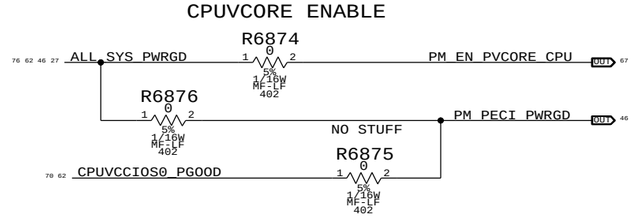
S0 ENABLE



S0 Rail PGOOD (BJT Version)

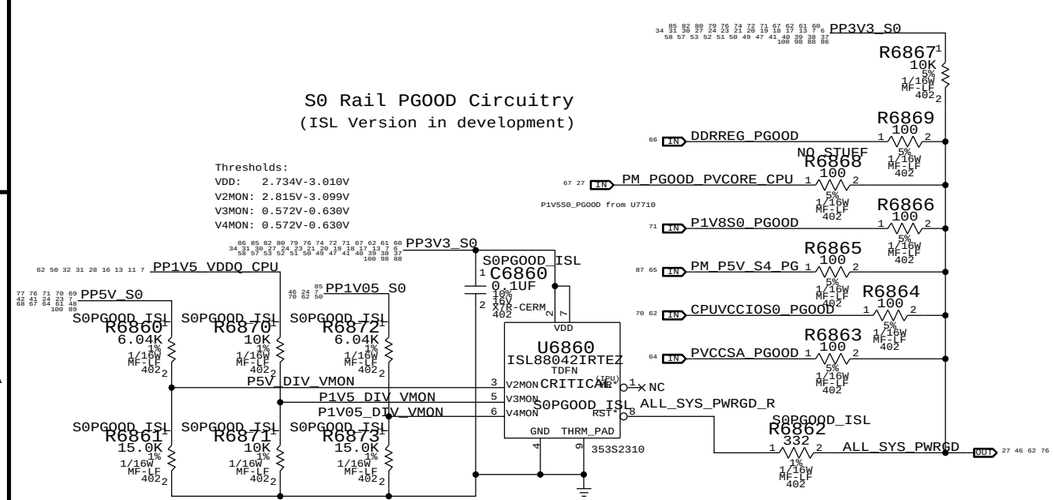


CPUVCORE ENABLE



S0 Rail PGOOD Circuitry

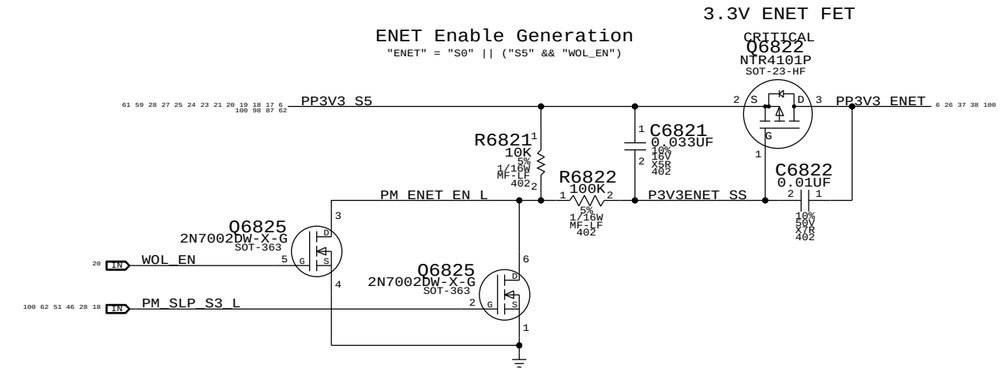
(ISL Version in development)

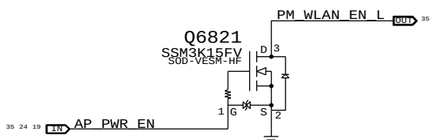


ENET Enable Generation

"ENET" = "S0" || ("S5" && "WOL_EN")

3.3V ENET FET





WLAN Enable Generation

"WLAN" = ("S4" && "AP_PWR_EN")

NOTE: S4 TERM IS GUARANTEED BY S3 PULL-UP ON OPEN-DRAIN AP_PWR_EN SIGNAL.

SYNC MASTER=REFERENCE_MLB SYNC DATE=11/23/2016

PAGE TITLE: Power Control 1/ENABLE

Apple Inc.

DRAWING NUMBER: 051-8937 SIZE: D

REVISION: 8.0.0

BRANCH:

PAGE: 68 OF 515

SHEET: 62 OF 116

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ROOM FOR MORE?

SYNC_MASTER=REFERENCE_MLB SYNC DATE=11/23/2010

PAGE TITLE

POWER CONTROL CONT.

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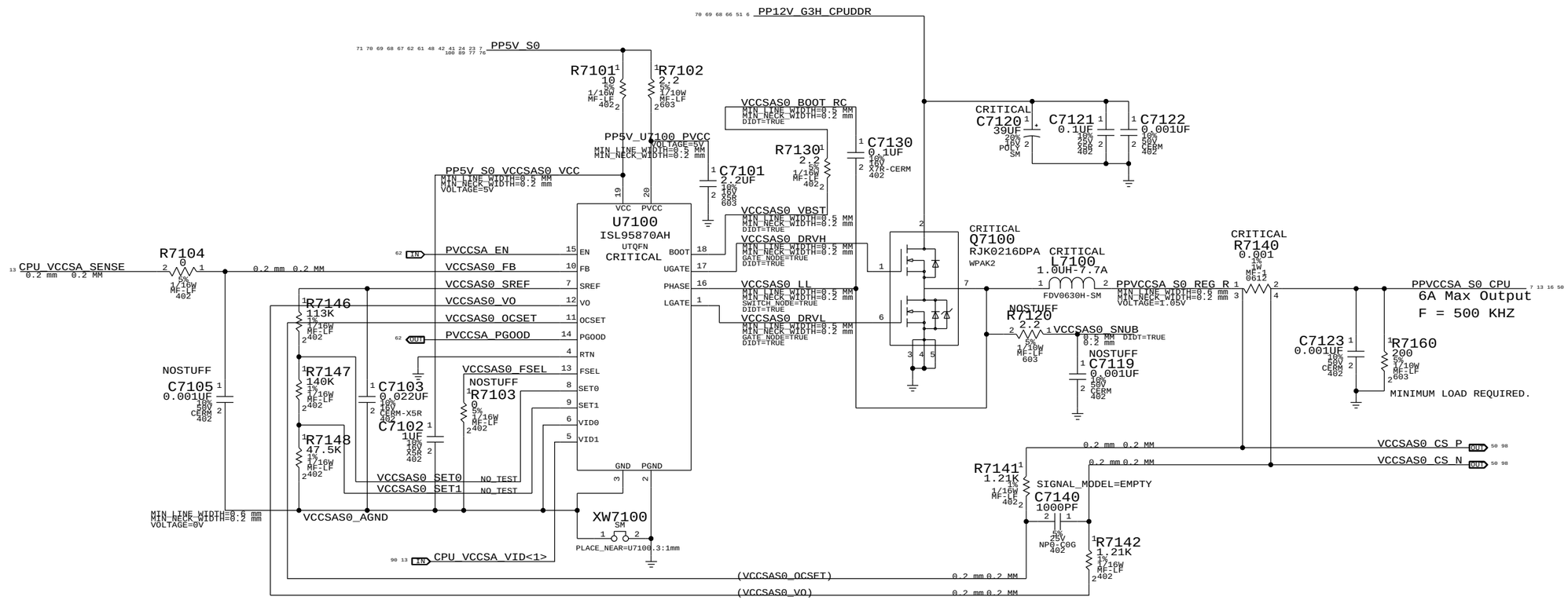
System Agent Power Supply



OCP: 10.3A NOM/7.5A MIN

CPU_VCCSA_VID<0> — PD_CPU_VCCSA_VID0
MAKE_BASE=TRUE

NOT USED FOR 2011 CPUS.

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE
VR - SYSTEM AGENT SUPPLY

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DRAWING NUMBER 051-8937 SIZE D

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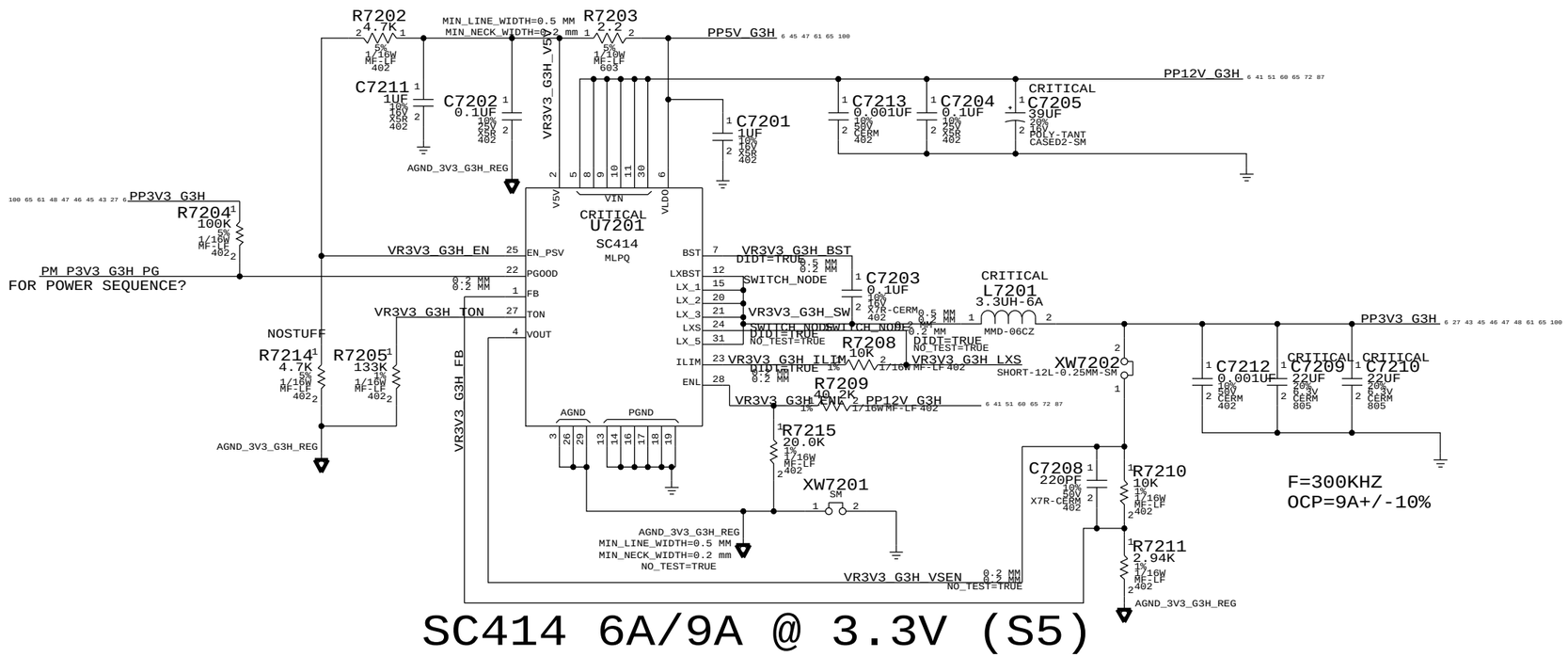
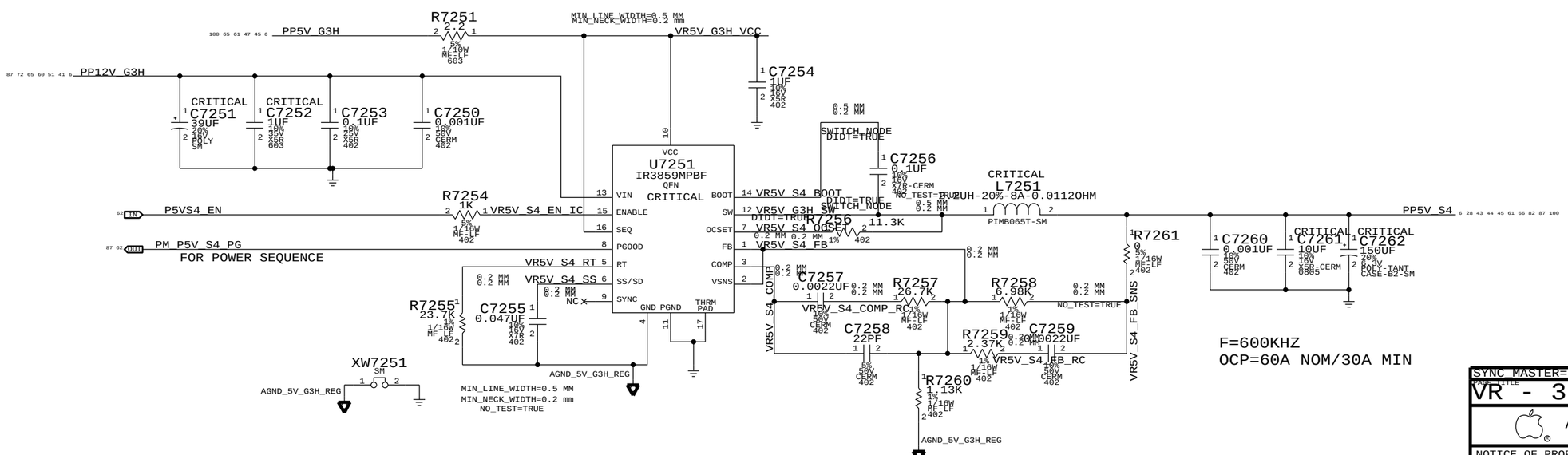


SC414 6A/9A @ 3.3V (S5)



IR3859 5A/9A @ 5V (S4)

SYNC MASTER=REFERENCE MLB SYNC DATE=11/23/2010

PAGE TITLE
VR - 3.3V S5 AND 5V S4

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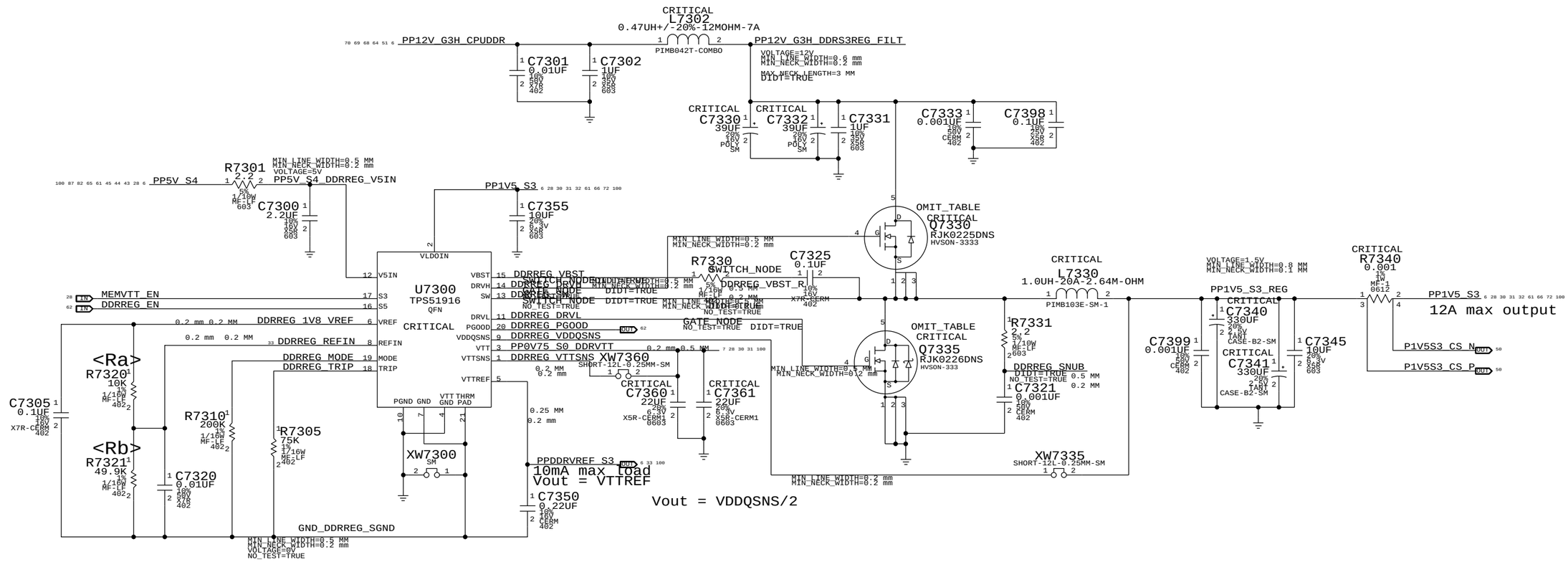

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
376S0979	1	TRA,FET,FAIRCHILD	Q7330	CRITICAL	FET_SET_A:FAIRCHILD
376S0874	1	TRA,FET,FAIRCHILD	Q7335	CRITICAL	FET_SET_A:FAIRCHILD

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
376S0964	1	TRA,FET,RENESAS	Q7330	CRITICAL	FET_SET_A:RENESAS
376S0965	1	TRA,FET,RENESAS	Q7335	CRITICAL	FET_SET_A:RENESAS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
085-3109	1	COMP SET,FETS,FAIRCHILD	CSET1	CRITICAL	FET_SET_A:USE_PHANTOMS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
085-3110	085-3109	FET_SET_A:USE_PHANTOMS	CSET1	COMP SET,FETS,RENESAS

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE
DDR 1.5V VR

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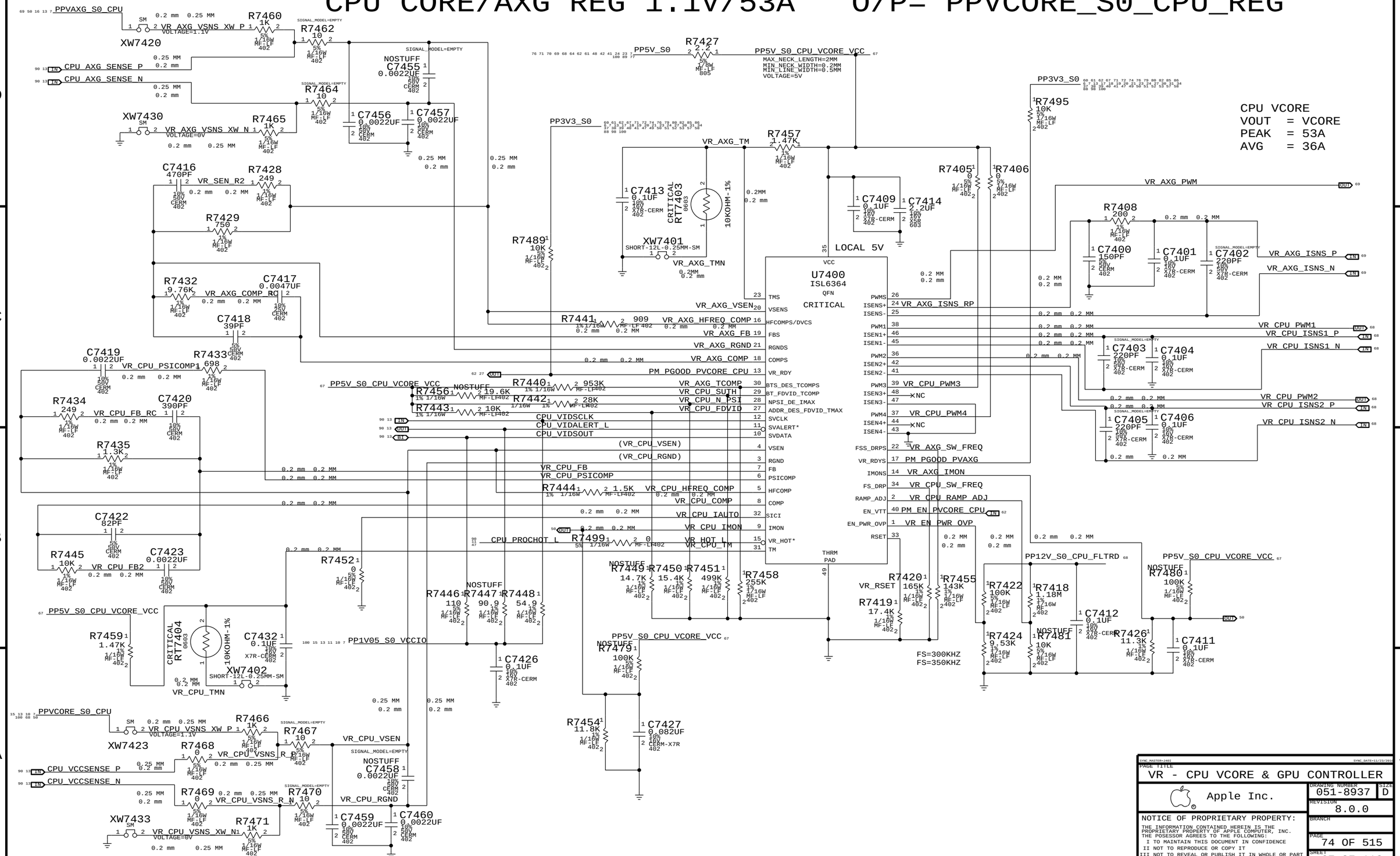
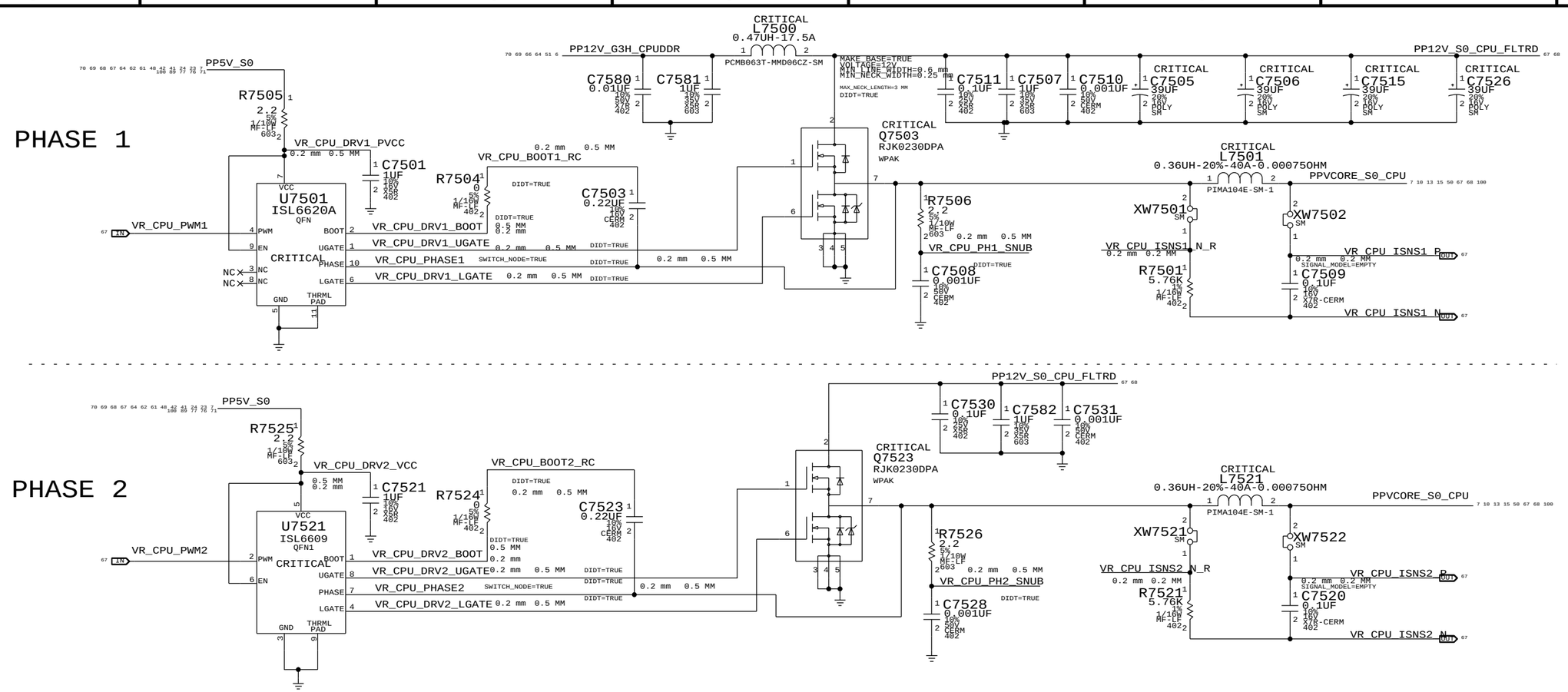
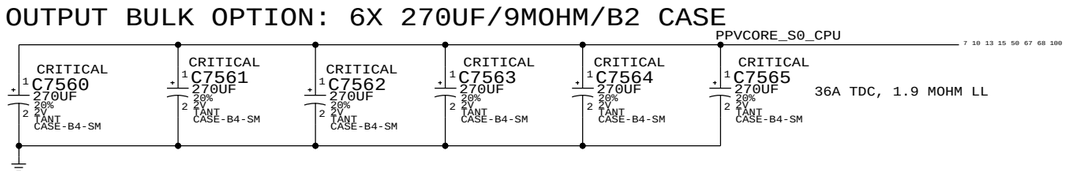
CPU CORE/AXG REG 1.1V/53A O/P= PPVCORE_S0_CPU_REG





OUTPUT BULK OPTION: 6X 270UF/9MOHM/B2 CASE



PAGE TITLE: VR - CPU VCORE OUTPUT PHASES

Apple Inc.

DRAWING NUMBER: 051-8937 SIZE: D

REVISION: 8.0.0

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PAGE: 75 OF 515

SHEET: 68 OF 116

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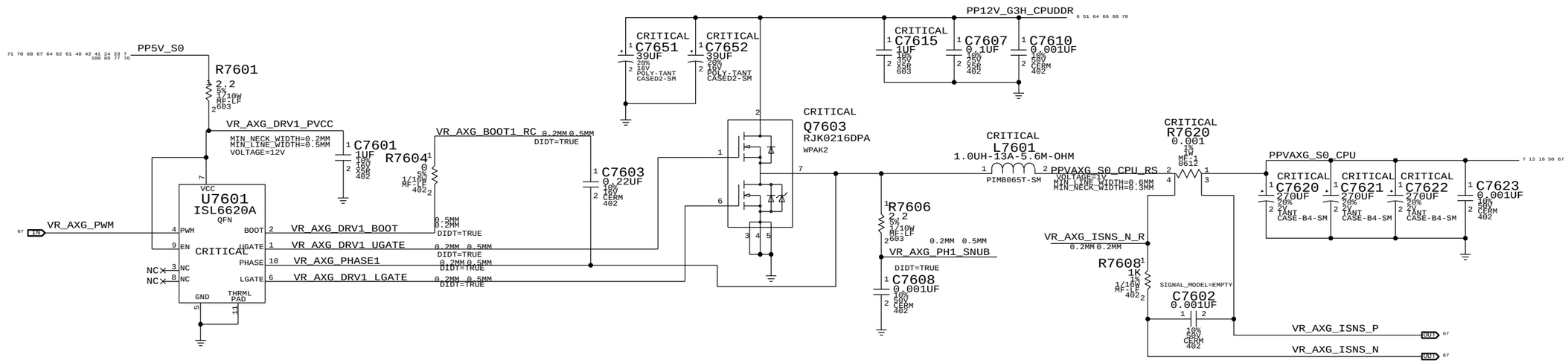
AXG PHASE (8A AVG/15A PEAK, 3.9MOHM LL)



SYNC_MASTER=J40S SYNC_DATE=11/23/2011

PAGE TITLE

VR - GPU

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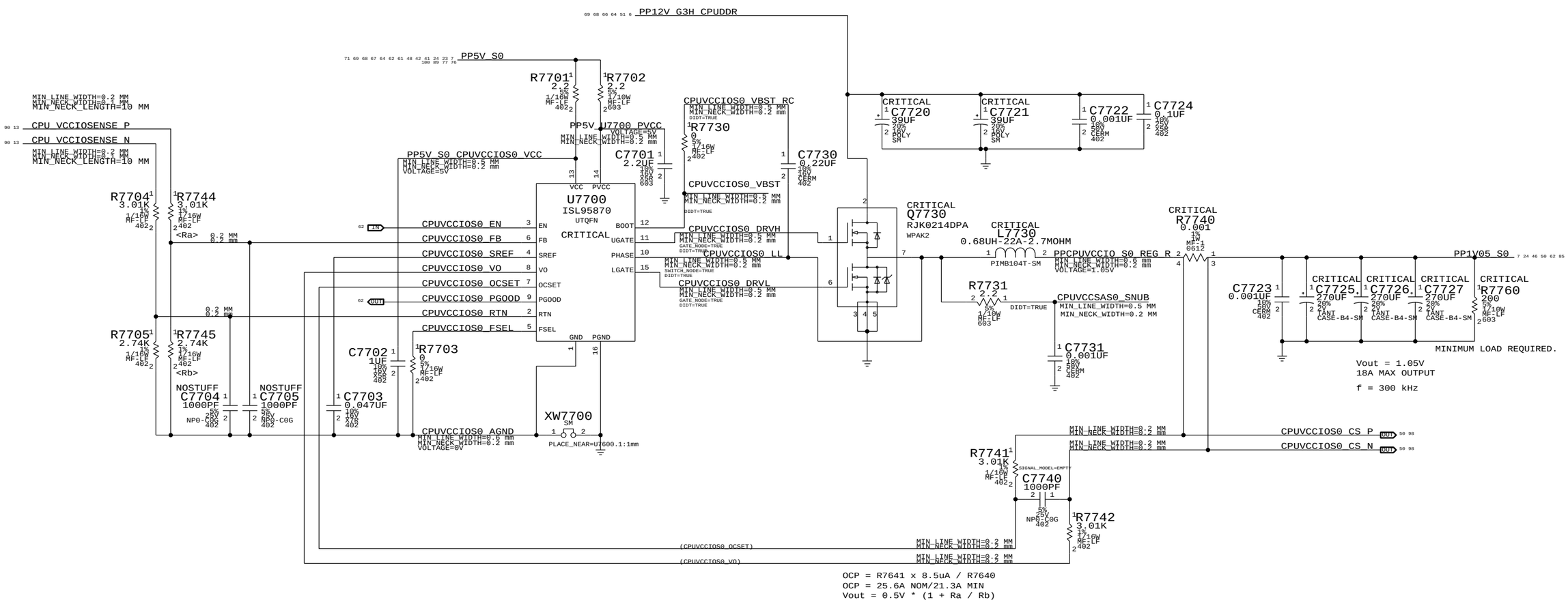
CPU VCCIO (1.05V S0) REGULATOR @ 18A/22A



SYNC_MASTER=J40G SYNC_DATE=12/02/2010

PAGE TITLE: VR - 1.05V S0

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DRAWING NUMBER: 051-8937 SIZE: D

REVISION: 8.0.0

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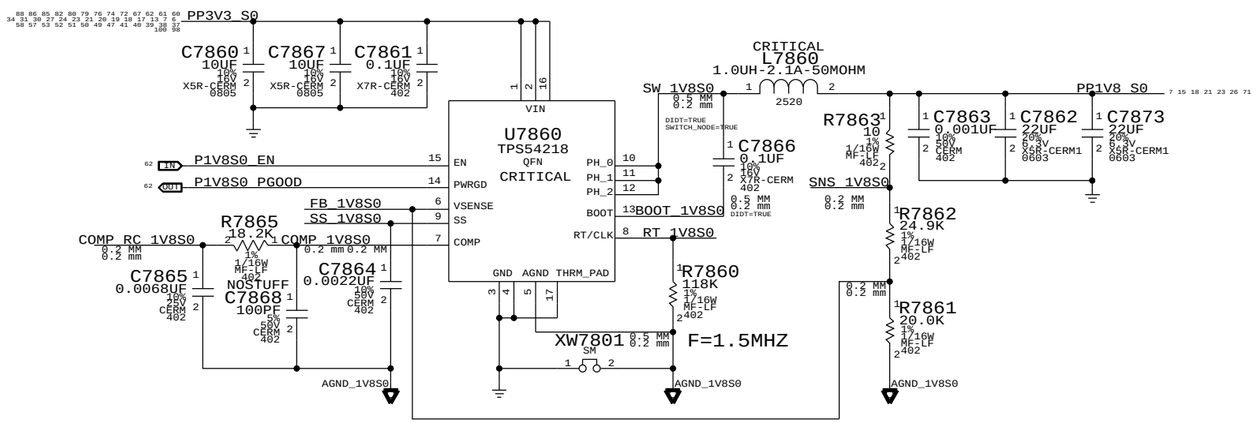
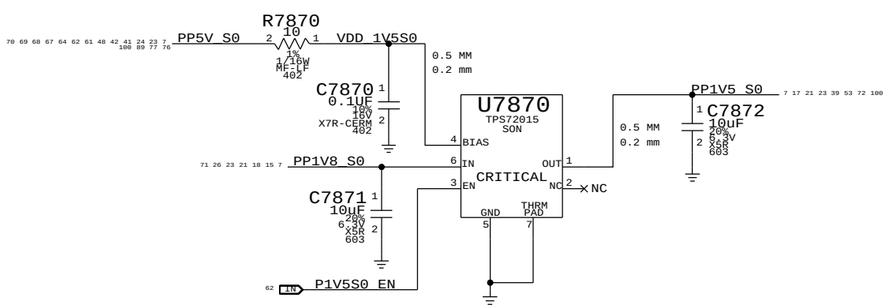
1.8V S0 SWITCHER @ 1.7A/2A



1.5V S0 @ 0.3A/0.5A



SYNC MASTER=REFERENCE_MLB SYNC DATE=11/23/2010

PAGE TITLE

VR - MISC

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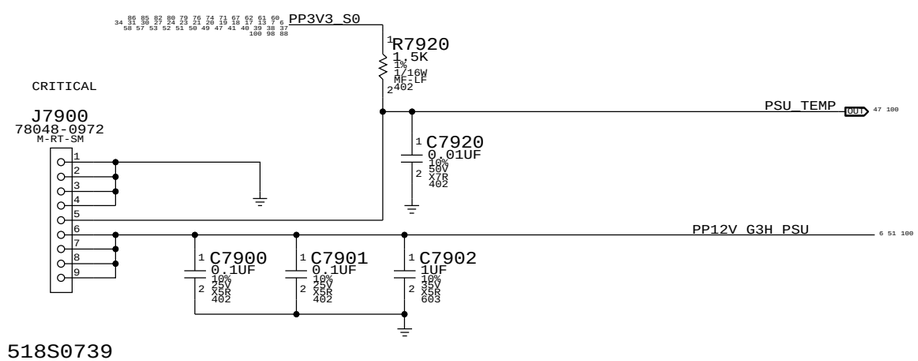
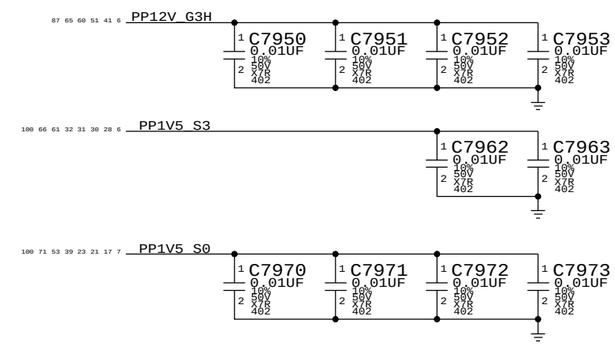


SPRINKLE THESE CAPS SOMEWHAT EVENLY AROUND THE PLANES AND ROUTES FOR THESE RAILS.



SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE
PSU CONNECTOR, MISC CAPS

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DRAWING NUMBER 051-8937 SIZE D

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Page Notes

Power aliases required by this page:

- +PPSV2_GPU_PEX_PLLVDD
- +PPSV2_GPU_PEX_IOVDDQ
- +PPSV2_GPU_PEX_IOVDD

Signal aliases required by this page:

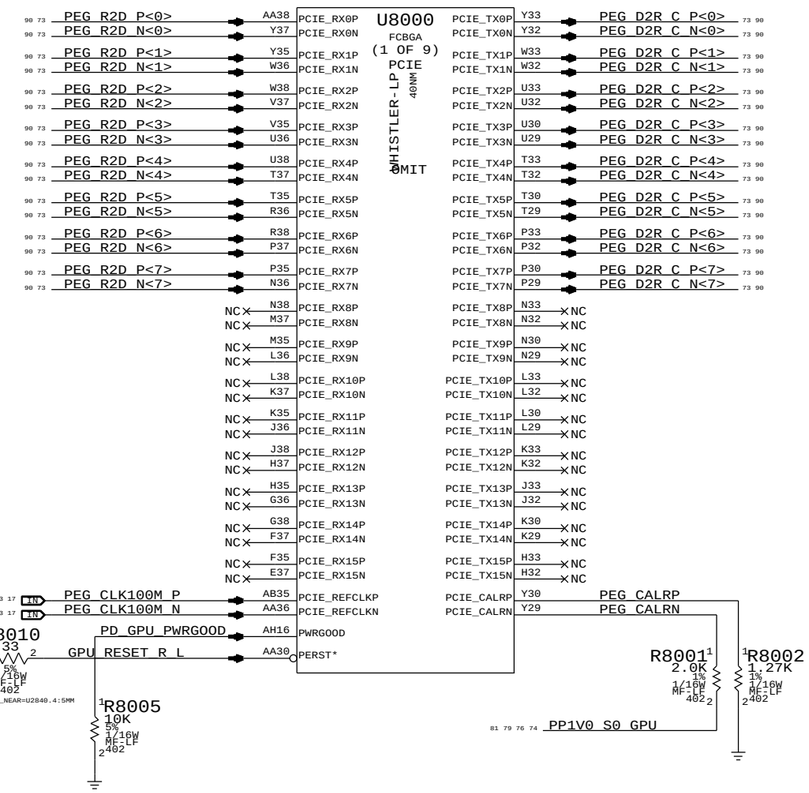
(NONE)

BOM options provided by this page:

(NONE)

90 8	IN	PEG_R2D_C_P<0>	C8020	0.1UF	1	2	PEG_R2D_P<0>	73 90	90 73 PEG_D2R_C_P<0>	C8055	0.1UF
90 8	IN	PEG_R2D_C_N<0>	C8021	0.1UF	1	2	PEG_R2D_N<0>	73 90	90 73 PEG_D2R_C_N<0>	C8056	0.1UF
90 8	IN	PEG_R2D_C_P<1>	C8022	0.1UF	1	2	PEG_R2D_P<1>	73 90	90 73 PEG_D2R_C_P<1>	C8057	0.1UF
90 8	IN	PEG_R2D_C_N<1>	C8023	0.1UF	1	2	PEG_R2D_N<1>	73 90	90 73 PEG_D2R_C_N<1>	C8058	0.1UF
90 8	IN	PEG_R2D_C_P<2>	C8024	0.1UF	1	2	PEG_R2D_P<2>	73 90	90 73 PEG_D2R_C_P<2>	C8059	0.1UF
90 8	IN	PEG_R2D_C_N<2>	C8025	0.1UF	1	2	PEG_R2D_N<2>	73 90	90 73 PEG_D2R_C_N<2>	C8060	0.1UF
90 8	IN	PEG_R2D_C_P<3>	C8026	0.1UF	1	2	PEG_R2D_P<3>	73 90	90 73 PEG_D2R_C_P<3>	C8061	0.1UF
90 8	IN	PEG_R2D_C_N<3>	C8027	0.1UF	1	2	PEG_R2D_N<3>	73 90	90 73 PEG_D2R_C_N<3>	C8062	0.1UF
90 8	IN	PEG_R2D_C_P<4>	C8028	0.1UF	1	2	PEG_R2D_P<4>	73 90	90 73 PEG_D2R_C_P<4>	C8063	0.1UF
90 8	IN	PEG_R2D_C_N<4>	C8029	0.1UF	1	2	PEG_R2D_N<4>	73 90	90 73 PEG_D2R_C_N<4>	C8064	0.1UF
90 8	IN	PEG_R2D_C_P<5>	C8030	0.1UF	1	2	PEG_R2D_P<5>	73 90	90 73 PEG_D2R_C_P<5>	C8065	0.1UF
90 8	IN	PEG_R2D_C_N<5>	C8031	0.1UF	1	2	PEG_R2D_N<5>	73 90	90 73 PEG_D2R_C_N<5>	C8066	0.1UF
90 8	IN	PEG_R2D_C_P<6>	C8032	0.1UF	1	2	PEG_R2D_P<6>	73 90	90 73 PEG_D2R_C_P<6>	C8067	0.1UF
90 8	IN	PEG_R2D_C_N<6>	C8033	0.1UF	1	2	PEG_R2D_N<6>	73 90	90 73 PEG_D2R_C_N<6>	C8068	0.1UF
90 8	IN	PEG_R2D_C_P<7>	C8034	0.1UF	1	2	PEG_R2D_P<7>	73 90	90 73 PEG_D2R_C_P<7>	C8069	0.1UF
90 8	IN	PEG_R2D_C_N<7>	C8035	0.1UF	1	2	PEG_R2D_N<7>	73 90	90 73 PEG_D2R_C_N<7>	C8070	0.1UF

1	2	10%6.3V	X5R	201	1	2	PEG_D2R_P<0>	73 90	8 90	OUT	
1	2	10%6.3V	X5R	201	1	2	PEG_D2R_N<0>	73 90	8 90	OUT	
1	2	10%6.3V	X5R	201	1	2	PEG_D2R_P<1>	73 90	8 90	OUT	
1	2	10%6.3V	X5R	201	1	2	PEG_D2R_N<1>	73 90	8 90	OUT	
1	2	10%6.3V	X5R	201	1	2	PEG_D2R_P<2>	73 90	8 90	OUT	
1	2	10%6.3V	X5R	201	1	2	PEG_D2R_N<2>	73 90	8 90	OUT	
1	2	10%6.3V	X5R	201	1	2	PEG_D2R_P<3>	73 90	8 90	OUT	
1	2	10%6.3V	X5R	201	1	2	PEG_D2R_N<3>	73 90	8 90	OUT	
1	2	10%6.3V	X5R	201	1	2	PEG_D2R_P<4>	73 90	8 90	OUT	
1	2	10%6.3V	X5R	201	1	2	PEG_D2R_N<4>	73 90	8 90	OUT	
1	2	10%6.3V	X5R	201	1	2	PEG_D2R_P<5>	73 90	8 90	OUT	
1	2	10%6.3V	X5R	201	1	2	PEG_D2R_N<5>	73 90	8 90	OUT	
1	2	10%6.3V	X5R	201	1	2	PEG_D2R_P<6>	73 90	8 90	OUT	
1	2	10%6.3V	X5R	201	1	2	PEG_D2R_N<6>	73 90	8 90	OUT	
1	2	10%6.3V	X5R	201	1	2	PEG_D2R_P<7>	73 90	8 90	OUT	
1	2	10%6.3V	X5R	201	1	2	PEG_D2R_N<7>	73 90	8 90	OUT	



SYNC_MASTER=J40G SYNC_DATE=11/23/2010

PAGE TITLE

Whistler PCI-E

Apple Inc.

DRAWING NUMBER 051-8937 SIZE D

REVISION 8.0.0

BRANCH

PAGE 80 OF 515

SHEET 73 OF 116

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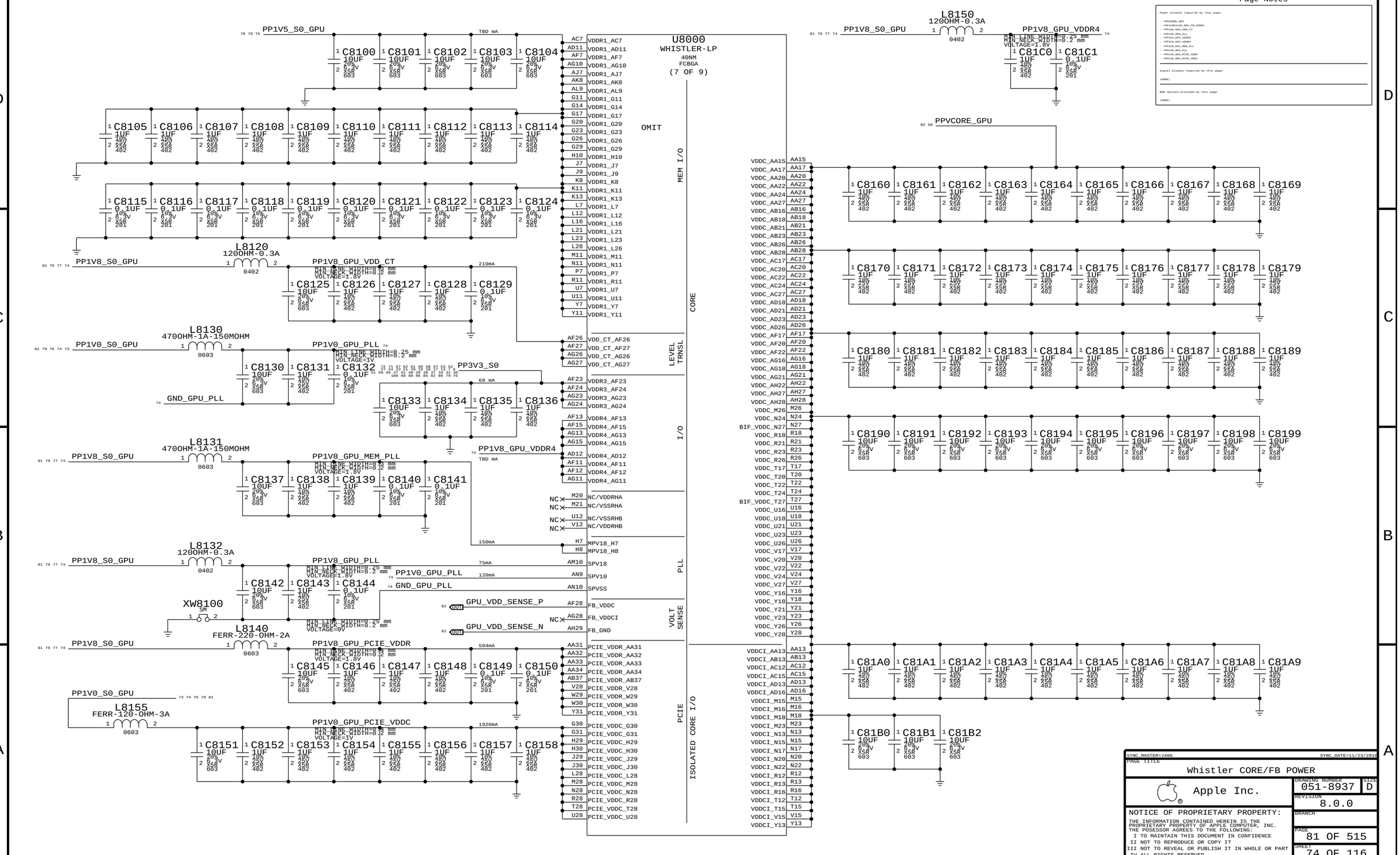
U8000
WHISTLER-LP
40NM
FCBGA
(7 OF 9)
OMIT
MEM I/O
CORE
LEVEL TRNSL
I/O
PLL
VOLT SENSE
PCIE
ISOLATED CORE I/O
PP1V5_S0_GPU
PP1V8_S0_GPU
PP1V8_GPU_VDD_CT
PP1V0_S0_GPU
PP1V0_GPU_PLL
PP3V3_S0
PP1V8_GPU_VDDR4
PP1V8_GPU_MEM_PLL
PP1V8_GPU_PLL
PP1V0_GPU_PLL
PP1V8_GPU_PCIE_VDDR
PP1V0_GPU_PCIE_VDDC
PPVCORE_GPU
GND_GPU_PLL
GPU_VDD_SENSE_P
GPU_VDD_SENSE_N
L8150
120OHM-0.3A
L8120
120OHM-0.3A
L8130
470OHM-1A-150MOHM
L8131
470OHM-1A-150MOHM
L8132
120OHM-0.3A
L8140
FERR-220-OHM-2A
L8155
FERR-120-OHM-3A
XW8100
Page Notes
Power aliases required by this page:
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)
SYNC MASTER=J40G
SYNC DATE=11/23/2010
PAGE TITLE
Whistler CORE/FB POWER
Apple Inc.
DRAWING NUMBER
051-8937
SIZE
D
REVISION
8.0.0
BRANCH
PAGE
81 OF 515
SHEET
74 OF 116
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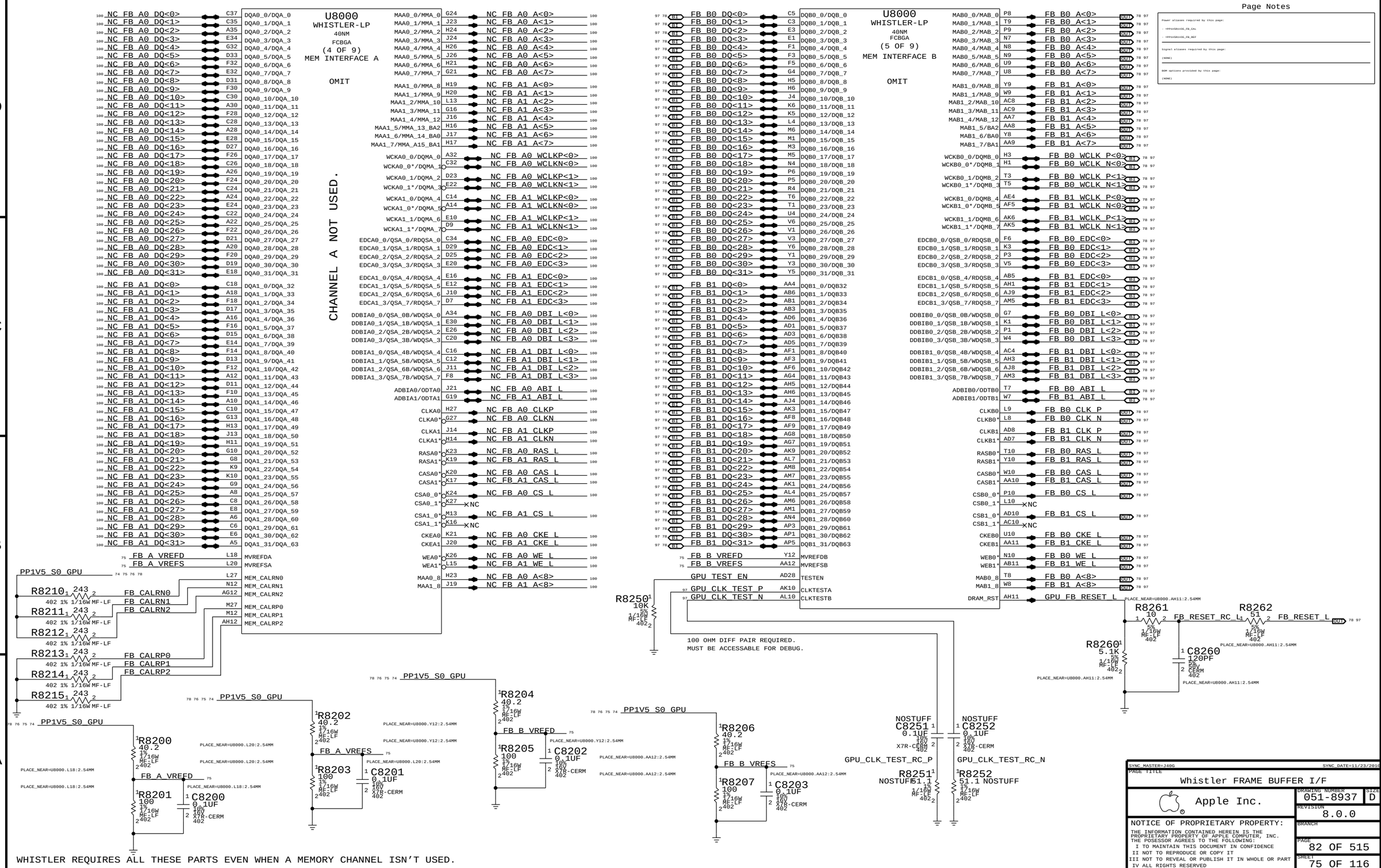
U8000
WHISTLER-LP
40NM
FCBGA
(4 OF 9)
MEM INTERFACE A
OMIT
CHANNEL A NOT USED.
U8000
WHISTLER-LP
40NM
FCBGA
(5 OF 9)
MEM INTERFACE B
OMIT
Page Notes
100 OHM DIFF PAIR REQUIRED.
MUST BE ACCESSABLE FOR DEBUG.
WHISTLER REQUIRES ALL THESE PARTS EVEN WHEN A MEMORY CHANNEL ISN'T USED.
SYNC_MASTER=J40G
SYNC_DATE=11/23/2010
PAGE TITLE
Whistler FRAME BUFFER I/F
Apple Inc.
DRAWING NUMBER
051-8937
SIZE
D
REVISION
8.0.0
BRANCH
PAGE
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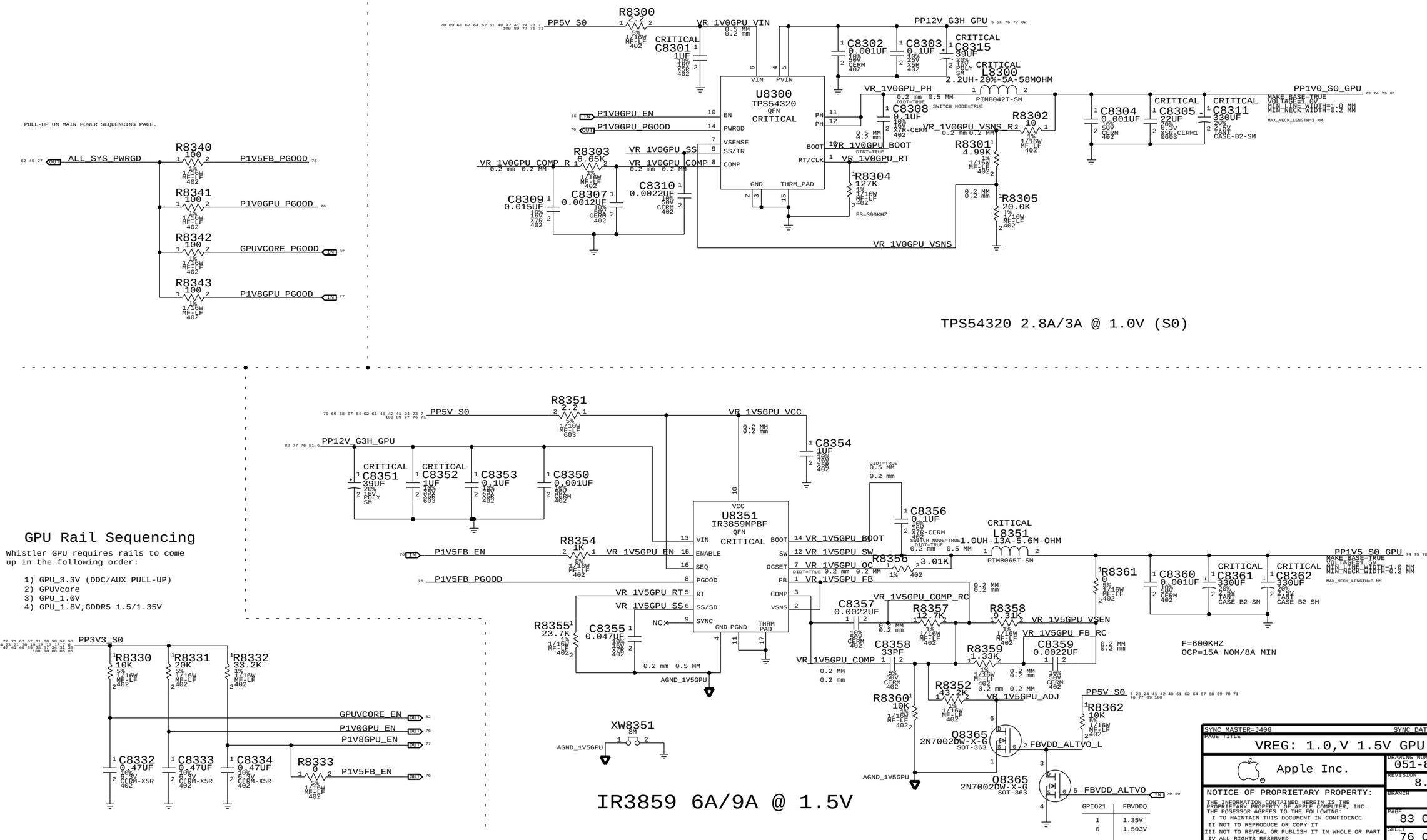

SYNC_MASTER=J40G SYNC_DATE=11/23/2010

PAGE TITLE

VREG: 1.0,V 1.5V GPU

Apple Inc.

DRAWING NUMBER 051-8937 SIZE D

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PAGE 83 OF 515

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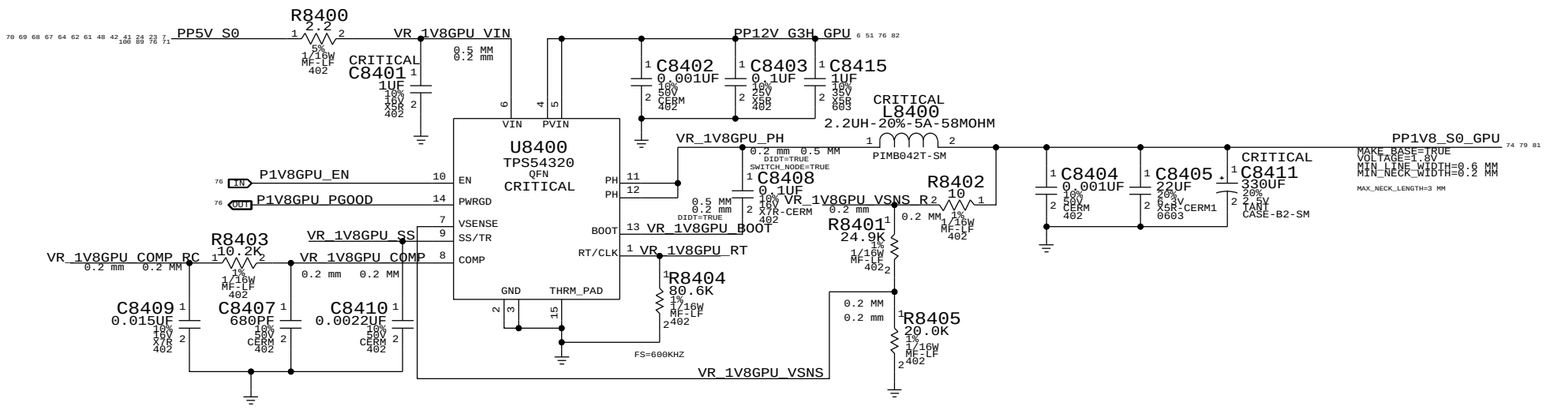

TPS54320 3A @ 1.8V (S0)

SYNC_MASTER=J40G SYNC_DATE=11/23/2010

PAGE TITLE

VREG:PP1V8_S0_GPU

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Page Notes

Power aliases required by this page:
- +PP1V5VRSV5_S0_FB_VDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

BITS SWAPPABLE BY BITS AND 8-BIT GROUPS.
GROUPS 2 AND 3 ARE SWAPPED.

U8500
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
OMIT

U8500
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)
OMIT

U8550
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
OMIT

U8550
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)
OMIT

BITS SWAPPABLE BY BITS AND 8-BIT GROUPS.

Page	Title
78	GDDR5 Frame Buffer B

Apple Inc.

DRAWING NUMBER 051-8937 SIZE D
REVISION 8.0.0
BRANCH
PAGE 85 OF 515
SHEET 78 OF 116

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Page Notes

Power aliases required by this page:
- +PP3V3_GPU_I2C
- +PP1V8_GPU_VREFG
- +PP1V8_GPU_DPLL
- +PP1V0_GPU_DPLL
- +PP1V8_GPU_TS

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PP1V8_S0_GPU

NOSTUFF R8610[1] 10K 5% 1/16W MF-LF 402 2
NOSTUFF R8611[1] 10K 5% 1/16W MF-LF 402 2
NOSTUFF R8612[1] 10K 5% 1/16W MF-LF 402 2
NOSTUFF R8613[1] 10K 5% 1/16W MF-LF 402 2

STRAPS FOR VIDEO MEMORY ID, IF NEEDED.

MAKE DVP*, GENERICA, GENERICD ACCESSIBLE FOR BOUNDRY SCAN.

PP3V3_S0

R8600[1] 4.7K 5% 1/10W MF-LF 402 2
[1]R8601 4.7K 5% 1/10W MF-LF 402 2

SMBUS SLAVE ID
DEFAULT = 0X41

NOTE: GPIO_21_BB_EN
MUST BE 0V AT RESET.

GPIO_23_CLKREQ* IS A RESERVED PIN.

GPIO_22_ROMCS* = HIGH ENABLES EXTERNAL BIOS ROM.

GPIO_19_CTF IS ACTIVE HIGH OUTPUT.

GPIO_17_THERMAL_INT IS ACTIVE LOW INPUT.

PP1V8_S0_GPU

R8602[1] 499 1% 1/16W MF-LF 402 2
C8600[1] 0.1UF 10% 16V X7R-CERM 402 2
R8603[1] 249 1% 1/16W MF-LF 402 2

L8600 470OHM-1A-150MOHM 0603
PP1V8_S0_GPU VOLTAGE=1.8V
C8601[1] 10UF 20% 6.3V X5R 603 2
C8602[1] 1UF 10% 25V X5R 402 2
C8603[1] 0.1UF 10% 16V X7R-CERM 402 2
MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.8V

L8601 470OHM-1A-150MOHM 0603
PP1V0_S0_GPU
C8604[1] 10UF 20% 6.3V X5R 603 2
C8605[1] 1UF 10% 25V X5R 402 2
C8606[1] 0.1UF 10% 16V X7R-CERM 402 2
MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1V

XW8600 SM
GND_GPU_DPLL
MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=0V

L8602 120OHM-0.3A 0402
PP1V8_S0_GPU
C8607[1] 10UF 20% 6.3V X5R 603 2
C8608[1] 1UF 10% 25V X5R 402 2
C8609[1] 0.1UF 10% 16V X7R-CERM 402 2
MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.8V

XW8601 SM
GND_GPU_TSVSS
MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=0V

U8000
WHISTLER-LP
40NM
FCBGA
(2 OF 9)

Signal	Ball	Function	Group
TP_DVPCNTL_M<0>	AR8	DVPCNTL_MVP_0	DPA
TP_DVPCNTL_M<1>	AU8	DVPCNTL_MVP_1	DPA
TP_DVPCNTL<0>	AP8	DVPCNTL_0	DPA
TP_DVPCNTL<1>	AW8	DVPCNTL_1	DPA
TP_DVPCNTL<2>	AR3	DVPCNTL_2	DPA
TP_DVPCLK	AR1	DVPCLK	DPA
DVPDATA<0>	AU1	DVPDATA_0	DPA
DVPDATA<1>	AU3	DVPDATA_1	DPA
DVPDATA<2>	AW3	DVPDATA_2	DPA
DVPDATA<3>	AP6	DVPDATA_3	DPA
TP_DVPDATA<4>	AW5	DVPDATA_4	DPA
TP_DVPDATA<5>	AU5	DVPDATA_5	DPA
TP_DVPDATA<6>	AR6	DVPDATA_6	DPA
TP_DVPDATA<7>	AW6	DVPDATA_7	DPA
TP_DVPDATA<8>	AU6	DVPDATA_8	DPA
TP_DVPDATA<9>	AT7	DVPDATA_9	DPA
TP_DVPDATA<10>	AV7	DVPDATA_10	DPA
TP_DVPDATA<11>	AN7	DVPDATA_11	DPA
TP_DVPDATA<12>	AV9	DVPDATA_12	DPA
TP_DVPDATA<13>	AT9	DVPDATA_13	DPA
TP_DVPDATA<14>	AR10	DVPDATA_14	DPA
TP_DVPDATA<15>	AW10	DVPDATA_15	DPA
TP_DVPDATA<16>	AU10	DVPDATA_16	DPA
TP_DVPDATA<17>	AP10	DVPDATA_17	DPA
TP_DVPDATA<18>	AV11	DVPDATA_18	DPA
TP_DVPDATA<19>	AT11	DVPDATA_19	DPA
TP_DVPDATA<20>	AR12	DVPDATA_20	DPA
TP_DVPDATA<21>	AW12	DVPDATA_21	DPA
TP_DVPDATA<22>	AU12	DVPDATA_22	DPA
TP_DVPDATA<23>	AP12	DVPDATA_23	DPA
NC	AJ21	SWAPLOCKA	MULTI GFX
NC	AK21	SWAPLOCKB	MULTI GFX
GPU_I2C_SCL	AK26	SCL	I2C
GPU_I2C_SDA	AJ26	SDA	I2C
GPU_PCIE_TX_PWR	AH20	GPIO_0	GPIO
GPU_GPIO_TX_DEEMP	AH18	GPIO_1	GPIO
GPU_PCIE_GEN2	AN16	GPIO_2	GPIO
GPU_SMB_DAT	AH23	GPIO_3_SMBDATA	GPIO
GPU_SMB_CLK	AJ23	GPIO_4_SMBCLK	GPIO
GPU_AC_BATT	AH17	GPIO_5_AC_BATT	GPIO
GPU_VCORE_VID0	AJ17	GPIO_6	GPIO
EG_BKLT_EN	AK17	GPIO_7_BLON	GPIO
GPU_ROM_SO	AJ13	GPIO_8_ROMSO	GPIO
GPU_ROM_SI	AH15	GPIO_9_ROMSI	GPIO
GPU_ROM_SCLK	AJ16	GPIO_10_ROMSCK	GPIO
GPU_CONFIG_0	AK16	GPIO_11	GPIO
GPU_CONFIG_1	AL16	GPIO_12	GPIO
GPU_CONFIG_2	AM16	GPIO_13	GPIO
=EG_DP_T29SNK0_HPD	AM14	GPIO_14_HPD2	GPIO
GPU_VCORE_VID1	AM13	GPIO_15_PWRCNTL_0	GPIO
GPU_VCORE_VID2	AK14	GPIO_16	GPIO
SMC_GFX_THROTTLE_R_L	AG30	GPIO_17_THERMAL_INT	GPIO
=EG_HDMI_HPD	AN14	GPIO_18_HPD3	GPIO
SMC_GFX_OVERTEMP_R	AM17	GPIO_19_CTF	GPIO
GPU_VCORE_VID3	AL13	GPIO_20_PWRCNTL_1	GPIO
FBVDD_ALTVO	AJ14	GPIO_21_BB_EN	GPIO
GPU_ROM_CS_L	AK13	GPIO_22_ROMCS*	GPIO
GPIO_23_NC	AN13	GPIO_23_CLKREQ*	GPIO
GPU_JTAG_TRST_L	AM23	JTAG_TRST*	GPIO
GPU_JTAG_TDI	AN23	JTAG_TDI	GPIO
GPU_JTAG_TCK	AK23	JTAG_TCK	GPIO
GPU_JTAG_TMS	AL24	JTAG_TMS	GPIO
GPU_JTAG_TDO	AM24	JTAG_TDO	GPIO
TP_GPU_GENERICA	AJ19	GENERICA	GPIO
NC_GPU_GENERICB	AK19	GENERICB	GPIO
NC_GPU_GENERICC	AJ20	GENERICC	GPIO
DP_CA_DET_EG_R	AK20	GENERICD	GPIO
=EG_DP_T29SNK1_HPD	AJ24	GENERICE_HPD4	GPIO
NC_GPU_GENERICF	AH26	GENERICF_HPD5	GPIO
NC_GPU_GENERICG	AH24	GENERICG_HPD6	GPIO
=EG_DP_EXTA_HPD	AK24	HPD1	GPIO
GPU_VREFG (0.60V)	AH13	VREFG	GPIO
PP1V8_GPU_DPLL 75mA	AM32	DPLL_PVDD	PLL/CLK
(GND_GPU_DPLL)	AN32	DPLL_PVSS	PLL/CLK
PP1V0_GPU_DPLL 125mA	AN31	DPLL_VDDC	PLL/CLK
NC	AV33	XTALIN	PLL/CLK
NC	AU34	XTALOUT	PLL/CLK
GPU_CLK27M	AW34	XO_IN	PLL/CLK
GPU_CLK100M	AW35	XO_IN2	PLL/CLK
GPU_TDIODE_P	AF29	DPLUS	THERMAL
GPU_TDIODE_N	AG29	DMINUS	THERMAL
GPU_TS_FDO	AK32	TS_FDO	THERMAL
NC	AL31	TSA/NC	THERMAL
PP1V8_GPU_TSVDD 20mA	AJ32	TSVDD	THERMAL
(GND_GPU_TSVSS)	AJ33	TSVSS	THERMAL

OMIT

Signal	Ball	Function	Group
TXCAP_DPA3P	AU24	=EG_DP_EXTA_ML_C_P<3>	DPA
TXCAM_DPA3N	AV23	=EG_DP_EXTA_ML_C_N<3>	DPA
TX0P_DPA2P	AT25	=EG_DP_EXTA_ML_C_P<2>	DPA
TX0M_DPA2N	AR24	=EG_DP_EXTA_ML_C_N<2>	DPA
TX1P_DPA1P	AU26	=EG_DP_EXTA_ML_C_P<1>	DPA
TX1M_DPA1N	AV25	=EG_DP_EXTA_ML_C_N<1>	DPA
TX2P_DPA0P	AT27	=EG_DP_EXTA_ML_C_P<0>	DPA
TX2M_DPA0N	AR26	=EG_DP_EXTA_ML_C_N<0>	DPA
TXCBP_DPB3P	AR30	=EG_DP_T29SNK0_ML_C_P<3>	DPB
TXCBM_DPB3N	AT29	=EG_DP_T29SNK0_ML_C_N<3>	DPB
TX3P_DPB2P	AV31	=EG_DP_T29SNK0_ML_C_P<2>	DPB
TX3M_DPB2N	AU30	=EG_DP_T29SNK0_ML_C_N<2>	DPB
TX4P_DPB1P	AR32	=EG_DP_T29SNK0_ML_C_P<1>	DPB
TX4M_DPB1N	AT31	=EG_DP_T29SNK0_ML_C_N<1>	DPB
TX5P_DPB0P	AT33	=EG_DP_T29SNK0_ML_C_P<0>	DPB
TX5M_DPB0N	AU32	=EG_DP_T29SNK0_ML_C_N<0>	DPB
TXCCP_DPC3P	AU14	=EG_HDMI_CLK_P	DPC
TXCCM_DPC3N	AV13	=EG_HDMI_CLK_N	DPC
TX0P_DPC2P	AT15	=EG_HDMI_C_P<0>	DPC
TX0M_DPC2N	AR14	=EG_HDMI_C_N<0>	DPC
TX1P_DPC1P	AU16	=EG_HDMI_C_P<1>	DPC
TX1M_DPC1N	AV15	=EG_HDMI_C_N<1>	DPC
TX2P_DPC0P	AT17	=EG_HDMI_C_P<2>	DPC
TX2M_DPC0N	AR16	=EG_HDMI_C_N<2>	DPC
TXCDP_DPD3P	AU20	=EG_DP_T29SNK1_ML_C_P<3>	DPD
TXCDM_DPD3N	AT19	=EG_DP_T29SNK1_ML_C_N<3>	DPD
TX3P_DPD2P	AT21	=EG_DP_T29SNK1_ML_C_P<2>	DPD
TX3M_DPD2N	AR20	=EG_DP_T29SNK1_ML_C_N<2>	DPD
TX4P_DPD1P	AU22	=EG_DP_T29SNK1_ML_C_P<1>	DPD
TX4M_DPD1N	AV21	=EG_DP_T29SNK1_ML_C_N<1>	DPD
TX5P_DPD0P	AT23	=EG_DP_T29SNK1_ML_C_P<0>	DPD
TX5M_DPD0N	AR22	=EG_DP_T29SNK1_ML_C_N<0>	DPD
R	AD39	NC	DAC1
R*	AD37	NC	DAC1
G	AE36	NC	DAC1
G*	AD35	NC	DAC1
B	AF37	NC	DAC1
B*	AE38	NC	DAC1
HSYNC	AC36	GPU_AUD_1	DAC1
VSYNC	AC38	GPU_AUD_0	DAC1
RSET	AB34	NC	DAC1
AVDD	AD34	PP1V8_S0_GPU	DAC1
AVSSQ	AE34		DAC1
VDD1DI	AC33		DAC1
VSS1DI	AC34		DAC1
R2/NC	AC30	NC	DAC2
R2*/NC	AC31	NC	DAC2
G2/NC	AD30	NC	DAC2
G2*/NC	AD31	NC	DAC2
B2/NC	AF30	NC	DAC2
B2*/NC	AF31	NC	DAC2
C/NC	AC32	NC	DAC2
Y/NC	AD32	NC	DAC2
COMP/NC	AF32	NC	DAC2
H2SYNC/GENLK_CLK	AD29	NC	DAC2
V2SYNC/GENLK_VSYNC	AC29	NC	DAC2
VDD2DI/NC	AG31	NC	DAC2
VSS2DI/NC	AG32	NC	DAC2
A2VDD/NC	AG33	NC	DAC2
A2VDDQ/NC	AD33	NC	DAC2
A2VSSQ/TSVSSQ	AF33	GND_GPU_TVSSQ (XW8602 SM) MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=0V	DAC2
R2SET/NC	AA29	NC	DAC2
DDC1CLK	AM26	=EG_DP_EXTA_DDC_CLK	DDC/AUX
DDC1DATA	AN26	=EG_DP_EXTA_DDC_DATA	DDC/AUX
AUX1P	AM27	=EG_DP_EXTA_AUXCH_C_P	DDC/AUX
AUX1N	AL27	=EG_DP_EXTA_AUXCH_C_N	DDC/AUX
DDC2CLK	AM19	NC	DDC/AUX
DDC2DATA	AL19	NC	DDC/AUX
AUX2P	AN20	=EG_DP_T29SNK0_AUXCH_C_P	DDC/AUX
AUX2N	AM20	=EG_DP_T29SNK0_AUXCH_C_N	DDC/AUX
DDCCLK_AUX3P	AL30	=EG_HDMI_DDC_CLK	DDC/AUX
DDCDATA_AUX3N	AM30	=EG_HDMI_DDC_DATA	DDC/AUX
DDCCLK_AUX4P	AL29	=EG_DP_T29SNK1_AUXCH_C_P	DDC/AUX
DDCDATA_AUX4N	AM29	=EG_DP_T29SNK1_AUXCH_C_N	DDC/AUX
DDCCLK_AUX5P	AN21	NC_LVDS_EG_DDC_CLK	DDC/AUX
DDCDATA_AUX5N	AM21	NC_LVDS_EG_DDC_DATA	DDC/AUX
DDC6CLK	AJ30	NC	DDC/AUX
DDC6DATA	AJ31	NC	DDC/AUX
DDCCLK_AUX7P	AK30	NC	DDC/AUX
DDCDATA_AUX7N	AK29	NC	DDC/AUX

NOTE:

GPIO_22_ROMCS*	CONFIG[2:0]	
0	=001	TO SELECT MEM APERTURE = 256MB
1	=101	TO INDICATE ROM IS M25P10A.

PP3V3_S0
Straps for audio on DP and HDMI
R8604[1] 10K 5% 1/10W MF-LF 402 2
[1]R8605 10K 5% 1/10W MF-LF 402 2

U8000
FCBGA
(3 OF 9)
WHISTLER-LP 40NM

LVDS CNTL

Signal	Ball	Function
VARY_BL	AK27	PD_LVDS_EG_BLK_PWM
DIGON	AJ27	PD_EG_LCD_PWR_EN
TXCLK_UP_DPF3P	AK35	NC_LVDS_EG_B_CLKP
TXCLK_UN_DPF3N	AL36	NC_LVDS_EG_B_CLKN
TXOUT_U0P_DPF2P	AJ38	NC_LVDS_EG_B_DATAP<0>
TXOUT_U0N_DPF2N	AK37	NC_LVDS_EG_B_DATAN<0>
TXOUT_U1P_DPF1P	AH35	NC_LVDS_EG_B_DATAP<1>
TXOUT_U1N_DPF1N	AJ36	NC_LVDS_EG_B_DATAN<1>
TXOUT_U2P_DPF0P	AG38	NC_LVDS_EG_B_DATAP<2>
TXOUT_U2N_DPF0N	AH37	NC_LVDS_EG_B_DATAP<2>
TXOUT_U3P	AF35	NC_LVDS_EG_B_DATAP<3>
TXOUT_U3N	AG36	NC_LVDS_EG_B_DATAN<3>
TXCLK_LP_DPE3P	AP34	NC_LVDS_EG_A_CLKP
TXCLK_LN_DPE3N	AR34	NC_LVDS_EG_A_CLKN
TXOUT_L0P_DPE2P	AW37	NC_LVDS_EG_A_DATAP<0>
TXOUT_L0N_DPE2N	AU35	NC_LVDS_EG_A_DATAN<0>
TXOUT_L1P_DPE1P	AR37	NC_LVDS_EG_A_DATAP<1>
TXOUT_L1N_DPE1N	AU39	NC_LVDS_EG_A_DATAN<1>
TXOUT_L2P_DPE0P	AP35	NC_LVDS_EG_A_DATAP<2>
TXOUT_L2N_DPE0N	AR35	NC_LVDS_EG_A_DATAN<2>
TXOUT_L3P	AN36	NC_LVDS_EG_A_DATAP<3>
TXOUT_L3N	AP37	NC_LVDS_EG_A_DATAN<3>

OMIT

[1]R8606 10K 5% 1/16W MF-LF 402 2
[1]R8607 10K 5% 1/16W MF-LF 402 2

SYNC_MASTER=J40G SYNC_DATE=11/23/2010
PAGE TITLE
Whistler LVDS/DP/GPIO

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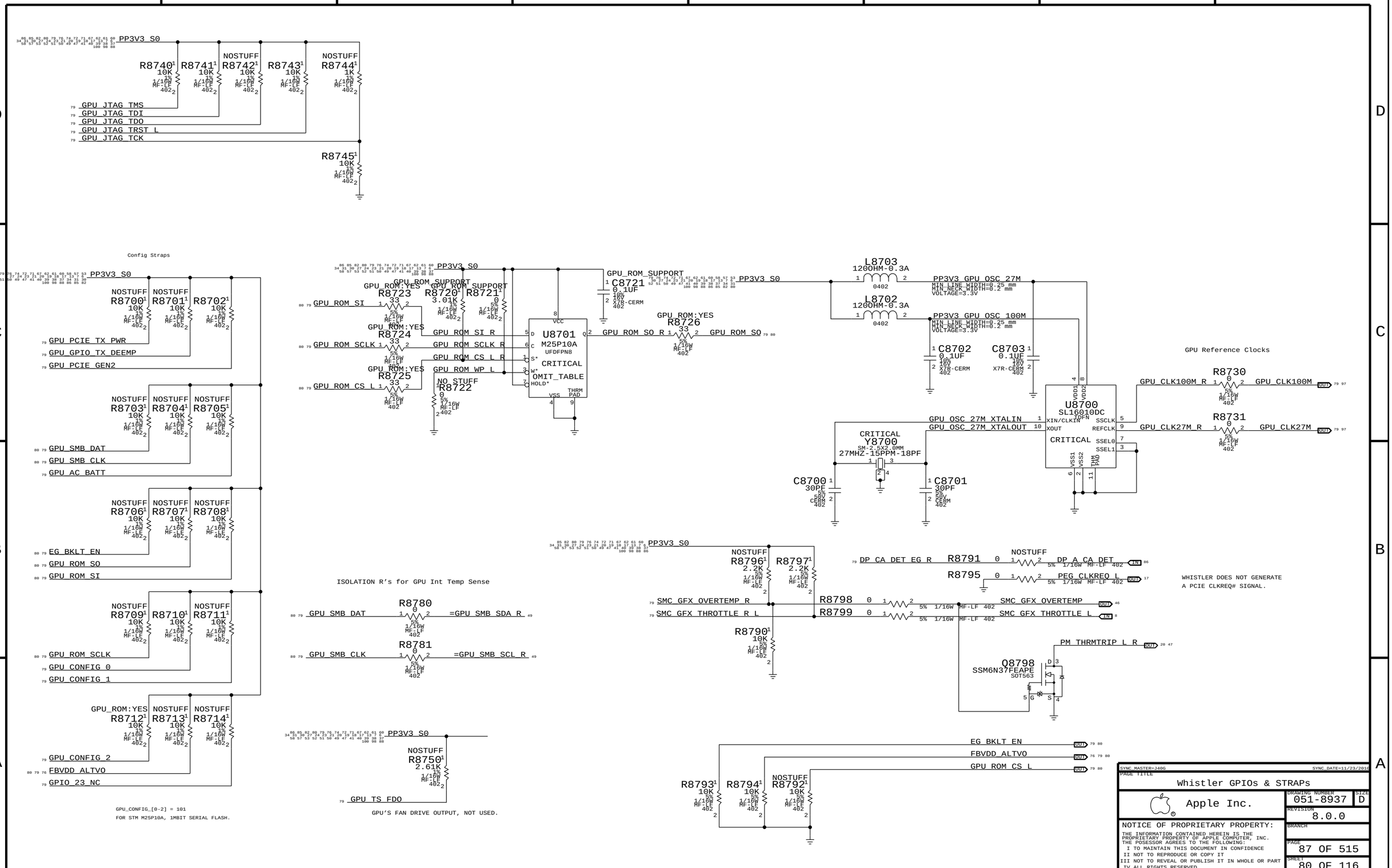
PP3V3_S0
R8740 10K 1% 1/16W MF-LF 402
R8741 10K 1% 1/16W MF-LF 402
NOSTUFF R8742 10K 1% 1/16W MF-LF 402
R8743 10K 1% 1/16W MF-LF 402
NOSTUFF R8744 1K 1% 1/16W MF-LF 402
R8745 10K 1% 1/16W MF-LF 402
GPU_JTAG_TMS
GPU_JTAG_TDI
GPU_JTAG_TDO
GPU_JTAG_TRST_L
GPU_JTAG_TCK
Config Straps
NOSTUFF R8700 10K 1% 1/16W MF-LF 402
NOSTUFF R8701 10K 1% 1/16W MF-LF 402
R8702 10K 1% 1/16W MF-LF 402
GPU_PCIE_TX_PWR
GPU_GPIO_TX_DEEMP
GPU_PCIE_GEN2
NOSTUFF R8703 10K 1% 1/16W MF-LF 402
NOSTUFF R8704 10K 1% 1/16W MF-LF 402
NOSTUFF R8705 10K 1% 1/16W MF-LF 402
GPU_SMB_DAT
GPU_SMB_CLK
GPU_AC_BATT
NOSTUFF R8706 10K 1% 1/16W MF-LF 402
NOSTUFF R8707 10K 1% 1/16W MF-LF 402
NOSTUFF R8708 10K 1% 1/16W MF-LF 402
EG_BKLT_EN
GPU_ROM_SO
GPU_ROM_SI
NOSTUFF R8709 10K 1% 1/16W MF-LF 402
R8710 10K 1% 1/16W MF-LF 402
NOSTUFF R8711 10K 1% 1/16W MF-LF 402
GPU_ROM_SCLK
GPU_CONFIG_0
GPU_CONFIG_1
GPU_ROM:YES R8712 10K 1% 1/16W MF-LF 402
NOSTUFF R8713 10K 1% 1/16W MF-LF 402
NOSTUFF R8714 10K 1% 1/16W MF-LF 402
GPU_CONFIG_2
FBVDD_ALTVO
GPIO_23_NC
GPU_CONFIG_[0-2] = 101
FOR STM M25P10A, 1MBIT SERIAL FLASH.
GPU_ROM_SUPPORT
GPU_ROM:YES R8723 33 5% 1/16W MF-LF 402
GPU_ROM_SUPPORT R8720 3.01K 1% 1/16W MF-LF 402
R8721 0 5% 1/16W MF-LF 402
GPU_ROM_SI
GPU_ROM:YES R8724 33 5% 1/16W MF-LF 402
GPU_ROM_SCLK
GPU_ROM:YES R8725 33 5% 1/16W MF-LF 402
GPU_ROM_CS_L
NO STUFF R8722 0 5% 1/16W MF-LF 402
GPU_ROM_SI_R
GPU_ROM_SCLK_R
GPU_ROM_CS_L_R
GPU_ROM_WP_L
U8701 M25P10A UFDFPN8 CRITICAL OMIT_TABLE
VCC
VSS
THRM PAD
C8721 0.1UF 10% 16V X7R-CERM 402
GPU_ROM_SUPPORT
GPU_ROM:YES R8726 33 5% 1/16W MF-LF 402
GPU_ROM_SO_R
GPU_ROM_SO
L8703 1200HM-0.3A 0402
L8702 1200HM-0.3A 0402
PP3V3_GPU_OSC_27M
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
PP3V3_GPU_OSC_100M
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
C8702 0.1UF 10% 16V X7R-CERM 402
C8703 0.1UF 10% 16V X7R-CERM 402
GPU Reference Clocks
U8700 SL16010DC TDFN CRITICAL
VDD1
VDD2
XIN/CLKIN
XOUT
SSCLK
REFCLK
SSEL0
SSEL1
VSS1
VSS2
THM PAD
GPU_CLK100M_R
R8730 0 5% 1/16W MF-LF 402
GPU_CLK100M
GPU_CLK27M_R
R8731 0 5% 1/16W MF-LF 402
GPU_CLK27M
GPU_OSC_27M_XTALIN
GPU_OSC_27M_XTALOUT
CRITICAL Y8700 SM-2.5X2.0MM 27MHZ-15PPM-18PF
C8700 30PF 5% 50V CERM 402
C8701 30PF 5% 50V CERM 402
ISOLATION R's for GPU Int Temp Sense
GPU_SMB_DAT
R8780 0 5% 1/16W MF-LF 402
=GPU_SMB_SDA_R
GPU_SMB_CLK
R8781 0 5% 1/16W MF-LF 402
=GPU_SMB_SCL_R
PP3V3_S0
NOSTUFF R8750 2.61K 1% 1/16W MF-LF 402
GPU_TS_FDO
GPU'S FAN DRIVE OUTPUT, NOT USED.
NOSTUFF R8796 2.2K 5% 1/16W MF-LF 402
R8797 2.2K 5% 1/16W MF-LF 402
DP_CA_DET_EG_R
R8791 0 5% 1/16W MF-LF 402
NOSTUFF
DP_A_CA_DET
R8795 0 5% 1/16W MF-LF 402
PEG_CLKREQ_L
WHISTLER DOES NOT GENERATE
A PCIE CLKREQ# SIGNAL.
SMC_GFX_OVERTEMP_R
SMC_GFX_THROTTLE_R_L
R8798 0 5% 1/16W MF-LF 402
SMC_GFX_OVERTEMP
R8799 0 5% 1/16W MF-LF 402
SMC_GFX_THROTTLE_L
R8790 10K 5% 1/16W MF-LF 402
PM_THRMTRIP_L_R
Q8798 SSM6N37FEAPE SOT563
EG_BKLT_EN
FBVDD_ALTVO
GPU_ROM_CS_L
R8793 10K 5% 1/16W MF-LF 402
R8794 10K 5% 1/16W MF-LF 402
NOSTUFF R8792 10K 5% 1/16W MF-LF 402
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SYNC_DATE=11/23/2010
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Whistler GPIOs & STRAPs
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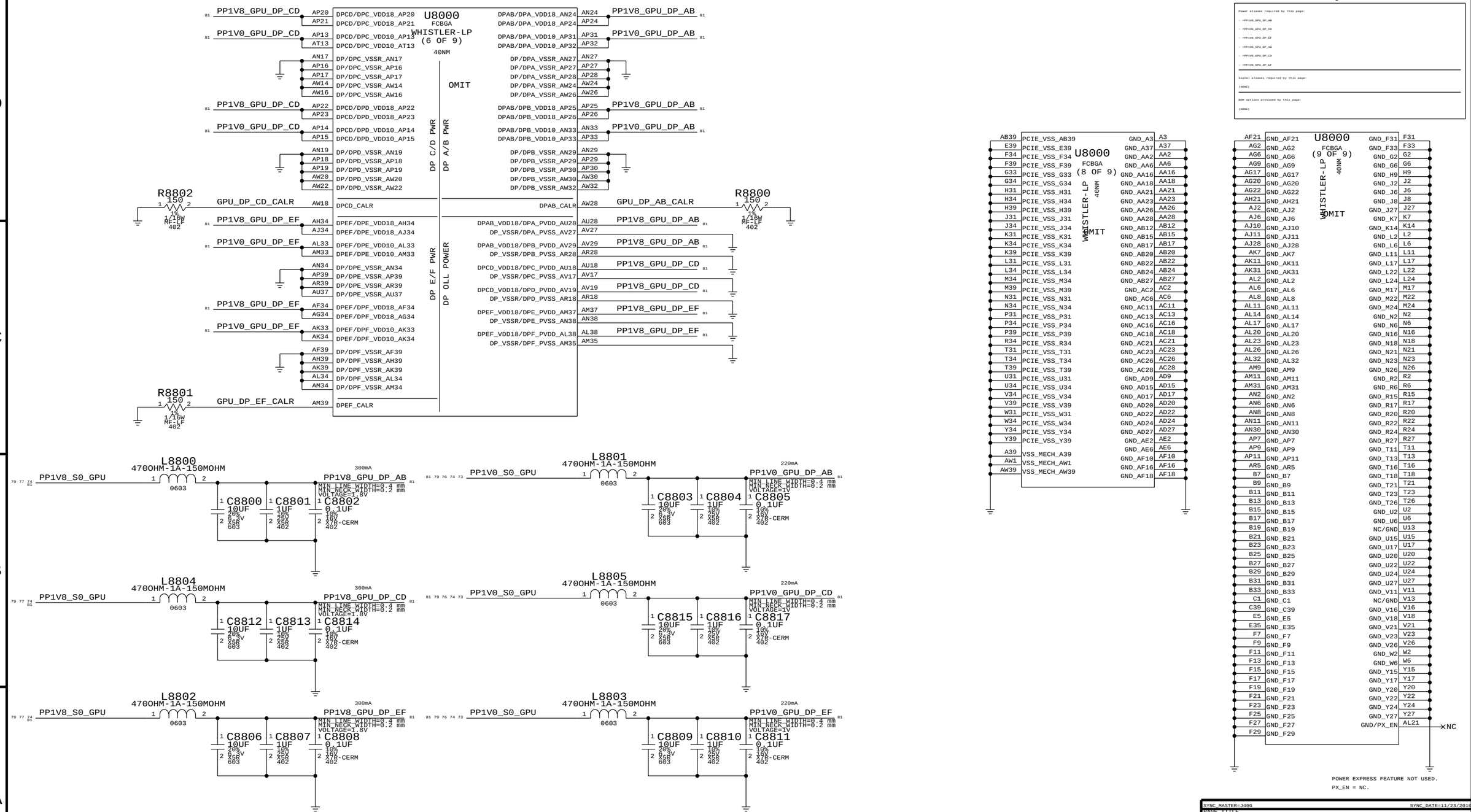

POWER EXPRESS FEATURE NOT USED.
PX_EN = NC.

Page Notes

Power aliases required by this page:

- =PP1V8_GPU_DP_AB
- =PP1V0_GPU_DP_CD
- =PP1V8_GPU_DP_EF
- =PP1V8_GPU_DP_AB
- =PP1V0_GPU_DP_CD
- =PP1V8_GPU_DP_EF

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

SYNC_MASTER=J40G SYNC_DATE=11/23/2010

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Whistler DP PWR/GNDs

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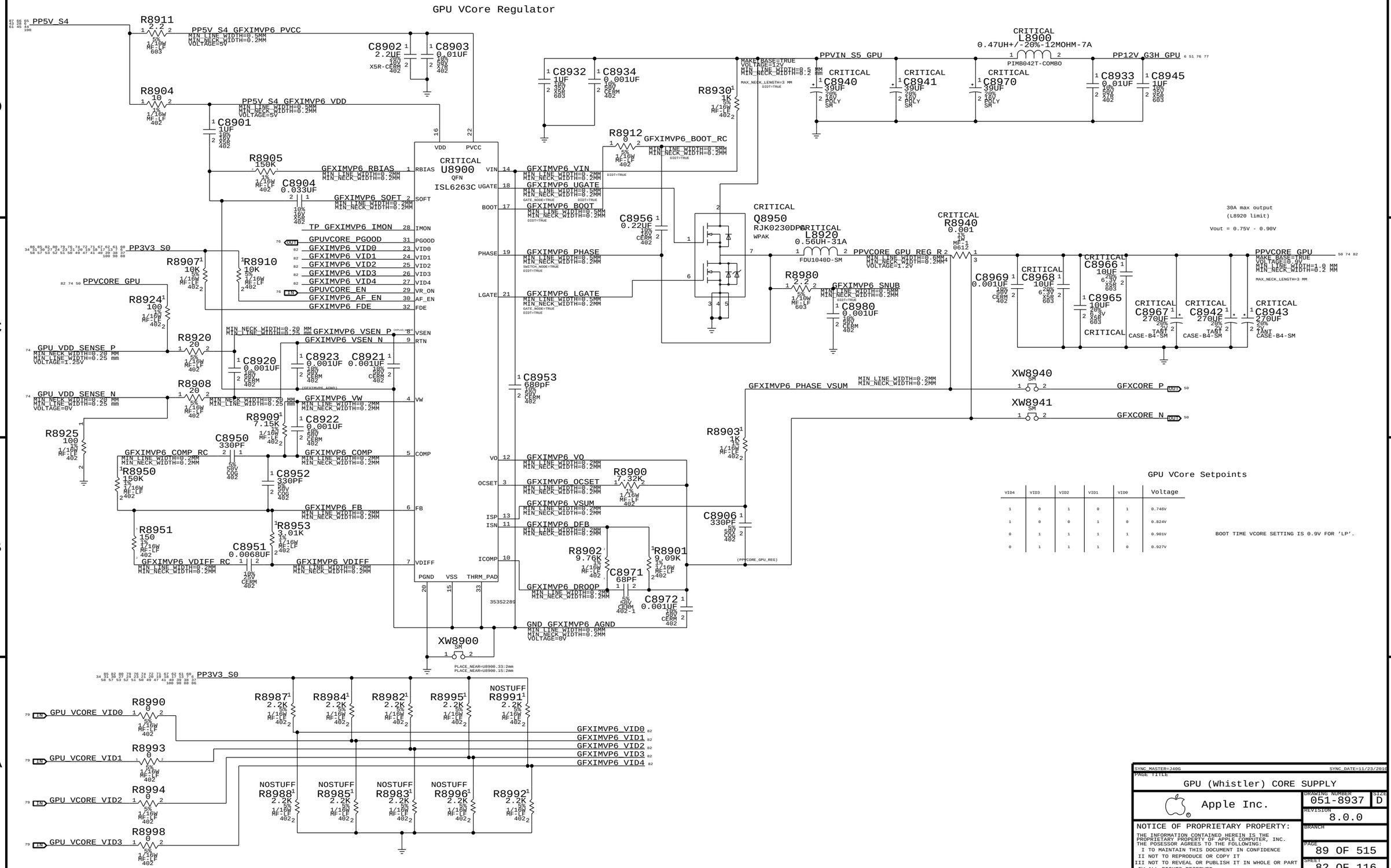

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GPU (Whistler) CORE SUPPLY

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CRITICAL
OMIT_TABLE
U9000
T29
FCBGA
(SYM 1 OF 2)

PCIE GEN2

RECEIVE

PCIE T29 R2D C P<0>	C9000 0.1UF	PCIE T29 R2D P<0>	V19 PER_0_P
PCIE T29 R2D C N<0>	C9001 0.1UF	PCIE T29 R2D N<0>	T19 PER_0_N
PCIE T29 R2D C P<1>	C9002 0.1UF	PCIE T29 R2D P<1>	P19 PER_1_P
PCIE T29 R2D C N<1>	C9003 0.1UF	PCIE T29 R2D N<1>	M19 PER_1_N
PCIE T29 R2D C P<2>	C9004 0.1UF	PCIE T29 R2D P<2>	K19 PER_2_P
PCIE T29 R2D C N<2>	C9005 0.1UF	PCIE T29 R2D N<2>	H19 PER_2_N
PCIE T29 R2D C P<3>	C9006 0.1UF	PCIE T29 R2D P<3>	F19 PER_3_P
PCIE T29 R2D C N<3>	C9007 0.1UF	PCIE T29 R2D N<3>	D19 PER_3_N

TRANSMIT

V21 PET_0_P	PCIE T29 D2R C P<0>	C9040 0.1UF	PCIE T29 D2R P<0>
T21 PET_0_N	PCIE T29 D2R C N<0>	C9041 0.1UF	PCIE T29 D2R N<0>
P21 PET_1_P	PCIE T29 D2R C P<1>	C9042 0.1UF	PCIE T29 D2R P<1>
M21 PET_1_N	PCIE T29 D2R C N<1>	C9043 0.1UF	PCIE T29 D2R N<1>
K21 PET_2_P	PCIE T29 D2R C P<2>	C9044 0.1UF	PCIE T29 D2R P<2>
H21 PET_2_N	PCIE T29 D2R C N<2>	C9045 0.1UF	PCIE T29 D2R N<2>
F21 PET_3_P	PCIE T29 D2R C P<3>	C9046 0.1UF	PCIE T29 D2R P<3>
D21 PET_3_N	PCIE T29 D2R C N<3>	C9047 0.1UF	PCIE T29 D2R N<3>

NO STUFF
TP T29 MONDC0 R9010 0 5% 1/16W MF-LF 402 T29 MONDC0 B21 MONDC0

DEBUG: For monitoring current/voltage
TP T29 MONDC1 R9011 0 5% 1/16W MF-LF 402 T29 MONDC1 A20 MONDC1

NO STUFF
TP T29 MONOBSP C9015 0.1UF T29 MONOBSP K17 MONOBSP

DEBUG: For monitoring clock
TP T29 MONOBSN C9016 0.1UF T29 MONOBSN M17 MONOBSN

WAKE* F1 T29 PCIE WAKE L R9051 10K 5% 1/16W MF-LF 402 PP3V3_T29
PERST* E6 T29 RESET L
RSENSE E14 T29 RSENSE R9055 1.0K 0.5% 1/16W MF-LF 603
RBIAS E16 T29 RBIAS

MISC

CLK REQUEST

T29 CLKREQ ISOL L	P3	PCIE_CLKREQ_0*
T29 GPIO<1>	N4	PCIE_CLKREQ_1*
T29 GPIO<2>	M3	PCIE_CLKREQ_2*
T29 RSVD	L4	PCIE_CLKREQ_3*

EEPROM

T29 SPI MOSI	P1	EE_DI
T29 SPI MISO	M1	EE_DO
T29 SPI CS L	N2	EE_CS*
T29 SPI CLK	L2	EE_CLK

TP T29 THERMDP A2 THERM_DP
Use B1 GND ball for THERM_DN

TEST PORT

T29 TEST EN	E4	TEST_EN
TP T29 TEST POINT 0	P5	TEST_POINT_0
TP T29 TEST POINT 1	N6	TEST_POINT_1
TP T29 TEST POINT 2	M5	TEST_POINT_2
T29 TEST POINT 3	L6	TEST_POINT_3

POWER ON RESET

PCIE_RST_0*	K1	NC T29 PCIE RESET0 L
PCIE_RST_1*	J2	NC T29 PCIE RESET1 L
PCIE_RST_2*	K3	NC T29 PCIE RESET2 L
PCIE_RST_3*	J4	NC T29 PCIE RESET3 L

Not used in host mode.

JTAG

TDI	T3	JTAG ISP TDI
TMS	R4	JTAG T29 TMS
TCK	R2	JTAG ISP TCK
TDO	T1	JTAG ISP TDO

CLOCKS

REFCLK_100_IN_P	H17	PCIE CLK100M T29 P
REFCLK_100_IN_N	G16	PCIE CLK100M T29 N
XTAL_25_IN	P17	SYSCLK CLK25M T29 R
XTAL_25_OUT	R16	TP T29 XTAL25OUT
TMU_CLK_OUT	U2	T29 TMU CLK OUT
TMU_CLK_IN	E2	T29 TMU CLK IN

PP3V3_T29
R9098 10K 5% 1/16W MF-LF 402
R9095 806 1% 1/16W MF-LF 402 SYSCLK_CLK25M_T29
R9096 1K 5% 1/16W MF-LF 402
NO STUFF R9099 10K 5% 1/16W MF-LF 402

DISPLAY

SINK PORT 0

DP T29SNK0 ML P<3>	AA4	DPSNK0_ML_LANE_3P
DP T29SNK0 ML N<3>	Y3	DPSNK0_ML_LANE_3N
DP T29SNK0 ML P<2>	AA6	DPSNK0_ML_LANE_2P
DP T29SNK0 ML N<2>	Y5	DPSNK0_ML_LANE_2N
DP T29SNK0 ML P<1>	AA8	DPSNK0_ML_LANE_1P
DP T29SNK0 ML N<1>	Y7	DPSNK0_ML_LANE_1N
DP T29SNK0 ML P<0>	AA10	DPSNK0_ML_LANE_0P
DP T29SNK0 ML N<0>	Y9	DPSNK0_ML_LANE_0N
DP T29SNK0 AUXCH P	V1	DPSNK0_AUX_CHP
DP T29SNK0 AUXCH N	W2	DPSNK0_AUX_CHN
DP T29SNK0 HPD	V5	DPSNK0_HOT_PLUG_DET

R9025 0 5% 1/16W MF-LF 402
R9029 0 5% 1/16W MF-LF 402
R9030 100K 5% 1/16W MF-LF 402

SINK PORT 1

DP T29SNK1 ML P<3>	V9	DPSNK1_ML_LANE_3P
DP T29SNK1 ML N<3>	U8	DPSNK1_ML_LANE_3N
DP T29SNK1 ML P<2>	V11	DPSNK1_ML_LANE_2P
DP T29SNK1 ML N<2>	U10	DPSNK1_ML_LANE_2N
DP T29SNK1 ML P<1>	V13	DPSNK1_ML_LANE_1P
DP T29SNK1 ML N<1>	U12	DPSNK1_ML_LANE_1N
DP T29SNK1 ML P<0>	V15	DPSNK1_ML_LANE_0P
DP T29SNK1 ML N<0>	U14	DPSNK1_ML_LANE_0N
DP T29SNK1 AUXCH P	V7	DPSNK1_AUX_CHP
DP T29SNK1 AUXCH N	U6	DPSNK1_AUX_CHN
DP T29SNK1 HPD	U4	DPSNK1_HOT_PLUG_DET

R9031 100K 5% 1/16W MF-LF 402

SOURCE PORT 0

DPSRC0_ML_LANE_3P	AA18	NC DP T29SRC ML CP<3>
DPSRC0_ML_LANE_3N	Y17	NC DP T29SRC ML CN<3>
DPSRC0_ML_LANE_2P	AA16	NC DP T29SRC ML CP<2>
DPSRC0_ML_LANE_2N	Y15	NC DP T29SRC ML CN<2>
DPSRC0_ML_LANE_1P	AA14	NC DP T29SRC ML CP<1>
DPSRC0_ML_LANE_1N	Y13	NC DP T29SRC ML CN<1>
DPSRC0_ML_LANE_0P	AA12	NC DP T29SRC ML CP<0>
DPSRC0_ML_LANE_0N	Y11	NC DP T29SRC ML CN<0>
DPSRC0_AUX_CHP	W16	NC DP T29SRC AUXCH CP
DPSRC0_AUX_CHN	U16	NC DP T29SRC AUXCH CN
DPSRC0_HOT_PLUG_DET	V3	PD DP T29SRC HPD
DP_ATEST	Y19	T29 DP ATEST
DP_RES_0	Y21	
DP_RES_1	AA20	T29 DP RES

100pF SRF > 40MHz
BYPASS=U9000.Y19::2MM
BYPASS=U9000.Y19::5.08MM
C9085 100PF 5% 50V C0G 402 C9086 0.01UF 10% 50V X7R 402
R9085 14.0K 1% 1/16W MF-LF 402 R9032 100K 5% 1/16W MF-LF 402

PORTS

PORT0

NC T29 R2D CP0	A6	PRT0_T29T_P
NC T29 R2D CN0	A4	PRT0_T29T_N
NC T29 D2RP0	C4	PRT0_T29R_P
NC T29 D2RN0	C2	PRT0_T29R_N
T29 LSEO LSOE0	J6	T29_0_LSEO
	K5	T29_0_LSOE

PORT1

NC T29 R2D CP1	A10	PRT1_T29T_P
NC T29 R2D CN1	A8	PRT1_T29T_N
NC T29 D2RP1	C8	PRT1_T29R_P
NC T29 D2RN1	C6	PRT1_T29R_N
T29 LSEO LSOE1	G6	T29_1_LSEO
	H5	T29_1_LSOE

I2C T29 SDA	F3	T29_SDA
I2C T29 SCL	F5	T29_SCL

PORT2

PRT2_T29T_P	A14	T29 R2D C P<0>
PRT2_T29T_N	A12	T29 R2D C N<0>
PRT2_T29R_P	C12	T29 D2R P<0>
PRT2_T29R_N	C10	T29 D2R N<0>
T29_2_LSEO	G4	T29 LSEO<0>
T29_2_LSOE	H3	T29 LSOE<0>

PORT3

PRT3_T29T_P	A18	T29 R2D C P<1>
PRT3_T29T_N	A16	T29 R2D C N<1>
PRT3_T29R_P	C16	T29 D2R P<1>
PRT3_T29R_N	C14	T29 D2R N<1>
T29_3_LSEO	G2	T29 LSEO<1>
T29_3_LSOE	H1	T29 LSOE<1>

NOTE: All unused LSOE/EO pairs should be aliased together. Other signals okay to float (TP/NC).

CRITICAL
OMIT_TABLE
U9090
M95320-RMB6TG
MLP

T29 SPI MOSI	D	
T29 SPI CLK	C	
T29 SPI CS L	S_L	
T29ROM WP L	W_L	
T29ROM HOLD L	HOLD_L	
	Q	T29 SPI MISO
	VCC	PP3V3_T29
	VSS, THM PAD	

R9090 3.3K 5% 1/16W MF-LF 402
R9091 3.3K 5% 1/16W MF-LF 402
C9090 1UF 10% 10V X5R 402-1
R9092 3.3K 5% 1/16W MF-LF 402
R9093 3.3K 5% 1/16W MF-LF 402
R9023 10K 5% 1/16W MF-LF 402
R9022 10K 5% 1/16W MF-LF 402
R9021 10K 5% 1/16W MF-LF 402

SNK0 AC Coupling

DP T29SNK0 ML C P<0>	C9020 0.1UF	DP T29SNK0 ML P<0>
DP T29SNK0 ML C N<0>	C9021 0.1UF	DP T29SNK0 ML N<0>
DP T29SNK0 ML C P<1>	C9022 0.1UF	DP T29SNK0 ML P<1>
DP T29SNK0 ML C N<1>	C9023 0.1UF	DP T29SNK0 ML N<1>
DP T29SNK0 ML C P<2>	C9024 0.1UF	DP T29SNK0 ML P<2>
DP T29SNK0 ML C N<2>	C9025 0.1UF	DP T29SNK0 ML N<2>
DP T29SNK0 ML C P<3>	C9026 0.1UF	DP T29SNK0 ML P<3>
DP T29SNK0 ML C N<3>	C9027 0.1UF	DP T29SNK0 ML N<3>
DP T29SNK0 AUXCH C P	C9028 0.1UF	DP T29SNK0 AUXCH P
DP T29SNK0 AUXCH C N	C9029 0.1UF	DP T29SNK0 AUXCH N

SNK1 AC COUPLING

DP T29SNK1 ML C P<0>	C9030 0.1UF	DP T29SNK1 ML P<0>
DP T29SNK1 ML C N<0>	C9031 0.1UF	DP T29SNK1 ML N<0>
DP T29SNK1 ML C P<1>	C9032 0.1UF	DP T29SNK1 ML P<1>
DP T29SNK1 ML C N<1>	C9033 0.1UF	DP T29SNK1 ML N<1>
DP T29SNK1 ML C P<2>	C9034 0.1UF	DP T29SNK1 ML P<2>
DP T29SNK1 ML C N<2>	C9035 0.1UF	DP T29SNK1 ML N<2>
DP T29SNK1 ML C P<3>	C9036 0.1UF	DP T29SNK1 ML P<3>
DP T29SNK1 ML C N<3>	C9037 0.1UF	DP T29SNK1 ML N<3>
DP T29SNK1 AUXCH C P	C9038 0.1UF	DP T29SNK1 AUXCH P
DP T29SNK1 AUXCH C N	C9039 0.1UF	DP T29SNK1 AUXCH N

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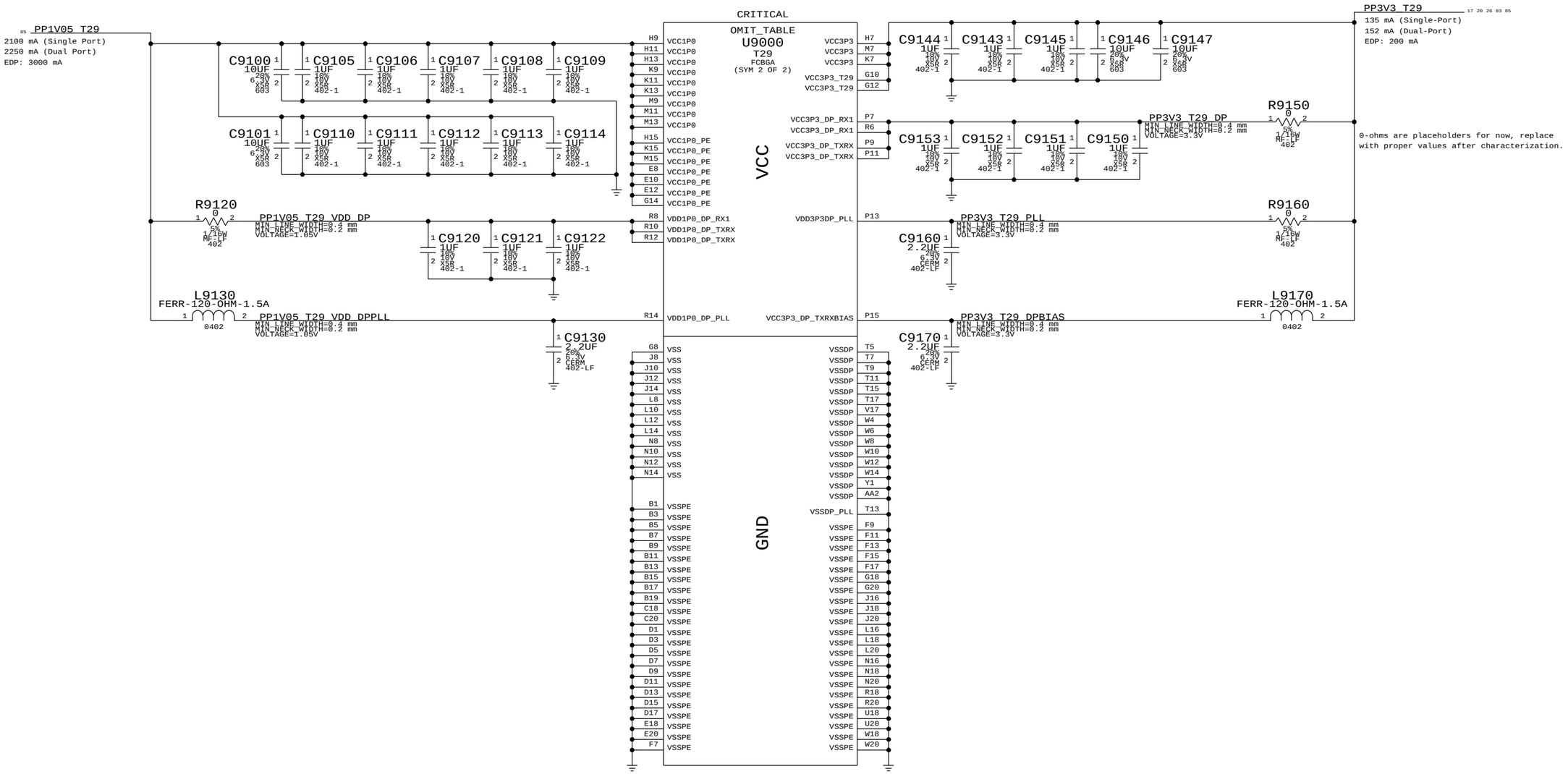

Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC_MASTER=J40S SYNC_DATE=11/23/2010

PAGE TITLE: T29 Host (2 of 2)

Apple Inc.

DRAWING NUMBER: 051-8937 SIZE: D

REVISION: 8.0.0

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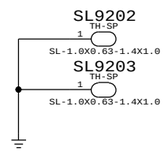
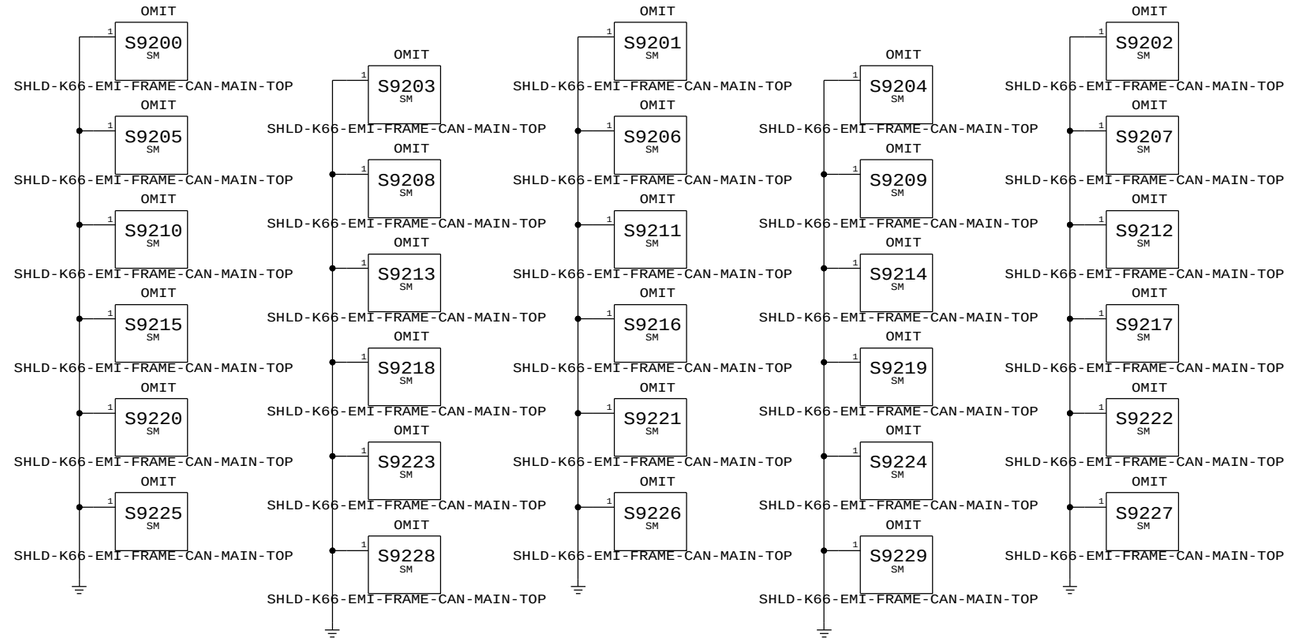
Page Notes

Power aliases required by this page:
- =PPVIN_SW_T29BST (8-13V Boost Input)
- =PP18V_T29_REG (18V Boost Output)
- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

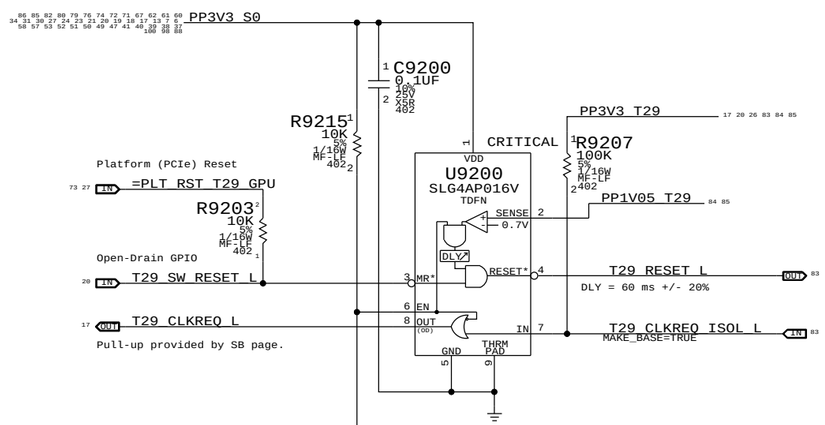
Signal aliases required by this page:
- =T29_CLKREQ_L
- =T29_RESET_L

BOM options provided by this page:
T29BST:Y - Stuffs 18V boost circuitry.

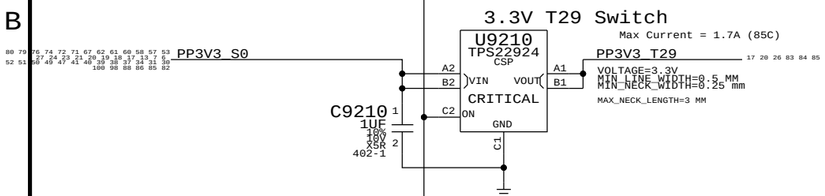




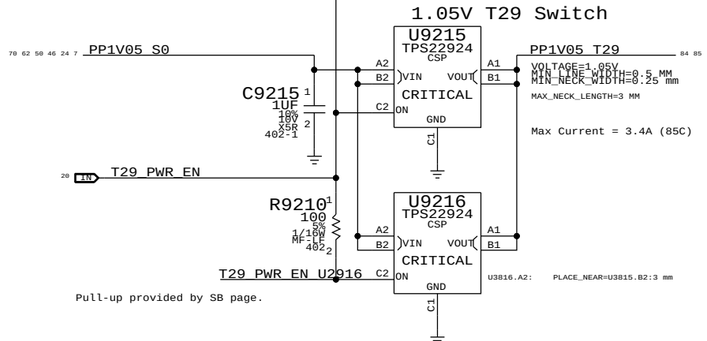
Supervisor & CLKREQ# Isolation



3.3V T29 Switch



1.05V T29 Switch



U9210 & U9215/U9216

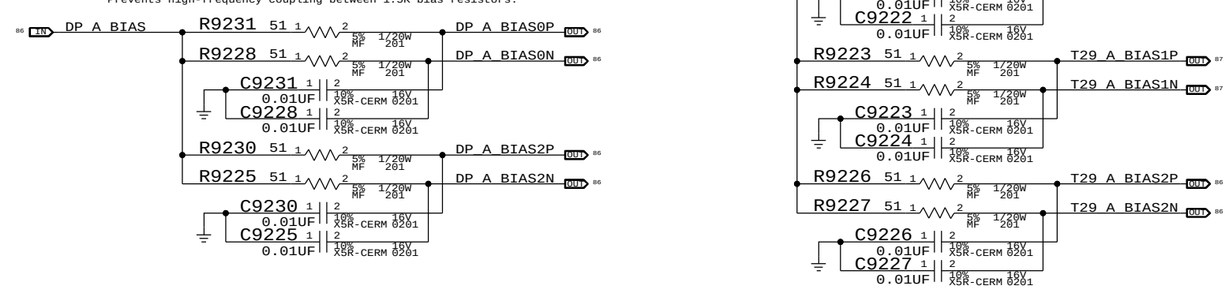
Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A per IC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-2254	1	FRAME,EMI SHIELD,TB,J40	SH9200	CRITICAL	?

DP/T29 Bias Filters

Prevents high-frequency coupling between 1.5K bias resistors.



SYNC_MASTER=J40S SYNC_DATE=11/23/2016

PAGE TITLE: T29 Power Support

Apple Inc.

DRAWING NUMBER: 051-8937 SIZE: D

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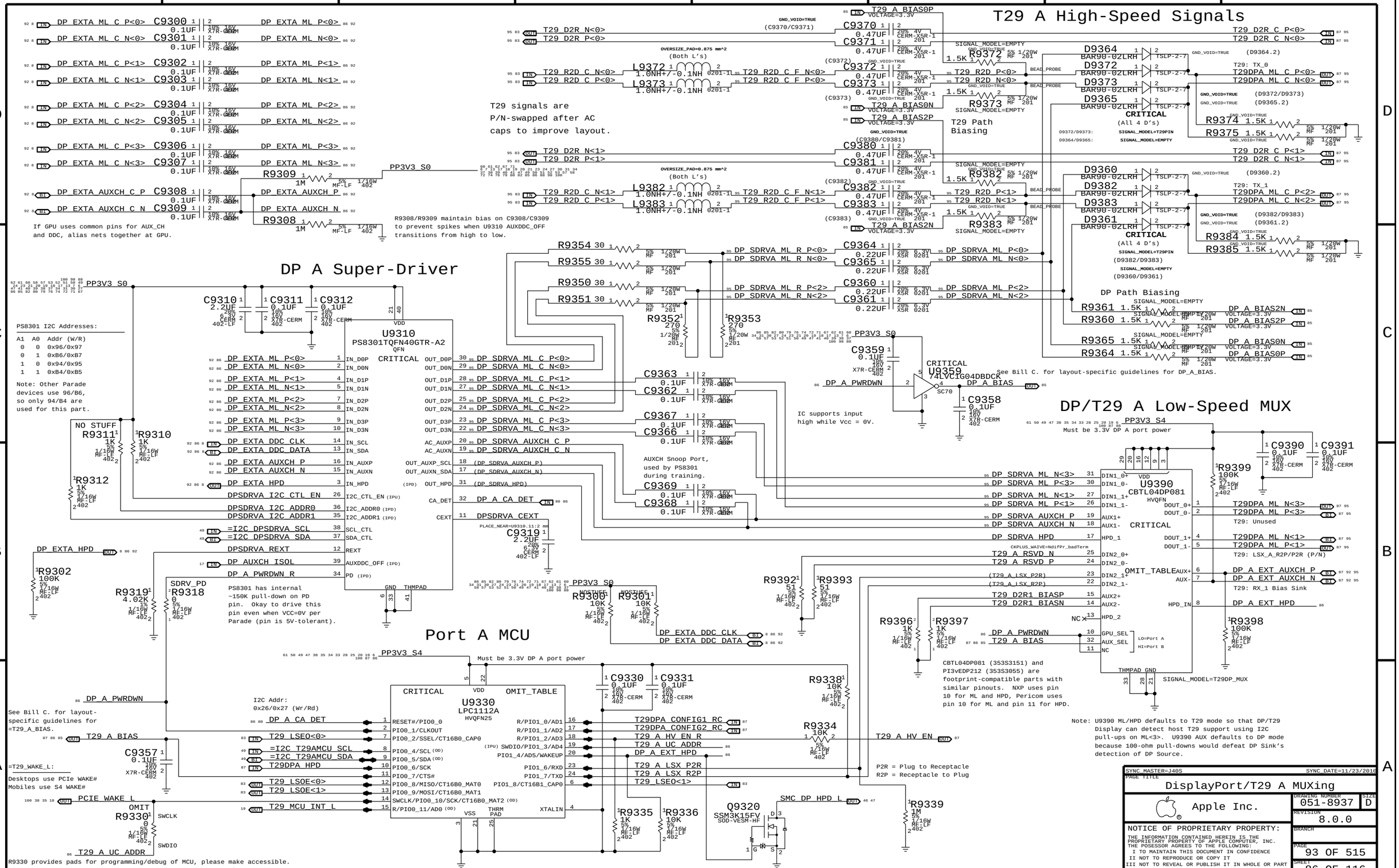
T29 A High-Speed Signals
DP A Super-Driver
DP/T29 A Low-Speed MUX
Port A MCU
T29 signals are P/N-swapped after AC caps to improve layout.
T29 Path Biasing
DP Path Biasing
If GPU uses common pins for AUX_CH and DDC, alias nets together at GPU.
R9308/R9309 maintain bias on C9308/C9309 to prevent spikes when U9310 AUXDDC_OFF transitions from high to low.
PS8301 I2C Addresses:
A1 A0 Addr (W/R)
0 0 0x96/0x97
0 1 0xB6/0xB7
1 0 0x94/0x95
1 1 0xB4/0xB5
Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.
U9310
PS8301TQFN40GTR-A2
QFN
U9359
74LVC1G04DBDCK
SC70
See Bill C. for layout-specific guidelines for DP_A_BIAS.
IC supports input high while Vcc = 0V.
AUXCH Snoop Port, used by PS8301 during training.
U9390
CBTL04DP081
HVQFN
Must be 3.3V DP A port power
T29: Unused
T29: LSX_A_R2P/P2R (P/N)
T29: RX_1 Bias Sink
CBTL04DP081 (353S3151) and PI3vEDP212 (353S3055) are footprint-compatible parts with similar pinouts. NXP uses pin 10 for ML and HPD, Pericom uses pin 10 for ML and pin 11 for HPD.
Note: U9390 ML/HPD defaults to T29 mode so that DP/T29 Display can detect host T29 support using I2C pull-ups on ML<3>. U9390 AUX defaults to DP mode because 100-ohm pull-downs would defeat DP Sink's detection of DP Source.
U9330
LPC1112A
HVQFN25
See Bill C. for layout-specific guidelines for =T29_A_BIAS.
Desktops use PCIe WAKE# Mobiles use S4 WAKE#
R9330 provides pads for programming/debug of MCU, please make accessible. If project has space for 10-pin programming header it should be used.
P2R = Plug to Receptacle
R2P = Receptacle to Plug
Q9320
SSM3K15FV
SOD-VESM-HF
SYNC_MASTER=J40S
SYNC_DATE=11/23/2010
PAGE TITLE
DisplayPort/T29 A MUXing
Apple Inc.
DRAWING NUMBER
051-8937
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3V3(DP)/2V9(T29) PORTA SUPPLY

12V T29 PORTA SUPPLY

	Nominal	Min	Max
IFLT	885mA	876mA	894mA (*)
ILIM	935mA	925mA	944mA (*)
TFLT	18.3ms	13.4ms	26.7ms
TSD	470ms	235ms	724ms

(*) U9410 tolerance unknown

12 VOLTS
12 WATTS MAX PER PORT

VO=0.5*(1+ RA/RB)
VO=0.5*(1+ 1.18K/249)=2.87V

IFLT = 200k / RFLT = 885mA
ILIM = 201k / RLIM = 935mA
TFLT = CCT * 38900
TSD = CCT * 100000

DisplayPort/T29 A Connector

Circuit threshold range: 2.877-2.941V (2.903V nominal)

470k R's for ESD protection on AC-coupled signals.

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

514-0XXX

SYNC_MASTER=J40G	SYNC_DATE=12/01/2010
PAGE TITLE	DisplayPort/T29 A Connector
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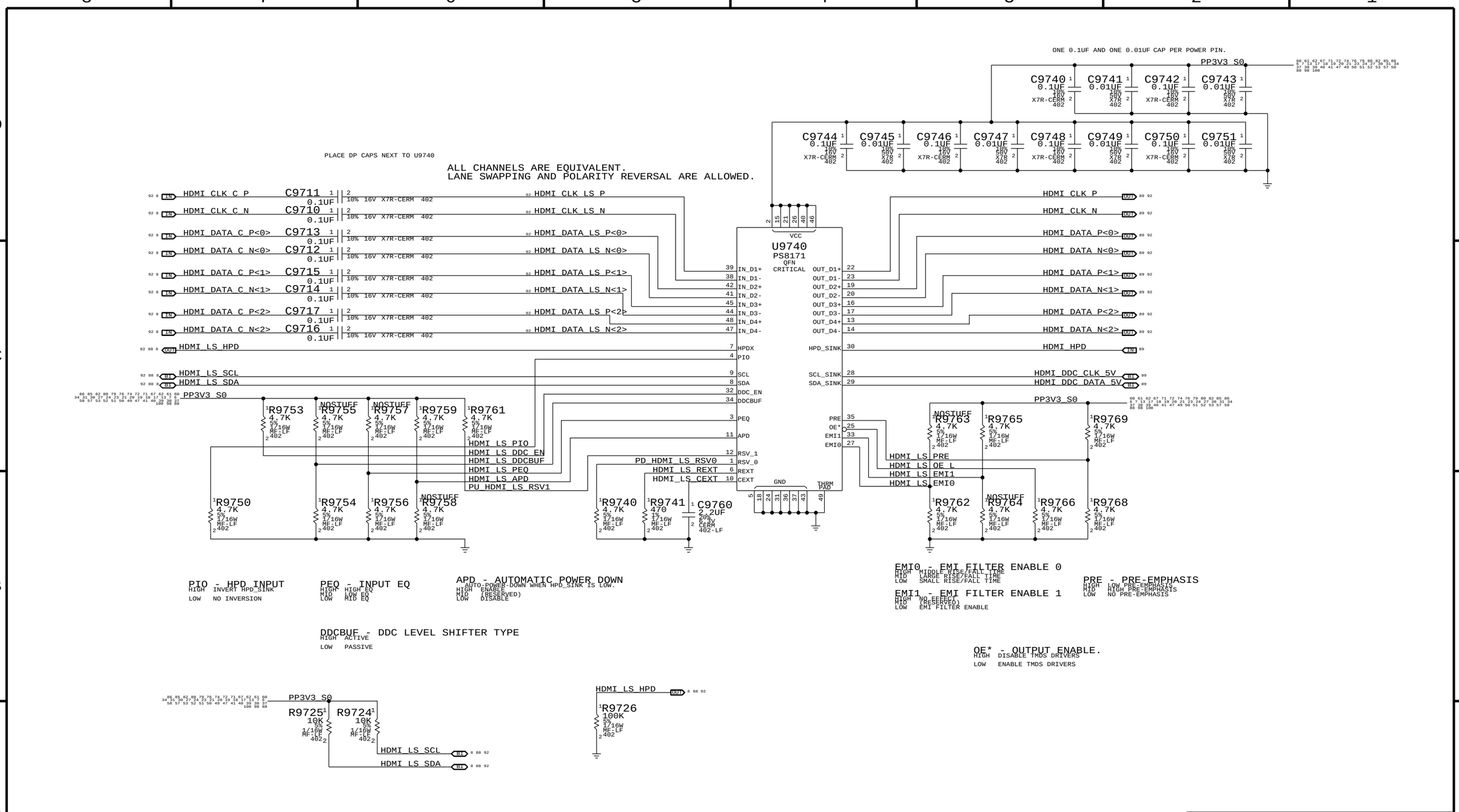

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE

HDMI SHIFTER

Apple Inc.

DRAWING NUMBER 051-8937 SIZE D

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HDMI CONNECTOR

PLACE NEAR J9430 CONNECTOR

CRITICAL
L9890
90-OHM-300MA
ACM2012H
SYM_VER-2

HDMI DATA P<0> — HDMI DATA CONN P<0>
HDMI DATA N<0> — HDMI DATA CONN N<0>

CRITICAL
D9811
RCLAMP0524P
SLP2510P8

CRITICAL
D9810
RCLAMP0524P
SLP2510P8

CRITICAL
L9891
90-OHM-300MA
ACM2012H
SYM_VER-2

HDMI DATA P<1> — HDMI DATA CONN P<1>
HDMI DATA N<1> — HDMI DATA CONN N<1>

CRITICAL
L9892
90-OHM-300MA
ACM2012H
SYM_VER-2

HDMI DATA P<2> — HDMI DATA CONN P<2>
HDMI DATA N<2> — HDMI DATA CONN N<2>

CRITICAL
D9810
RCLAMP0524P
SLP2510P8

CRITICAL
D9811
RCLAMP0524P
SLP2510P8

CRITICAL
L9893
360-OHM-0.100MA
ACM2012-SM
SYM_VER-2

HDMI CLK P — HDMI CLK CONN P
HDMI CLK N — HDMI CLK CONN N

(0.055A TO 0.5A LIMITS PER HDMI SPEC.)

PP5V S0

C9800 22UF 20% 6.3V X5R-CERM 603

C9802 0.1UF 10% 16V X7R-CERM 402

CRITICAL
U9800
TPS2051B
SOT23
IN, OUT, EN, OC*, GND

PP5V_HDMI_DDC_FUSE
VOLTAGE=5V
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM

NC_HD_OC
NO_TEST=TRUE

C9803 10UF 20% 6.3V X5R 603

CRITICAL
L9830
400-OHM-EMI
VOLTAGE=5V
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
SM-1

C9830 0.01UF 20% 50V CERM 603

J9830
HDMI-PLASTIC-J40
F-RT-SM

Pin	Signal	Pin	Signal
1	TMDS_DATA2_P	2	TMDS_DATA2_SHLD1
3	TMDS_DATA2_M	4	TMDS_DATA1_P
5	TMDS_DATA1_SHLD1	6	TMDS_DATA1_M
7	TMDS_DATA0_P	8	TMDS_DATA0_SHLD1
9	TMDS_DATA0_M	10	TMDS_CLK_P
11	TMDS_CLK_SHLD	12	TMDS_CLK_M
13	CEC	14	RSRVD
15	SCL	16	SDA
17	DDC_CED_GND	18	P_5V_PWR
19	HOT_PLUG_DETECT		
20–34 (even)	IO20–IO34	21–33 (odd)	IO21–IO33

CRITICAL
SHLD PINS

HDMI DATA CONN P<2>
HDMI DATA CONN N<2>
HDMI DATA CONN P<0>
HDMI DATA CONN N<0>
TP_HDMI_CEC_CONN
HDMI DDC CLK CONN
HDMI HPD CONN

HDMI DATA CONN P<1>
HDMI DATA CONN N<1>
HDMI CLK CONN P
HDMI CLK CONN N
HDMI DDC DATA CONN
PP5V HDMI DDC CONN

CRITICAL
D9800
RCLAMP0504F
SC70-6-1

PLACE CAPS CLOSE
TO HDMI CONNECTOR

PP5V HDMI DDC CONN

PP5V HDMI DDC FUSE

R9810 4.7K 5% 1/16W MF-LF 402

R9812 4.7K 5% 1/16W MF-LF 402

C9810 0.01UF 10% 50V X7R 402

CRITICAL
L9810
FERR-220-OHM
0402

HDMI DDC CLK CONN — HDMI DDC CLK F

R9811 33 5% 1/16W MF-LF 402

HDMI DDC CLK 5V

C9811 22PF 5% 50V CERM 402

CRITICAL
L9811
FERR-220-OHM
0402

HDMI DDC DATA CONN — HDMI DDC DATA F

R9813 33 5% 1/16W MF-LF 402

HDMI DDC DATA 5V

C9813 22PF 5% 50V CERM 402

CRITICAL
L9841
FERR-220-OHM
0402

HDMI HPD CONN — HDMI HPD Q

R9814 10K 5% 1/16W MF-LF 402

HDMI HPD

C9814 220PF 10% 50V X7R-CERM 402

100K PULL-DOWN IS BUILT INTO LEVEL SHIFTER.

SYNC_MASTER=REFERENCE_MLB SYNC_DATE=11/23/2010

PAGE TITLE: HDMI CONNECTOR

Apple Inc.

DRAWING NUMBER: 051-8937 SIZE: D

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: HR PDG section 4.1.9, PDDG section 2.5.1

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	10 18
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	10 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	10 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	10 18
1125 DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	11 17
1126	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	11 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	8 18
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	8 18
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	8 18
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	8 18
	CPU_50S	CPU_AGTL	FDI_INT	8 18
	CPU_50S	CPU_VID	CPU_VCCSA_VID<1>	13 64
1144	CPU_50S	CPU_VID	CPU_VIDALERT_L	13 67
1144	CPU_50S	CPU_VID	CPU_VIDALERT_L_R	13
1145	CPU_50S	CPU_VID	CPU_VIDSCLK	13 67
1142	CPU_50S	CPU_VID	CPU_VIDSCLK_R	13
1141	CPU_50S	CPU_VID	CPU_VIDSOUT	13 67
1140	CPU_50S	CPU_VID	CPU_VIDSOUT_R	13
1140 CPU_PECI	CPU_50S	PCIE	CPU_PECI	11 20 46
	CPU_50S	PCIE	CPU_PECI_R	46
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	11 18
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	11 18 28
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2..0>	11
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<11..0>	10 24
1124 CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<17..16>	10
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	6 11
	CPU_50S	CPU_AGTL	CPU_PROC_SEL_L	11 18
1115	CPU_50S	CPU_AGTL	CPU_VTTSELECT	
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	11 47 67
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	11 20 24
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	11 20
	CPU_55S	CPU_8MIL	CPU_PSI_L	
PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	10
	CPU_27P4S	CPU_COMP	CPU_PEG_RBIAS	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP3	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP2	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP1	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP0	
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	13 67
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	13 67
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P	13 70
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N	13 70
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P	13 67
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N	13 67
1120	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	10
1121	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	10
1122	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	10
1123	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	10
	CPU_55S	CPU_8MIL	GFX_VID<6..0>	
PM_DPRSLPVR	CPU_50S	CPU_AGTL	GFX_DPRSLPVR	
	CPU_50S	CPU_AGTL	GFX_VR_EN	
	CPU_50S	CPU_AGTL	GFXIMVP_IMON	
	PCIE_85D	PCIE	PEG_R2D_P<7..0>	73
	PCIE_85D	PCIE	PEG_R2D_N<7..0>	73
PEG_R2D	PCIE_85D	PCIE	PEG_R2D_C_P<7..0>	8 73
	PCIE_85D	PCIE	PEG_R2D_C_N<7..0>	8 73
PEG_D2R	PCIE_85D	PCIE	PEG_D2R_P<7..0>	8 73
	PCIE_85D	PCIE	PEG_D2R_N<7..0>	8 73
	PCIE_85D	PCIE	PEG_D2R_C_P<7..0>	73
	PCIE_85D	PCIE	PEG_D2R_C_N<7..0>	73

PEG CLOCK ON PP103 WITH PCIE CONSTRAINTS.

XDP Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
XDP_BPM	CPU_50S	CPU_ITP	XDP_BPM_L<3..0>	11 24
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<7..4>	11 24
	CPU_50S	CPU_ITP	XDP_CPURST_L	24
1137 CPU_CFG	CPU_50S	CPU_ITP	XDP_CPU_CFG<0>	24
XDP_PRDY_L	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	11 24
XDP_PREQ_l	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	11 24
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	11 24
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	11 24
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	11 24
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	11 24
XDP_TRST_l	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	11 24
1112	CPU_50S	CPU_ITP	XDP_PCH_TCK	17 24
1112	CPU_50S	CPU_ITP	XDP_PCH_TDI	17 24
1113	CPU_50S	CPU_ITP	XDP_PCH_TDO	17 24
1113	CPU_50S	CPU_ITP	XDP_PCH_TMS	17 24
1113	CPU_50S	CPU_ITP	XDP_TDI	24
1113	CPU_50S	CPU_ITP	XDP_TDO	24
1113	CPU_50S	CPU_ITP	XDP_TMS	24
XDP_CPU_PWRGOOD	CPU_50S	CPU_ITP	XDP_CPU_PWRGD	24
XDP_BDRESET_L	CPU_50S	CPU_ITP	XDP_DBRESET_L	11 24 27
1113	CPU_50S	CPU_ITP	XDP_PRESENT_L	24
1113	CPU_50S	CPU_ITP	XDP_RES_RL	24
1113	CPU_50S	CPU_ITP	XDP_CPU_PWRBTN_L	24
1113	CPU_50S	CPU_ITP	XDP_VR_READY	24
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	11 17
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	11 17
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	17 24
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	17 24
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	24
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	24

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3:
DQ/DM signals should be matched within 0.508mm of associated DQS pair.
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-12.7mm] and [CLK+25.4mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-12.7mm] to [CLK+0.0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to SODIMM pad is 139.7mm, from procesor ball to SODIMM pad is 114.3mm.

SOURCE: Calpella SFF Platform DG, Rev 1.5 (#407364), Section 2.2
SOURCE: HR PDG, Section 4.1.9

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_85D	MEM_CLK	MEM_A_CLK_P<5..0>	12 30
MEM_A_CLK	MEM_85D	MEM_CLK	MEM_A_CLK_N<5..0>	12 30
MEM_A_CNTL	MEM_40S	MEM_CTRL	MEM_A_CKE<3..0>	12 30
MEM_A_CNTL	MEM_40S	MEM_CTRL	MEM_A_CS_L<3..0>	12 30
MEM_A_CNTL	MEM_40S	MEM_CTRL	MEM_A_ODT<3..0>	12 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>	12 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>	12 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L	12 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L	12 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L	12 30
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0>	12 29
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8>	12 29
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16>	12 29
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24>	12 29
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32>	12 29
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40>	12 29
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48>	12 29
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56>	12 29
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	12 29
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	12 29
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	12 29
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	12 29
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	12 29
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	12 29
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	12 29
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	12 29
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	12 29
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	12 29
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	12 29
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	12 29
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	12 29
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	12 29
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	12 29
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	12 29
MEM_B_CLK	MEM_85D	MEM_CLK	MEM_B_CLK_P<5..0>	12 31
MEM_B_CLK	MEM_85D	MEM_CLK	MEM_B_CLK_N<5..0>	12 31
MEM_B_CNTL	MEM_40S	MEM_CTRL	MEM_B_CKE<3..0>	12 31
MEM_B_CNTL	MEM_40S	MEM_CTRL	MEM_B_CS_L<3..0>	12 31
MEM_B_CNTL	MEM_40S	MEM_CTRL	MEM_B_ODT<3..0>	12 31
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0>	12 31
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>	12 31
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L	12 31
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L	12 31
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L	12 31
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0>	12 29
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8>	12 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16>	12 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24>	12 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32>	12 29
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40>	12 29
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48>	12 29
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56>	12 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	12 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	12 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	12 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	12 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	12 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	12 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	12 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	12 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	12 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	12 29
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	12 29
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	12 29
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	12 29
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	12 29
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	12 29
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	12 29

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
DP_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TMDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
TMDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TMDS_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=4:1_SPACING	?
TMDS	*	=4:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4:1_SPACING	?
TMDS	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PDG, TABLES 191,193, Radeon TRM section 7.7.1
PER ANIL: MODIFIED DP CONNECTOR NEEDS 90 OHMS. MEASURE PROTO BOARD AND ADJUST IF NEEDED.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=5:1_SPACING	?
SATA_ICOMP	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=5:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4:1_SPACING	?
USB_RBIAS	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD1_D2R_CONN_N	42 100
	SATA_90D	SATA	SATA_HDD1_D2R_CONN_P	42 100
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD1_D2R_N	17 42
	SATA_90D	SATA	SATA_HDD1_D2R_P	17 42
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD1_R2D_CONN_N	42 100
	SATA_90D	SATA	SATA_HDD1_R2D_CONN_P	42 100
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD1_R2D_C_N	17 42
	SATA_90D	SATA	SATA_HDD1_R2D_C_P	17 42
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD2_D2R_CONN_N	42 100
	SATA_90D	SATA	SATA_HDD2_D2R_CONN_P	42 100
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD2_D2R_N	17 42
	SATA_90D	SATA	SATA_HDD2_D2R_P	17 42
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD2_R2D_CONN_N	42 100
	SATA_90D	SATA	SATA_HDD2_R2D_CONN_P	42 100
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD2_R2D_C_N	17 42
	SATA_90D	SATA	SATA_HDD2_R2D_C_P	17 42
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD1_D2R_DF_N	42
	SATA_90D	SATA	SATA_HDD1_D2R_DF_P	42
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD1_R2D_DF_N	42
	SATA_90D	SATA	SATA_HDD1_R2D_DF_P	42
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD2_D2R_DF_N	42
	SATA_90D	SATA	SATA_HDD2_D2R_DF_P	42
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD2_R2D_DF_N	42
	SATA_90D	SATA	SATA_HDD2_R2D_DF_P	42
PCH_SATA3_ICOMP	SATA_50SE	SATA_ICOMP	PCH_SATA3COMP	17
PCH_SATA_ICOMP	SATA_37SE	SATA_ICOMP	PCH_SATAICOMP	17
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	19
USB_HUB1_UP	USB_85D	USB	USB_HUB1_UP_N	19 25
	USB_85D	USB	USB_HUB1_UP_P	19 25
USB_HUB2_UP	USB_85D	USB	USB_HUB2_UP_N	19 25
	USB_85D	USB	USB_HUB2_UP_P	19 25
USB_EXTA	USB_85D	USB	USB_EXTA_N	25 43
	USB_85D	USB	USB_EXTA_P	25 43
USB_EXTB	USB_85D	USB	USB_EXTB_N	25 43
	USB_85D	USB	USB_EXTB_P	25 43
USB_EXTC	USB_85D	USB	USB_EXTC_N	25 43
	USB_85D	USB	USB_EXTC_P	25 43
USB_EXTD	USB_85D	USB	USB_EXTD_N	25 43
	USB_85D	USB	USB_EXTD_P	25 43
	USB_85D	USB	USB_PORT0_N	43
	USB_85D	USB	USB_PORT0_P	43
	USB_85D	USB	USB_PORT1_N	43
	USB_85D	USB	USB_PORT1_P	43
	USB_85D	USB	USB_PORT2_N	43
	USB_85D	USB	USB_PORT2_P	43
	USB_85D	USB	USB_PORT3_N	43
	USB_85D	USB	USB_PORT3_P	43
USB_IR	USB_85D	USB	USB_IR_N	25 44
	USB_85D	USB	USB_IR_P	25 44
	USB_85D	USB	USB_IR_R_N	44
	USB_85D	USB	USB_IR_R_P	44
USB_BT	USB_85D	USB	USB_BT_N	25 35
	USB_85D	USB	USB_BT_P	25 35
	USB_85D	USB	USB_BT_CONN_N	35 100
	USB_85D	USB	USB_BT_CONN_P	35 100
	USB_85D	USB	USB_B_MUXED_N	43
	USB_85D	USB	USB_B_MUXED_P	43

DP Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DP_90D	DISPLAYPORT	DP_AUX_CH_CK_N	
	DP_90D	DISPLAYPORT	DP_AUX_CH_CK_P	
	DP_90D	DISPLAYPORT	DP_AUX_CH_C_N	
	DP_90D	DISPLAYPORT	DP_AUX_CH_C_P	
	T29DP_90D	T29DP	DP_A_EXT_AUXCH_N	86 87 95
	T29DP_90D	T29DP	DP_A_EXT_AUXCH_P	86 87 95
	DP_90D	DISPLAYPORT	DP_EXTA_AUXCH_C_N	8 86
	DP_90D	DISPLAYPORT	DP_EXTA_AUXCH_C_P	8 86
	DP_90D	DISPLAYPORT	DP_EXTA_AUXCH_N	86
	DP_90D	DISPLAYPORT	DP_EXTA_AUXCH_P	86
	DP_90D	DISPLAYPORT	DP_EXTA_DDC_CLK_AUX_P	Manual Diff Pair
	DP_90D	DISPLAYPORT	DP_EXTA_DDC_DATA_AUX_N	Manual Diff Pair
	DP_55S	DISPLAYPORT	DP_EXTA_DDC_CLK	8 86
	DP_55S	DISPLAYPORT	DP_EXTA_DDC_DATA	8 86
	DP_55S	DISPLAYPORT	DP_EXTA_HPD	8 86
	DP_90D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_N	8 83
	DP_90D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_P	8 83
	DP_90D	DISPLAYPORT	DP_T29SNK0_AUXCH_N	83
	DP_90D	DISPLAYPORT	DP_T29SNK0_AUXCH_P	83
	DP_90D	DISPLAYPORT	DP_EXTA_ML_C_N<3..0>	8 86
	DP_90D	DISPLAYPORT	DP_EXTA_ML_C_P<3..0>	8 86
	DP_90D	DISPLAYPORT	DP_EXTA_ML_N<3..0>	86
	DP_90D	DISPLAYPORT	DP_EXTA_ML_P<3..0>	86
	DP_90D	DISPLAYPORT	DP_ML_CK_N<3..0>	
	DP_90D	DISPLAYPORT	DP_ML_CK_P<3..0>	
	DP_90D	DISPLAYPORT	DP_ML_C_N<3..0>	
	DP_90D	DISPLAYPORT	DP_ML_C_P<3..0>	
	DP_90D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_N	8 83
	DP_90D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_P	8 83
	DP_90D	DISPLAYPORT	DP_T29SNK1_AUXCH_N	83
	DP_90D	DISPLAYPORT	DP_T29SNK1_AUXCH_P	83
	DP_90D	DISPLAYPORT	DP_T29SNK0_ML_C_N<3..0>	8 83
	DP_90D	DISPLAYPORT	DP_T29SNK0_ML_C_P<3..0>	8 83
	DP_90D	DISPLAYPORT	DP_T29SNK0_ML_N<3..0>	83
	DP_90D	DISPLAYPORT	DP_T29SNK0_ML_P<3..0>	83
	DP_55S	DISPLAYPORT	DP_T29SNK0_DDC_CLK	
	DP_55S	DISPLAYPORT	DP_T29SNK0_DDC_DATA	
	DP_55S	DISPLAYPORT	DP_T29SNK0_HPD	8 83
	DP_90D	DISPLAYPORT	DP_T29SNK1_ML_C_N<3..0>	8 83
	DP_90D	DISPLAYPORT	DP_T29SNK1_ML_C_P<3..0>	8 83
	DP_90D	DISPLAYPORT	DP_T29SNK1_ML_N<3..0>	83
	DP_90D	DISPLAYPORT	DP_T29SNK1_ML_P<3..0>	83
	DP_55S	DISPLAYPORT	DP_T29SNK1_HPD	8 83

HDMI Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	TMDS_100D	TMDS	HDMI_CLK_CONN_N	89
	TMDS_100D	TMDS	HDMI_CLK_CONN_P	89
	TMDS_85D	TMDS	HDMI_CLK_C_N	8 88
	TMDS_85D	TMDS	HDMI_CLK_C_P	8 88
	TMDS_85D	TMDS	HDMI_CLK_LS_N	88
	TMDS_85D	TMDS	HDMI_CLK_LS_P	88
	TMDS_100D	TMDS	HDMI_CLK_N	88 89
	TMDS_100D	TMDS	HDMI_CLK_P	88 89
	TMDS_100D	TMDS	HDMI_DATA_CONN_N<2..0>	89
	TMDS_100D	TMDS	HDMI_DATA_CONN_P<2..0>	89
	TMDS_85D	TMDS	HDMI_DATA_C_N<2..0>	8 88
	TMDS_85D	TMDS	HDMI_DATA_C_P<2..0>	8 88
	TMDS_85D	TMDS	HDMI_DATA_LS_N<2..0>	88
	TMDS_85D	TMDS	HDMI_DATA_LS_P<2..0>	88
	TMDS_100D	TMDS	HDMI_DATA_N<2..0>	88 89
	TMDS_100D	TMDS	HDMI_DATA_P<2..0>	88 89
	TMDS_55S	TMDS	HDMI_LS_SCL	8 88
	TMDS_55S	TMDS	HDMI_LS_SDA	8 88
	TMDS_55S	TMDS	HDMI_LS_HPD	8 88

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_50S	LPC	LPC AD<3..0>	17 46 48
	LPC_50S	LPC	LPC R AD<3..0>	17
LPC_FRAME_L	LPC_50S	LPC	LPC FRAME L	17 46 48
	LPC_50S	LPC	LPC FRAME R L	17
LPC_RESET_L	LPC_50S	LPC	LPCPLUS RESET L	27 48
PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC CLK33M SMC R	19 27
	CLK_LPC_50S	CLK_LPC	LPC CLK33M SMC	27 46
	CLK_LPC_50S	CLK_LPC	LPC CLK33M LPCPLUS	27 48
	CLK_LPC_50S	CLK_LPC	LPC CLK33M LPCPLUS R	19 27
	SMB_50S	SMB	SMB PCH STR SCL	49
	SMB_50S	SMB	SMB PCH STR SDA	49
	SMB_50S	SMB	SMB PCH DIMM SCL	49
	SMB_50S	SMB	SMB PCH DIMM SDA	49
	SMB_50S	SMB	SMB PCH MKY SCL	49
	SMB_50S	SMB	SMB PCH MKY SDA	49
	SMB_50S	SMB	SMB PCH VRF SCL	49
	SMB_50S	SMB	SMB PCH VRF SDA	49
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS PCH CLK	17 49
	SMB_50S	SMB	SMBUS PCH DATA	17 49
SMBUS_PCH_0_CLK	SMB_50S	SMB	SMB PCH XDP SCL	49
	SMB_50S	SMB	SMB PCH XDP SDA	49
	SMB_50S	SMB	SML PCH 1 CLK	17 49
	SMB_50S	SMB	SML PCH 1 DATA	17 49
SPI_CLK	SPI_55S	SPI	SPI CLK R	17 48
	SPI_55S	SPI	SPI CLK	48 100
SPI_MOSI	SPI_55S	SPI	SPI MOSI R	17 48
	SPI_55S	SPI	SPI MOSI	48 100
SPI_MISO	SPI_55S	SPI	SPI MISO	17 48 100
SPI_CS0	SPI_55S	SPI	SPI CS0 R L	17 48
	SPI_55S	SPI	SPI CS0 L	48 100
HDA_BIT_CLK	HDA_50S	HDA	HDA BIT CLK	17 53
	HDA_50S	HDA	HDA BIT CLK R	17
HDA_SYNC	HDA_50S	HDA	HDA SYNC	17 53
	HDA_50S	HDA	HDA SYNC R	17
HDA_RST_L	HDA_50S	HDA	HDA RST R L	17
	HDA_50S	HDA	HDA RST L	17 53
HDA_SDIN0	HDA_50S	HDA	HDA SDIN0	17 53
	HDA_50S	HDA	AUD SDI R	53
HDA_SDOUT	HDA_50S	HDA	HDA SDOUT	17 53
	HDA_50S	HDA	HDA SDOUT R	17
	CLK_PCIE_90D	CLK_PCIE	PCH CLK96M DOT P	17
	CLK_PCIE_90D	CLK_PCIE	PCH CLK96M DOT N	17
	CLK_PCIE_90D	CLK_PCIE	PCH CLK100M SATA P	17
	CLK_PCIE_90D	CLK_PCIE	PCH CLK100M SATA N	17
	CPU_50S	CLK_PCIE	PCH CLK14P3M REFCLK	17
	CPU_50S	CLK_PCIE	PCH CLK33M PCIIN	17 27
	PCIE_85D	PCIE	PCIE ENET R2D P	37
	PCIE_85D	PCIE	PCIE ENET R2D N	37
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE ENET R2D C P	17 37
	PCIE_85D	PCIE	PCIE ENET R2D C N	17 37
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE ENET D2R P	17 37
	PCIE_85D	PCIE	PCIE ENET D2R N	17 37
	PCIE_85D	PCIE	PCIE ENET D2R C P	37
	PCIE_85D	PCIE	PCIE ENET D2R C N	37
	PCIE_85D	PCIE	PCIE AP R2D P	35 100
	PCIE_85D	PCIE	PCIE AP R2D N	35 100
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE AP R2D C P	17 35
	PCIE_85D	PCIE	PCIE AP R2D C N	17 35
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE AP D2R P	17 35 100
	PCIE_85D	PCIE	PCIE AP D2R N	17 35 100
	PCIE_85D	PCIE	PCIE FW R2D P	39
	PCIE_85D	PCIE	PCIE FW R2D N	39
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE FW R2D C P	17 39
	PCIE_85D	PCIE	PCIE FW R2D C N	17 39
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE FW D2R P	17 39
	PCIE_85D	PCIE	PCIE FW D2R N	17 39
	PCIE_85D	PCIE	PCIE FW D2R C P	39
	PCIE_85D	PCIE	PCIE FW D2R C N	39
	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M PCH P	17
	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M PCH N	17
PCIE_CLK100M_T29_	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M T29 P	17 83
	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M T29 N	17 83
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG CLK100M P	17 73
	CLK_PCIE_90D	CLK_PCIE	PEG CLK100M N	17 73
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M ENET P	17 37
	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M ENET N	17 37
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M AP CONN P	35 100
	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M AP CONN N	35 100
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M AP P	17 35
	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M AP N	17 35
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M FW P	17 39
	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M FW N	17 39
PCIE_T29_R2D	PCIE_85D	PCIE	PCIE T29 R2D C P<3..0>	8 83
PCIE_T29_R2D	PCIE_85D	PCIE	PCIE T29 R2D C N<3..0>	8 83
PCIE_T29_R2D	PCIE_85D	PCIE	PCIE T29 R2D P<3..0>	83
PCIE_T29_R2D	PCIE_85D	PCIE	PCIE T29 R2D N<3..0>	83
PCIE_T29_D2R	PCIE_85D	PCIE	PCIE T29 D2R P<3..0>	8 83
PCIE_T29_D2R	PCIE_85D	PCIE	PCIE T29 D2R N<3..0>	8 83
PCIE_T29_D2R	PCIE_85D	PCIE	PCIE T29 D2R C P<3..0>	83
PCIE_T29_D2R	PCIE_85D	PCIE	PCIE T29 D2R C N<3..0>	83

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ETHERNET CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?
2KV_SPACING	*	0.50 MM	100
2KV_SPACING	TOP,BOTTOM	1.27 MM	100

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_HV	*	*	2KV_SPACING
ENET_HV	ENET_HV	*	ENET_MDI

NOTE: 2.2kV isolation needed on all primary-side ethernet signals. Min 1.27mm separation from all other copper on the board!

SD CARD INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_INTERFACE	*	=3X_DIELECTRIC	?

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI	26 37
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO	26 37
	ENET_50S	ENET_3X	ENET_RESET_L	27 34
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3..0>	36 37
	ENET_100D	ENET_MDI	ENET_MDI_N<3..0>	36 37
	ENET_100D	ENET_HV	ENET_MDI_TRAN_N<3..0>	36
	ENET_100D	ENET_HV	ENET_MDI_TRAN_P<3..0>	36
	ENET_50S	ENET_HV	ENET_CENTER_TAP<3..0>	36
		ENET_HV	ENET_CMODE_REF	36

High-voltage isolated ethernet signals.

SD Interface Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SD_55S	SD_INTERFACE	SDCONN_CLK	34 37 100
	SD_55S	SD_INTERFACE	SDCONN_CLK_FF	34
	SD_55S	SD_INTERFACE	SDCONN_CMD	34 37 100
	SD_55S	SD_INTERFACE	SDCONN_DATA<7..0>	34 37 100
	SD_55S	SD_INTERFACE	SDCONN_CLK_R	34
	SD_55S	SD_INTERFACE	SDCONN_CMD_R	34
	SD_55S	SD_INTERFACE	SDCONN_DATA_R<7..0>	34
	SD_55S	SD_INTERFACE	ENET_CR_CLK	37
	SD_55S	SD_INTERFACE	ENET_CR_CMD	37
	SD_55S	SD_INTERFACE	ENET_CR_DATA<7..0>	37
	SD_55S	SD_INTERFACE	SDCONNF_CLK	34
	SD_55S	SD_INTERFACE	SDCONNF_CLK_FF	34

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FW_P1_TPA	FW_110D	FW_TP	FW_P0_TPA_L_N	40
	FW_110D	FW_TP	FW_P0_TPA_L_P	40
FW_P1_TPB	FW_110D	FW_TP	FW_P0_TPB_L_N	40
	FW_110D	FW_TP	FW_P0_TPB_L_P	40
	FW_110D	FW_TP	FW_PORT0_TPAL_N	41
	FW_110D	FW_TP	FW_PORT0_TPAL_P	41
	FW_110D	FW_TP	FW_PORT0_TPA_N	40 41
	FW_110D	FW_TP	FW_PORT0_TPA_P	40 41
	FW_110D	FW_TP	FW_PORT0_TPBL_N	41
	FW_110D	FW_TP	FW_PORT0_TPBL_P	41
	FW_110D	FW_TP	FW_PORT0_TPB_N	40 41
	FW_110D	FW_TP	FW_PORT0_TPB_P	40 41
	50_OHM_SE	CLK_PCIE	CLK98M_FW_XI	39
	50_OHM_SE	CLK_PCIE	CLK98M_FW_XI_R	39

Port 0 and 2 Not Used

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	=2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

T29/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

T29 IC Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
		T29_I2C_55S	T29_I2C	I2C_T29_SCL	49 83
		T29_I2C_55S	T29_I2C	I2C_T29_SDA	49 83
T29_SPI_CLK		T29_SPI_55S	T29_SPI	T29_SPI_CLK	83
T29_SPI_MOSI		T29_SPI_55S	T29_SPI	T29_SPI_MOSI	83
T29_SPI_MISO		T29_SPI_55S	T29_SPI	T29_SPI_MISO	83
T29_SPI_CS_L		T29_SPI_55S	T29_SPI	T29_SPI_CS_L	83
		T29DP_90D	T29DP	T29_R2D_C_P<3..0>	83 86
		T29DP_90D	T29DP	T29_R2D_C_N<3..0>	83 86
		T29DP_90D	T29DP	T29_D2R_P<3..0>	83 86
		T29DP_90D	T29DP	T29_D2R_N<3..0>	83 86

T29/DP Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
T29_R2D0		T29DP_90D	T29DP	T29_R2D_P<0>	86
T29_R2D0		T29DP_90D	T29DP	T29_R2D_N<0>	86
T29_R2D1		T29DP_90D	T29DP	T29_R2D_P<1>	86
T29_R2D1		T29DP_90D	T29DP	T29_R2D_N<1>	86
T29_D2R0		T29DP_90D	T29DP	T29_D2R_C_P<0>	86 87
T29_D2R0		T29DP_90D	T29DP	T29_D2R_C_N<0>	86 87
T29_D2R1		T29DP_90D	T29DP	T29_D2R_C_P<1>	86 87
T29_D2R1		T29DP_90D	T29DP	T29_D2R_C_N<1>	86 87
		T29DP_90D	T29DP	T29_R2D_C_F_P<1..0>	86
		T29DP_90D	T29DP	T29_R2D_C_F_N<1..0>	86
		T29DP_90D	T29DP	T29DPA_D2R1_AUXCH_P	87
		T29DP_90D	T29DP	T29DPA_D2R1_AUXCH_N	87
		T29DP_90D	T29DP	DP_SDRVA_ML_C_P<3..0>	86
		T29DP_90D	T29DP	DP_SDRVA_ML_C_N<3..0>	86
		T29DP_90D	T29DP	DP_SDRVA_ML_R_P<3..0>	86
		T29DP_90D	T29DP	DP_SDRVA_ML_R_N<3..0>	86
		T29DP_90D	T29DP	DP_SDRVA_ML_P<2>	86
		T29DP_90D	T29DP	DP_SDRVA_ML_N<2>	86
DP_SDRVA_ML		T29DP_90D	T29DP	DP_SDRVA_ML_P<3>	86
DP_SDRVA_ML		T29DP_90D	T29DP	DP_SDRVA_ML_N<3>	86
		T29DP_90D	T29DP	DP_SDRVA_ML_P<0>	86
		T29DP_90D	T29DP	DP_SDRVA_ML_N<0>	86
DP_SDRVA_ML		T29DP_90D	T29DP	DP_SDRVA_ML_P<1>	86
DP_SDRVA_ML		T29DP_90D	T29DP	DP_SDRVA_ML_N<1>	86
DP_SDRVA_AUXCH		T29DP_90D	T29DP	DP_SDRVA_AUXCH_P	86
DP_SDRVA_AUXCH		T29DP_90D	T29DP	DP_SDRVA_AUXCH_N	86
		T29DP_90D	T29DP	DP_SDRVA_AUXCH_C_P	86
		T29DP_90D	T29DP	DP_SDRVA_AUXCH_C_N	86
		T29DP_90D	T29DP	T29DPA_ML_P<3..0>	86 87
		T29DP_90D	T29DP	T29DPA_ML_N<3..0>	86 87
		T29DP_90D	T29DP	T29DPA_ML_C_P<3..0>	86 87
		T29DP_90D	T29DP	T29DPA_ML_C_N<3..0>	86 87
		T29DP_90D	T29DP	DP_A_EXT_AUXCH_P	86 87 92
		T29DP_90D	T29DP	DP_A_EXT_AUXCH_N	86 87 92
		T29DP_90D	T29DP	T29DPA_D2R1_AUXCH_CC_P	
		T29DP_90D	T29DP	T29DPA_D2R1_AUXCH_CC_N	
		T29DP_90D	T29DP	T29_D2R_CC_P<0>	
		T29DP_90D	T29DP	T29_D2R_CC_N<0>	

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_A_S3_SCL	46 49
	SMB_50S	SMB	SMBUS_SMC_A_S3_SDA	46 49
SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_B_S0_SCL	46 49
	SMB_50S	SMB	SMBUS_SMC_B_S0_SDA	46 49
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	46 49
	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	46 49
SMBUS_SMC_BSA_SCL	SMB_50S	SMB	ENET_ASF_SMB_CLK	37 49
	SMB_50S	SMB	ENET_ASF_SMB_DATA	37 49
SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_MGMT_SCL	46 49
	SMB_50S	SMB	SMBUS_SMC_MGMT_SDA	46 49
183	SMB_50S	SMB	SMB_SMC_B_STR_SCL	49
184	SMB_50S	SMB	SMB_SMC_B_STR_SDA	49
185	SMB_50S	SMB	SMB_SMC_B_TSN_SCL	49
186	SMB_50S	SMB	SMB_SMC_B_TSN_SDA	49

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GDDR5 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR5_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR5_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?
GDDR5_CMD	*	=2x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?
GDDR5_EDC	*	=7x_DIELECTRIC	?

GDDR5 FB B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_P	75 78
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_N	75 78
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_P	75 78
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_N	75 78
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_A<8..0>	75 78
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_A<8..0>	75 78
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_ABI_L	75 78
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_ABI_L	75 78
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_RAS_L	75 78
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_RAS_L	75 78
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CAS_L	75 78
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CAS_L	75 78
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_WE_L	75 78
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_WE_L	75 78
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CKE_L	75 78
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CKE_L	75 78
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CS_L	75 78
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CS_L	75 78
FB_B0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<0>	75 78
FB_B0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<1>	75 78
FB_B0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<2>	75 78
FB_B0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<3>	75 78
FB_B1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<0>	75 78
FB_B1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<1>	75 78
FB_B1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<2>	75 78
FB_B1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<3>	75 78
FB_B0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<0>	75 78
FB_B0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<1>	75 78
FB_B0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<2>	75 78
FB_B0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<3>	75 78
FB_B1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<0>	75 78
FB_B1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<1>	75 78
FB_B1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<2>	75 78
FB_B1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<3>	75 78
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<0>	75 78
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<0>	75 78
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<1>	75 78
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<1>	75 78
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<0>	75 78
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<0>	75 78
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<1>	75 78
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<1>	75 78
FB_B0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<7..0>	75 78
FB_B0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<15..8>	75 78
FB_B0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<23..16>	75 78
FB_B0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<31..24>	75 78
FB_B1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<7..0>	75 78
FB_B1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<15..8>	75 78
FB_B1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<23..16>	75 78
FB_B1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<31..24>	75 78
FB_AB_RESET	GDDR5_45R50SE	GDDR5_CMD	FB_RESET_L	75 78

Whistler Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
GPU_CLK27M	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M	79 80
GPU_CLK100M	CLK_SLOW_55S	CLK_SLOW	GPU_CLK100M	79 80
	100_OHM_DIFF	3X_DIELECTRIC	GPU_CLK_TEST_N	75
	100_OHM_DIFF	3X_DIELECTRIC	GPU_CLK_TEST_P	75
DP_AUX_CH	DP_90D	DISPLAYPORT	DP_EG_AUX_CH_P	
	DP_90D	DISPLAYPORT	DP_EG_AUX_CH_N	

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GPU (Whistler) CONSTRAINTS

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	2.54 MM OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	2.54 MM OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 MM OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	12.7 MM OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	2.54 MM OVERRIDE	OVERRIDE	OVERRIDE

Breakout Constraint Overrides

Alternate diffpair width/gap through BGA fanout areas

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_PCIE_90D	BGA	100_DIFF_BGA
DP_90D	BGA	100_DIFF_BGA
TMDS_85D	BGA	TMDS_85D
ENET_100D	BGA	100_DIFF_BGA
FW_110D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
PCIE_85D	BGA	PCIE_85D
MEM_85D	BGA	MEM_85D
USB_85D	BGA	USB_85D
GDDR5_80D	BGA	GDDR5_80D

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA	BGA_P075
MEM_50S	BGA	BGA_P075

J40* SPECIFIC NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_P	50 64
	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_N	50 64
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_P	50 70
	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_N	50 70
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_P	51
	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_N	51

J40* SPECIFIC NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
		SB_POWER	PP3V3_S5	6 17 18 19 20 21 23 24 25 27 28 59 61 62 87 100
		SB_POWER	PP3V3_S0	100 50 51 52 53 57 58 60 61 62 67 6 7 13 17 18 19 20 21 23 24 27 30 33 35 37 38 39 40 41 47 48 71 72 74 76 79 80 82 85 86 88
		GND	GND	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P	10 52
	THERM_1TO1_55S	THERM	CPU_THERMD_N	10 52
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	
	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P	52 79
	THERM_1TO1_55S	THERM	GPU_TDIODE_N	52 79
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	T29_THERMD_P	
	THERM_1TO1_55S	THERM	T29_THERMD_N	

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J40GS BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,ISL12,ISL13,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	ISL6,ISL9	Y	0.190 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD
27P4_OHM_SE	*	Y	0.235 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.195 MM	0.095 MM			
37_OHM_SE	ISL6,ISL9	Y	0.119 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD
37_OHM_SE	*	Y	0.145 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.095 MM			
40_OHM_SE	ISL6,ISL9	Y	0.105 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	*	Y	0.125 MM	0.095 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.095 MM			
45_OHM_SE	ISL6,ISL9	Y	0.082 MM	0.082 MM	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	*	Y	0.099 MM	0.099 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	ISL6,ISL9	Y	0.067 MM	0.067 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	*	Y	0.085 MM	0.080 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

NOTE: 55 OHMS SE NOT POSSIBLE ON LAYERS 6 & 9, RULE GIVES 49 OHMS ON THOSE LAYERS
AVOID ROUTING 55 OHMS ON LAYERS 6 AND 9.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.160 MM	0.160 MM
80_OHM_DIFF	ISL6,ISL9	Y	0.095 MM	0.095 MM	=STANDARD	0.130 MM	0.130 MM
80_OHM_DIFF	*	Y	0.111 MM	0.111 MM	=STANDARD	0.150 MM	0.150 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.095 MM		0.160 MM	0.090 MM
85_OHM_DIFF	ISL6,ISL9	Y	0.086 MM	0.067 MM	=STANDARD	0.150 MM	0.090 MM
85_OHM_DIFF	*	Y	0.101 MM	0.090 MM	=STANDARD	0.170 MM	0.110 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.090 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL6,ISL9	Y	0.080 MM	0.080 MM	=STANDARD	0.200 MM	0.200 MM
90_OHM_DIFF	*	Y	0.091 MM	0.091 MM	=STANDARD	0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL6,ISL9	Y	0.065 MM	0.065 MM	=STANDARD	0.220 MM	0.200 MM
100_OHM_DIFF	*	Y	0.074 MM	0.074 MM	=STANDARD	0.220 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	TOP,BOTTOM	Y	0.076 MM	0.076 MM		0.250 MM	0.250 MM
110_OHM_DIFF	ISL6,ISL9	Y	0.065 MM	0.065 MM	=STANDARD	0.220 MM	0.200 MM
110_OHM_DIFF	*	Y	0.074 MM	0.074 MM	=STANDARD	0.220 MM	0.200 MM

NOTE: 110-Ohms DIFF is not possible on inner layers, the rule gives 100-Ohms for inner layers to allow routing where needed. Avoid routing 110-Ohm DIFF on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	TOP,BOTTOM	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	*	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BGA_P075	TOP	Y	0.110 MM	0.080 MM	10 MM		
BGA_P075	BOTTOM	Y	0.110 MM	0.073 MM	10 MM		

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P075MM	*	0.075 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P075MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?

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PCB Rule Definitions

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Airport/BT/Camera Conn.

FUNC_TEST

TRUE	PCIE_AP_D2R_P	17 35 93
TRUE	PCIE_AP_D2R_N	17 35 93
TRUE	PCIE_AP_R2D_P	35 93
TRUE	PCIE_AP_R2D_N	35 93
TRUE	PCIE_CLK100M_AP_CONN_P	35 93
TRUE	PCIE_CLK100M_AP_CONN_N	35 93
TRUE	AP_CLKREQ_Q_L	35
TRUE	PCIE_WAKE_L	18 35 38 86
TRUE	AP_RESET_CONN_L	35
TRUE	WLAN_THROTTLE_L	35
TRUE	PP3V3_S4_BT_F	35
TRUE	PP3V3_WLAN	35 47 — 3 TPS
TRUE	USB_BT_CONN_P	35 92
TRUE	USB_BT_CONN_N	35 92
TRUE	GND	— 3 TPS

SD Card Connector
NOT USED - REMOVE

FUNC_TEST

FALSE	SDCONN_DATA<7..0>	34 37 94
FALSE	SDCONN_CMD	34 37 94
FALSE	SDCONN_CLK	34 37 94
FALSE	SDCONN_DETECT	34
FALSE	SDCONN_WP	34 37
FALSE	PP3V3_SW_SD_PWR	34
TRUE	GND	— 2 TPs

SATA HDD Connector

FUNC_TEST

TRUE	PP5V_S0	89 100 / 67 68 69 70 / 7 23 24 41 42 / 46 61 63 64 / 71 76 77 / 42 92 — 2 TPS
TRUE	SATA_HDD1_D2R_CONN_P	
TRUE	SATA_HDD1_D2R_CONN_N	42 92
TRUE	SATA_HDD1_R2D_CONN_N	42 92
TRUE	SATA_HDD1_R2D_CONN_P	42 92
TRUE	GND	— 2 TPS

SATA HDD2 CONNECTOR

FUNC_TEST

TRUE	PP5V_S0	89 100 / 67 68 69 70 / 7 23 24 41 42 / 46 61 63 64 / 71 76 77 — 2 TPS
TRUE	SATA_HDD2_D2R_CONN_N	42 92
TRUE	SATA_HDD2_D2R_CONN_P	42 92
TRUE	SATA_HDD2_R2D_CONN_N	42 92
TRUE	SATA_HDD2_R2D_CONN_P	42 92
TRUE	GND	— 2 TPS

IR/LED,POWER BUTTON CONNECTORS

FUNC_TEST

TRUE	PPIRRCVR_F	45 — 1 TPS
TRUE	SMC_SYS_LED_DR	45
TRUE	IRRCVR_OUT	44 45
TRUE	POWER_BTN_N	45
TRUE	POWER_BTN_P	45
TRUE	GND	— 1 TPS

TEMPERATURE SENSOR CONNECTORS

TRUE	HDD_THRMD_P
TRUE	HDD_THRMD_N

Speaker Connectors

FUNC_TEST

TRUE	SPKRAMP_M_P_OUT	56 57
TRUE	SPKRAMP_M_N_OUT	56 57

Fan Connectors

FUNC_TEST

TRUE	PP12V_S0_FAN0_F	60
TRUE	FAN0_CTL_F	60
TRUE	FAN0_TACH_F	60
TRUE	GND	— 1 TPS

PSU CONNECTOR

FUNC_TEST

TRUE	PP12V_G3H_PSU	6 51 72 — 4 TPS
TRUE	PSU_TEMP	47 72
TRUE	GND	— 4 TPS

Power Nets

FUNC_TEST

TRUE	PP3V3_G3_RTC	6 17 18 21 27
TRUE	PP5V_G3H	6 45 47 61 65
TRUE	PP3V3_G3H	6 27 43 45 46 47 48 61 65 100
TRUE	PP3V3_S5	6 17 18 19 20 21 23 24 25 27 28 / 59 61 62 87 98
TRUE	PP3V3_ENET	6 26 37 38 62
TRUE	PP1V2_ENET	6 37 38
TRUE	PP5V_S4	6 28 43 44 45 61 65 66 82 87
TRUE	PP3V3_S4	6 19 20 25 28 33 34 35 38 47 49 / 50 61 86 87
TRUE	PP1V5_S3	6 28 30 31 32 61 66 72
TRUE	PPDDRVREF_S3	6 33 66
TRUE	PP5V_S0	89 100 / 7 23 24 41 42 48 61 62 64 67 68 69 70 / 71 76 77 / 88 91 92 53 57 58 60 61 62 67 / 6 13 17 18 19 20 21 24 27 / 29 37 38 39 40 41 42 43 47 49 / 71 73 74 75 76 80 82 85 86 88 / 17 21 23 39 53 71 72
TRUE	PP3V3_S0	7 10 11 13 15 67
TRUE	PP1V5_S0	7 28 30 31 66
TRUE	PP1V05_S0_VCCIO	7 10 13 15 50 67 68
TRUE	PP0V75_S0_DDRVTT	
TRUE	PPVCORE_S0_CPU	
TRUE	FW_PORT0_VP	41
TRUE	PP3V3_S5_AVREF_SMC	46 47
TRUE	PP4V5_AUDIO_ANALOG	53
TRUE	PP3V3R12V_SW_DPAPWR_F	87
TRUE	PP5V_HDMI_DDC_CONN	89
TRUE	GND	— 1 TPS
TRUE	SMC_PM_G2_EN	46 47 62
TRUE	PM_SLP_S5_L	18 46 62
TRUE	PM_SLP_S4_L	18 28 46 62
TRUE	PM_SLP_S3_L	18 28 46 51 62

SPI BOOTROM SIGNALS

FUNC_TEST

TRUE	PP3V3_G3H	100 / 24 37 / 43 / 46 47 / 65 — 45 — 1 TPS
TRUE	SPI_CS0_L	48 93
TRUE	SPI_CLK	48 93
TRUE	SPI_MOSI	48 93
TRUE	SPI_MISO	17 48 93
TRUE	SPIROM_USE_MLB	20 48 59
TRUE	GND	— 1 TPS

NO_TEST

TRUE	NC_AUD_GPIO_0	53
TRUE	NC_AUD_HP_PORT_R	53
TRUE	NC_AUD_MIC_INN_R	53
TRUE	NC_CLINK_CLK	17
TRUE	NC_CRT_IG_BLUE	18
TRUE	NC_CRT_IG_GREEN	18
TRUE	NC_CRT_IG_VSYNC	18
TRUE	NC_DP_OC	
TRUE	NC_EDP_TXN<3..0>	10
TRUE	NC_FW_P1_TPAP	39
TRUE	NC_FW_P2_TPAP	39
TRUE	NC_HD_OC	89
TRUE	NC_HDA_SDIN3	17
TRUE	NC_IG_DP_T29SNK0_AUXCH_CN	8
TRUE	NC_IG_DP_T29SNK0_CTRL_DATA	8
TRUE	NC_IG_DP_T29SNK0_ML_CP<3..0>	8
TRUE	NC_IRUC_P04	44
TRUE	NC_IRUC_P14	44
TRUE	NC_LPC_DREQ0_L	17
TRUE	NC_LVDS_IG_A_DATAN<3..0>	19
TRUE	NC_LVDS_IG_B_CLKP	19
TRUE	NC_LVDS_IG_BKL_ON	19
TRUE	NC_LVDS_IG_CTRL_DATA	19
TRUE	NC_LVDS_IG_PANEL_PWR	19
TRUE	NC_OBSFN_B0	24
TRUE	NC_OBSFN_D01	24
TRUE	NC_PCH_CLKOUT_DPP	17
TRUE	NC_PCH_GPIO66_CLKOUTFLEX2	17
TRUE	NC_PCH_LVDS_VBG	19
TRUE	NC_PCIE_4_D2RP	17
TRUE	NC_PCIE_5_D2RN	17
TRUE	NC_PCIE_5_R2D_CP	17
TRUE	NC_PCIE_6_R2D_CN	17
TRUE	NC_PCIE_7_D2RP	17
TRUE	NC_PCIE_8_D2RN	17
TRUE	NC_PCIE_8_R2D_CP	17
TRUE	NC_PCIE_CLK100M_PE5N	17
TRUE	NC_PCIE_CLK100M_PE6P	20
TRUE	NC_PCIE_CLK100M_PEBN	17
TRUE	NC_PCIE_CLK100M_T29P	
TRUE	NC_PCIE_T29_R2D_CN<3..0>	
TRUE	NC_PEG_CLK100MP	
TRUE	NC_PEG_D2RP<7..0>	
TRUE	NC_PEG_R2D_CN<15..12>	10
TRUE	NC_SATA_C_D2RN	17
TRUE	NC_SATA_C_R2D_CP	17
TRUE	NC_SATA_D_R2D_CN	17
TRUE	NC_SATA_E_D2RP	17
TRUE	NC_SATA_F_D2RN	17
TRUE	NC_SATA_F_R2D_CP	17
TRUE	NC_SDVO_STALLN	18
TRUE	NC_SDVO_TVCLKINP	18
TRUE	NC_SMC_FAN_1_TACH	46
TRUE	NC_SMC_FAN_3_CTL	46
TRUE	NC_SMC_P20	46
TRUE	NC_SMC_P43	46
TRUE	NC_SMC_SYS_KBDLED	46
TRUE	NC_USB_1N	19
TRUE	NC_USB_2P	19
TRUE	NC_USB_4N	19
TRUE	NC_USB_5P	19
TRUE	NC_USB_7N	19
TRUE	NC_USB_9P	19
TRUE	NC_USB_11N	19
TRUE	NC_USB_12P	19
TRUE	NC_CPU_AXG_SENSEN	
TRUE	NC_CPU_AXG_VALSENSEP	
TRUE	NC_EG_DP_T29SNK0_AUXCH_CP	
TRUE	NC_EG_DP_T29SNK0_ML_CP<3..0>	
TRUE	NC_FB_A0_ABI_L	75
TRUE	NC_FB_A0_CKE_L	75
TRUE	NC_FB_A0_CLKP	75
TRUE	NC_FB_A0_DBI_L<3..0>	75
TRUE	NC_FB_A0_EDC<3..0>	75
TRUE	NC_FB_A0_WCLKN<1..0>	75
TRUE	NC_FB_A0_WE_L	75
TRUE	NC_FB_A1_ABI_L	75
TRUE	NC_FB_A1_CKE_L	75
TRUE	NC_FB_A1_CLKP	75
TRUE	NC_FB_A1_DBI_L<3..0>	75
TRUE	NC_FB_A1_EDC<3..0>	75
TRUE	NC_FB_A1_WCLKN<1..0>	75
TRUE	NC_FB_A1_WE_L	75
TRUE	NC_GPU_GENERICB	79
TRUE	NC_GPU_GENERICC	79
TRUE	NC_GPU_GENERICE	
TRUE	NC_GPU_GENERICF	79
TRUE	NC_GPU_GENERICG	79
TRUE	NC_LVDS_EG_A_CLKN	79
TRUE	NC_LVDS_EG_A_CLKP	79
TRUE	NC_LVDS_EG_A_DATAN<3..0>	79
TRUE	NC_LVDS_EG_A_DATAP<3..0>	79
TRUE	NC_LVDS_EG_B_CLKN	79
TRUE	NC_LVDS_EG_B_CLKP	79
TRUE	NC_LVDS_EG_B_DATAN<3..0>	79
TRUE	NC_LVDS_EG_B_DATAP<3..0>	79
TRUE	NC_LVDS_EG_DDC_CLK	79
TRUE	NC_LVDS_EG_DDC_DATA	79

NO_TEST

TRUE	NC_AUD_GPIO_2	53
TRUE	NC_AUD_LO3_N_R	53
TRUE	NC_AUD_MIC_INP_R	53
TRUE	NC_CLINK_DATA	17
TRUE	NC_CRT_IG_DDC_CLK	18
TRUE	NC_CRT_IG_HSYNC	18
TRUE	NC_CS4206_FP	53
TRUE	NC_EDP_AUXN	10
TRUE	NC_EDP_TXP<3..0>	10
TRUE	NC_FW_P1_TPBIAS	39
TRUE	NC_FW_P2_TPBIAS	39
TRUE	NC_HDA_SDIN1	17
TRUE	NC_IG_D_AUXN	18
TRUE	NC_IG_DP_T29SNK0_AUXCH_CP	8
TRUE	NC_IG_DP_T29SNK0_HPD	8
TRUE	NC_IRUC_P02	44
TRUE	NC_IRUC_P06	44
TRUE	NC_IRUC_P15	44
TRUE	NC_LVDS_IG_A_CLKN	19
TRUE	NC_LVDS_IG_A_DATAP<3..0>	19
TRUE	NC_LVDS_IG_B_DATAN<3..0>	19
TRUE	NC_LVDS_IG_BKL_PWM	19
TRUE	NC_LVDS_IG_DDC_CLK	19
TRUE	NC_LVDS_IG_VREFH	19
TRUE	NC_OBSFN_B1	24
TRUE	NC_OBSFN_D11	24
TRUE	NC_PCH_GPIO64_CLKOUTFLEX0	17
TRUE	NC_PCH_GPIO67_CLKOUTFLEX3	17
TRUE	NC_PCI_PME_L	19
TRUE	NC_PCIE_4_R2D_CN	17
TRUE	NC_PCIE_5_D2RP	17
TRUE	NC_PCIE_6_D2RN	17
TRUE	NC_PCIE_6_R2D_CP	17
TRUE	NC_PCIE_7_R2D_CN	17
TRUE	NC_PCIE_8_D2RP	17
TRUE	NC_PCIE_CLK100M_EXCARDN	17
TRUE	NC_PCIE_CLK100M_PE5P	17
TRUE	NC_PCIE_CLK100M_PE7N	20
TRUE	NC_PCIE_CLK100M_PEBP	17
TRUE	NC_PCIE_T29_D2RN<3..0>	
TRUE	NC_PCIE_T29_R2D_CP<3..0>	
TRUE	NC_PEG_D2RN<7..0>	
TRUE	NC_PEG_D2RP<15..12>	10
TRUE	NC_PEG_R2D_CP<7..0>	
TRUE	NC_SATA_C_D2RP	17
TRUE	NC_SATA_D_D2RN	17
TRUE	NC_SATA_D_R2D_CP	17
TRUE	NC_SATA_E_R2D_CN	17
TRUE	NC_SATA_F_D2RP	17
TRUE	NC_SDVO_INTN	18
TRUE	NC_SDVO_STALLP	18
TRUE	NC_SMC_BMON_MUX_SEL	
TRUE	NC_SMC_FAN_2_CTL	46
TRUE	NC_SMC_FAN_3_TACH	46
TRUE	NC_SMC_P24	46
TRUE	NC_SMC_PF5	46
TRUE	NC_SPI_DESCRIPTOR_OVERRIDE_L	46
TRUE	NC_USB_1P	19
TRUE	NC_USB_3N	19
TRUE	NC_USB_4P	19
TRUE	NC_USB_6N	19
TRUE	NC_USB_7P	19
TRUE	NC_USB_10N	19
TRUE	NC_USB_11P	19
TRUE	NC_USB_13N	19
TRUE	NC_CPU_AXG_SENSEP	
TRUE	NC_CPU_AXG_VALSENSEN	
TRUE	NC_EG_DP_T29SNK0_AUXCH_CN	
TRUE	NC_EG_DP_T29SNK0_ML_CN<3..0>	
TRUE	NC_FB_A0_A<8..0>	75
TRUE	NC_FB_A0_CAS_L	75
TRUE	NC_FB_A0_CLKN	75
TRUE	NC_FB_A0_CS_L	75
TRUE	NC_FB_A0_DQ<31..0>	75
TRUE	NC_FB_A0_RAS_L	75
TRUE	NC_FB_A0_WCLKP<1..0>	75
TRUE	NC_FB_A1_A<8..0>	75
TRUE	NC_FB_A1_CAS_L	75
TRUE	NC_FB_A1_CLKN	75
TRUE	NC_FB_A1_CS_L	75
TRUE	NC_FB_A1_DQ<31..0>	75
TRUE	NC_FB_A1_RAS_L	75
TRUE	NC_FB_A1_WCLKP<1..0>	75
TRUE	NC_EDP_HPD	10

NO_TEST

TRUE	NC_AUD_HP_PORT_L	53
TRUE	NC_AUD_LO3_P_R	53
TRUE	NC_BCM57765_CE_L_MS_INS_L	37
TRUE	NC_CLINK_RESET_L	17
TRUE	NC_CRT_IG_DDC_DATA	18
TRUE	NC_CRT_IG_RED	18
TRUE	NC_CS4206_MICBIAS	53
TRUE	NC_EDP_AUXP	10
TRUE	NC_FW_P1_TPAN	39
TRUE	NC_FW_P2_TPAN	39
TRUE	NC_GPIO35	20
TRUE	NC_HDA_SDIN2	17
TRUE	NC_IG_D_AUXP	18
TRUE	NC_IG_DP_T29SNK0_CTRL_CLK	8
TRUE	NC_IG_DP_T29SNK0_ML_CN<3..0>	8
TRUE	NC_IRUC_P03	44
TRUE	NC_IRUC_P13	44
TRUE	NC_IRUC_P16	44
TRUE	NC_LVDS_IG_A_CLKP	19
TRUE	NC_LVDS_IG_B_CLKN	19
TRUE	NC_LVDS_IG_B_DATAP<3..0>	19
TRUE	NC_LVDS_IG_CTRL_CLK	19
TRUE	NC_LVDS_IG_DDC_DATA	19
TRUE	NC_LVDS_IG_VREFL	19
TRUE	NC_OBSFN_C0	24
TRUE	NC_PCH_CLKOUT_DPN	17
TRUE	NC_PCH_GPIO65_CLKOUTFLEX1	17
TRUE	NC_PCH_LVDS_IBG	19
TRUE	NC_PCIE_4_D2RN	17
TRUE	NC_PCIE_4_R2D_CP	17
TRUE	NC_PCIE_5_R2D_CN	17
TRUE	NC_PCIE_6_D2RP	17
TRUE	NC_PCIE_7_D2RN	17
TRUE	NC_PCIE_7_R2D_CP	17
TRUE	NC_PCIE_8_R2D_CN	17
TRUE	NC_PCIE_CLK100M_EXCARDP	17
TRUE	NC_PCIE_CLK100M_PE6N	20
TRUE	NC_PCIE_CLK100M_PE7P	20
TRUE	NC_PCIE_CLK100M_T29N	
TRUE	NC_PCIE_T29_D2RP<3..0>	
TRUE	NC_PEG_CLK100MN	
TRUE	NC_PEG_D2RN<15..12>	10
TRUE	NC_PEG_R2D_CN<7..0>	
TRUE	NC_PEG_R2D_CP<15..12>	10
TRUE	NC_SATA_C_R2D_CN	17
TRUE	NC_SATA_D_D2RP	17
TRUE	NC_SATA_E_D2RN	17
TRUE	NC_SATA_E_R2D_CP	17
TRUE	NC_SATA_F_R2D_CN	17
TRUE	NC_SDVO_INTP	18
TRUE	NC_SDVO_TVCLKINN	18
TRUE	NC_SMC_FAN_1_CTL	46
TRUE	NC_SMC_FAN_2_TACH	46
TRUE	NC_SMC_P10	46
TRUE	NC_SMC_P41	46
TRUE	NC_SMC_RSTGATE_L	46
TRUE	NC_T29_PWR_EN	
TRUE	NC_USB_2N	19
TRUE	NC_USB_3P	19
TRUE	NC_USB_5N	19
TRUE	NC_USB_6P	19
TRUE	NC_USB_9N	19
TRUE	NC_USB_10P	19
TRUE	NC_USB_12N	19
TRUE	NC_USB_13P	19
TRUE	NC_T29_R2D_CP1	83
TRUE	NC_T29_R2D_CP0	83
TRUE	NC_T29_R2D_CN1	83
TRUE	NC_T29_R2D_CN0	83
TRUE	NC_T29_PCIE_RESET3_L	83
TRUE	NC_T29_PCIE_RESET2_L	83
TRUE	NC_T29_PCIE_RESET1_L	83
TRUE	NC_T29_PCIE_RESET0_L	83
TRUE	NC_T29_D2RP1	83
TRUE	NC_T29_D2RP0	83
TRUE	NC_T29_D2RN1	83
TRUE	NC_T29_D2RN0	83
TRUE	NC_DP_T29SRC_ML_CP<3..0>	83
TRUE	NC_DP_T29SRC_ML_CN<3..0>	83
TRUE	NC_DP_T29SRC_AUXCH_CP	83
TRUE	NC_DP_T29SRC_AUXCH_CN	83
TRUE	NC_DP_T29SNK1_MLP<3..0>	
TRUE	NC_DP_T29SNK1_MLN<3..0>	
TRUE	NC_DP_T29SNK1_AUXCHP	
TRUE	NC_DP_T29SNK1_AUXCHN	

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Title: Basenet Report
Design: mlb
Date: Apr 7 20:19:40 2011

Base nets and synonyms for mlb_lib.MLB(@mlb_lib.mlb(sch_1))

Base Signal	Synonyms	Location([Zone][dir])
1V05_S0_LDO_EN	1V05_S0_LDO_EN - @mlb_lib.MLB	62C1
	CPUVCCIOS0_EN - @mlb_lib.MLB	62C1 70C6
3V3R2V8_DPAPWR_ADJ	3V3R2V8_DPAPWR_ADJ - @mlb_lib.MLB	87D7
3V3R2V8_SS_A	3V3R2V8_SS_A - @mlb_lib.MLB	87D8
80101A_NC	80101A_NC - @mlb_lib.MLB	87C8
=FDI_DATA_N<0>	=FDI_DATA_N<0> - @mlb_lib.MLB	10C8
	NC_FDI_CPU_DATAN<7..0> -	8D2
	@mlb_lib.MLB	
=FDI_DATA_N<7..0>	=FDI_DATA_N<7..0> - @mlb_lib.MLB	8D5
	NC_FDI_CPU_DATAN<7..0> -	8D2
	@mlb_lib.MLB	
=FDI_DATA_N<1>	=FDI_DATA_N<1> - @mlb_lib.MLB	10C8
	NC_FDI_CPU_DATAN<7..0> -	8D2
	@mlb_lib.MLB	
=FDI_DATA_N<2>	=FDI_DATA_N<2> - @mlb_lib.MLB	10C8
	NC_FDI_CPU_DATAN<7..0> -	8D2
	@mlb_lib.MLB	
=FDI_DATA_N<3>	=FDI_DATA_N<3> - @mlb_lib.MLB	10C8
	NC_FDI_CPU_DATAN<7..0> -	8D2
	@mlb_lib.MLB	
=FDI_DATA_N<4>	=FDI_DATA_N<4> - @mlb_lib.MLB	10C8
	NC_FDI_CPU_DATAN<7..0> -	8D2
	@mlb_lib.MLB	
=FDI_DATA_N<5>	=FDI_DATA_N<5> - @mlb_lib.MLB	10C8
	NC_FDI_CPU_DATAN<7..0> -	8D2
	@mlb_lib.MLB	
=FDI_DATA_N<6>	=FDI_DATA_N<6> - @mlb_lib.MLB	10C8
	NC_FDI_CPU_DATAN<7..0> -	8D2
	@mlb_lib.MLB	
=FDI_DATA_N<7>	=FDI_DATA_N<7> - @mlb_lib.MLB	10C8
	NC_FDI_CPU_DATAN<7..0> -	8D2
	@mlb_lib.MLB	
=FDI_DATA_P<0>	=FDI_DATA_P<0> - @mlb_lib.MLB	10C8
	NC_FDI_CPU_DATAP<7..0> -	8D2
	@mlb_lib.MLB	
=FDI_DATA_P<7..0>	=FDI_DATA_P<7..0> - @mlb_lib.MLB	8D5
	NC_FDI_CPU_DATAP<7..0> -	8D2
	@mlb_lib.MLB	
=FDI_DATA_P<1>	=FDI_DATA_P<1> - @mlb_lib.MLB	10C8
	NC_FDI_CPU_DATAP<7..0> -	8D2
	@mlb_lib.MLB	
=FDI_DATA_P<2>	=FDI_DATA_P<2> - @mlb_lib.MLB	10C8
	NC_FDI_CPU_DATAP<7..0> -	8D2
	@mlb_lib.MLB	
=FDI_DATA_P<3>	=FDI_DATA_P<3> - @mlb_lib.MLB	10C8
	NC_FDI_CPU_DATAP<7..0> -	8D2
	@mlb_lib.MLB	
=FDI_DATA_P<4>	=FDI_DATA_P<4> - @mlb_lib.MLB	10C8
	NC_FDI_CPU_DATAP<7..0> -	8D2
	@mlb_lib.MLB	
=FDI_DATA_P<5>	=FDI_DATA_P<5> - @mlb_lib.MLB	10C8
	NC_FDI_CPU_DATAP<7..0> -	8D2
	@mlb_lib.MLB	
=FDI_DATA_P<6>	=FDI_DATA_P<6> - @mlb_lib.MLB	10C8
	NC_FDI_CPU_DATAP<7..0> -	8D2
	@mlb_lib.MLB	
=FDI_DATA_P<7>	=FDI_DATA_P<7> - @mlb_lib.MLB	10C8
	NC_FDI_CPU_DATAP<7..0> -	8D2
	@mlb_lib.MLB	
=FDI_INT	=FDI_INT - @mlb_lib.MLB	8D5 10C8
	PD_FDI_CPU_INT - @mlb_lib.MLB	8D3
=I2C_DPSDRVA_SCL	=I2C_DPSDRVA_SCL - @mlb_lib.MLB	49B1 49B6 86B7
	I2C_DPSDRVA_SCL - @mlb_lib.MLB	49B2 49B7
=I2C_DPSDRVA_SDA	=I2C_DPSDRVA_SDA - @mlb_lib.MLB	49B1 49B6 86B7
	I2C_DPSDRVA_SDA - @mlb_lib.MLB	49B2 49B7
=IG_DP_EXTA_AUXCH_C_N	=IG_DP_EXTA_AUXCH_C_N -	8C5 18D1
	@mlb_lib.MLB	
	NC_IG_DP_EXTA_AUXCH_CN -	8C2
	@mlb_lib.MLB	
=IG_DP_EXTA_AUXCH_C_P	=IG_DP_EXTA_AUXCH_C_P -	8C5 18D1
	@mlb_lib.MLB	
	NC_IG_DP_EXTA_AUXCH_CP -	8C2
	@mlb_lib.MLB	
=IG_DP_EXTA_DDC_CLK	=IG_DP_EXTA_DDC_CLK - @mlb_lib.MLB	8C5 18D1
	NC_IG_DP_EXTA_DDC_CLK -	8C2
	@mlb_lib.MLB	
=IG_DP_EXTA_DDC_DATA	=IG_DP_EXTA_DDC_DATA - @mlb_lib.MLB	8C5 18D1
	NC_IG_DP_EXTA_DDC_DATA -	8C2
	@mlb_lib.MLB	
=IG_DP_EXTA_HPD	=IG_DP_EXTA_HPD - @mlb_lib.MLB	8C5 18D1
	NC_IG_DP_EXTA_HPD - @mlb_lib.MLB	8C2
=IG_DP_EXTA_ML_C_N<0>	=IG_DP_EXTA_ML_C_N<0> -	18D1
	@mlb_lib.MLB	
	NC_IG_DP_EXTA_ML_CN<3..0> -	8C2
	@mlb_lib.MLB	
=IG_DP_EXTA_ML_C_N<3..0>	=IG_DP_EXTA_ML_C_N<3..0> -	8C5
	@mlb_lib.MLB	
	NC_IG_DP_EXTA_ML_CN<3..0> -	8C2
	@mlb_lib.MLB	
=IG_DP_EXTA_ML_C_N<1>	=IG_DP_EXTA_ML_C_N<1> -	18C1
	@mlb_lib.MLB	
	NC_IG_DP_EXTA_ML_CN<3..0> -	8C2
	@mlb_lib.MLB	
=IG_DP_EXTA_ML_C_N<2>	=IG_DP_EXTA_ML_C_N<2> -	18C1
	@mlb_lib.MLB	
	NC_IG_DP_EXTA_ML_CN<3..0> -	8C2
	@mlb_lib.MLB	
=IG_DP_EXTA_ML_C_N<3>	=IG_DP_EXTA_ML_C_N<3> -	18C1
	@mlb_lib.MLB	
	NC_IG_DP_EXTA_ML_CN<3..0> -	8C2
	@mlb_lib.MLB	
=IG_DP_EXTA_ML_C_P<0>	=IG_DP_EXTA_ML_C_P<0> -	18D1
	@mlb_lib.MLB	
	NC_IG_DP_EXTA_ML_CP<3..0> -	8C2
	@mlb_lib.MLB	
=IG_DP_EXTA_ML_C_P<3>	=IG_DP_EXTA_ML_C_P<3..0> -	8C5
	@mlb_lib.MLB	
	NC_IG_DP_EXTA_ML_CP<3..0> -	8C2
	@mlb_lib.MLB	
=IG_DP_EXTA_ML_C_P<1>	=IG_DP_EXTA_ML_C_P<1> -	18C1
	@mlb_lib.MLB	
	NC_IG_DP_EXTA_ML_CP<3..0> -	8C2
	@mlb_lib.MLB	
=IG_DP_EXTA_ML_C_P<2>	=IG_DP_EXTA_ML_C_P<2> -	18C1
	@mlb_lib.MLB	
	NC_IG_DP_EXTA_ML_CP<3..0> -	8C2
	@mlb_lib.MLB	
=IG_DP_EXTA_ML_C_P<3>	=IG_DP_EXTA_ML_C_P<3> -	18C1
	@mlb_lib.MLB	
	NC_IG_DP_EXTA_ML_CP<3..0> -	8C2
	@mlb_lib.MLB	
=IG_DP_EXTA_ML_C_P<3>	=IG_DP_EXTA_ML_C_P<3> -	18C1
	@mlb_lib.MLB	
	NC_IG_DP_EXTA_ML_CP<3..0> -	8C2
	@mlb_lib.MLB	
=IG_HDMI_CLK_C_N	=IG_HDMI_CLK_C_N - @mlb_lib.MLB	8C5 18B1
	NC_IG_HDMI_CLK_CN - @mlb_lib.MLB	8C2
=IG_HDMI_CLK_C_P	=IG_HDMI_CLK_C_P - @mlb_lib.MLB	8C5 18B1
	NC_IG_HDMI_CLK_CP - @mlb_lib.MLB	8C2
=IG_HDMI_DATA_C_N<0>	=IG_HDMI_DATA_C_N<0> - @mlb_lib.MLB	18B1
	NC_IG_HDMI_DATA_CN<2..0> -	8C2
	@mlb_lib.MLB	
=IG_HDMI_DATA_C_N<2..0>	=IG_HDMI_DATA_C_N<2..0> -	8C5
	@mlb_lib.MLB	
	NC_IG_HDMI_DATA_CN<2..0> -	8C2
	@mlb_lib.MLB	
=IG_HDMI_DATA_C_N<1>	=IG_HDMI_DATA_C_N<1> - @mlb_lib.MLB	18B1
	NC_IG_HDMI_DATA_CN<2..0> -	8C2
	@mlb_lib.MLB	
=IG_HDMI_DATA_C_N<2>	=IG_HDMI_DATA_C_N<2> - @mlb_lib.MLB	18B1
	NC_IG_HDMI_DATA_CN<2..0> -	8C2
	@mlb_lib.MLB	
=IG_HDMI_DATA_C_P<0>	=IG_HDMI_DATA_C_P<0> - @mlb_lib.MLB	18B1
	NC_IG_HDMI_DATA_CP<2..0> -	8C2
	@mlb_lib.MLB	
=IG_HDMI_DATA_C_P<2..0>	=IG_HDMI_DATA_C_P<2..0> -	8C5
	@mlb_lib.MLB	
	NC_IG_HDMI_DATA_CP<2..0> -	8C2
	@mlb_lib.MLB	
=IG_HDMI_DATA_C_P<1>	=IG_HDMI_DATA_C_P<1> - @mlb_lib.MLB	18B1
	NC_IG_HDMI_DATA_CP<2..0> -	8C2
	@mlb_lib.MLB	
=IG_HDMI_DATA_C_P<2>	=IG_HDMI_DATA_C_P<2> - @mlb_lib.MLB	18B1
	NC_IG_HDMI_DATA_CP<2..0> -	8C2
	@mlb_lib.MLB	
=IG_HDMI_LS_HPD	=IG_HDMI_LS_HPD - @mlb_lib.MLB	8C5 18B1
	NC_IG_HDMI_LS_HPD - @mlb_lib.MLB	8C2
=IG_HDMI_LS_SCL	=IG_HDMI_LS_SCL - @mlb_lib.MLB	8C5 18C1
	NC_IG_HDMI_LS_SCL - @mlb_lib.MLB	8C2
=IG_HDMI_LS_SDA	=IG_HDMI_LS_SDA - @mlb_lib.MLB	8C5 18C1
	NC_IG_HDMI_LS_SDA - @mlb_lib.MLB	8C2
=PLT_RST_T29_GPU	=PLT_RST_T29_GPU - @mlb_lib.MLB	27C1 73B4 85C8
	PLT_RST_BUF_L - @mlb_lib.MLB	27C3
=SMC_GFX_THROTTLE_L	=SMC_GFX_THROTTLE_L - @mlb_lib.MLB	8B5 46C8
	SMC_GFX_THROTTLE_L - @mlb_lib.MLB	8B2 80B2
ALL_SYS_PWRGD	ALL_SYS_PWRGD - @mlb_lib.MLB	27A8 46D8 62A5 62C5 62C6
		76C8
ALL_SYS_PWRGD_R	ALL_SYS_PWRGD_R - @mlb_lib.MLB	62A6
AMBIENT_THRMD_N	AMBIENT_THRMD_N - @mlb_lib.MLB	52B3 52C8
AMBIENT_THRMD_P	AMBIENT_THRMD_P - @mlb_lib.MLB	52B3 52C8
AP_CLKREQ_L	AP_CLKREQ_L - @mlb_lib.MLB	17B4 17B5 35A3
AP_CLKREQ_Q_L	AP_CLKREQ_Q_L - @mlb_lib.MLB	35A4 100D7
AP_PWR_EN	AP_PWR_EN - @mlb_lib.MLB	19C1 24D4 35A3 62A4
AP_RESET_CONN_L	AP_RESET_CONN_L - @mlb_lib.MLB	35B4 100D7
AP_RESET_L	AP_RESET_L - @mlb_lib.MLB	27D1 35B3
AUD_4V5_REG_IN	AUD_4V5_REG_IN - @mlb_lib.MLB	53A6
AUD_CONNJ1_MIC_HI	AUD_CONNJ1_MIC_HI - @mlb_lib.MLB	57D7
AUD_CONNJ1_PERIPHDET	AUD_CONNJ1_PERIPHDET - @mlb_lib.MLB	57C7
AUD_CONNJ1_RING	AUD_CONNJ1_RING - @mlb_lib.MLB	57D7
AUD_CONNJ1_SLEEVE	AUD_CONNJ1_SLEEVE - @mlb_lib.MLB	57C7
AUD_CONNJ1_SLEEVEDET	AUD_CONNJ1_SLEEVEDET - @mlb_lib.MLB	57D7
AUD_CONNJ1_TIP	AUD_CONNJ1_TIP - @mlb_lib.MLB	57D7
AUD_CONNJ1_TIPDET	AUD_CONNJ1_TIPDET - @mlb_lib.MLB	57C7
AUD_CONNJ2_RING	AUD_CONNJ2_RING - @mlb_lib.MLB	57B6
AUD_CONNJ2_SLEEVE	AUD_CONNJ2_SLEEVE - @mlb_lib.MLB	57B6
AUD_CONNJ2_TIP	AUD_CONNJ2_TIP - @mlb_lib.MLB	57B6
AUD_CONNJ2_TIPDET	AUD_CONNJ2_TIPDET - @mlb_lib.MLB	57B6
AUD_GPIO_1	AUD_GPIO_1 - @mlb_lib.MLB	53D7 55B6
AUD_GPIO_3	AUD_GPIO_3 - @mlb_lib.MLB	53C7 56B7
AUD_HPAMP_INL_N	AUD_HPAMP_INL_N - @mlb_lib.MLB	55C5
AUD_HPAMP_INL_P	AUD_HPAMP_INL_P - @mlb_lib.MLB	55C5
AUD_HPAMP_INR_N	AUD_HPAMP_INR_N - @mlb_lib.MLB	55B5
AUD_HPAMP_INR_P	AUD_HPAMP_INR_P - @mlb_lib.MLB	55C5
AUD_HPAMP_MUTE_L	AUD_HPAMP_MUTE_L - @mlb_lib.MLB	55B5
AUD_HPAMP_OUTL	AUD_HPAMP_OUTL - @mlb_lib.MLB	55C1 55C5 57D3
AUD_HPAMP_OUTR	AUD_HPAMP_OUTR - @mlb_lib.MLB	55B1 55B5 57D3
AUD_HPAMP_RETURN	AUD_HPAMP_RETURN - @mlb_lib.MLB	55B1 57C3
AUD_HPREF	AUD_HPREF - @mlb_lib.MLB	53D3
AUD_I2C_INT_L	AUD_I2C_INT_L - @mlb_lib.MLB	19D6 58D5
AUD_INJACK_INSERT_L	AUD_INJACK_INSERT_L - @mlb_lib.MLB	58A5
AUD_IPHS_SWITCH_EN	AUD_IPHS_SWITCH_EN - @mlb_lib.MLB	20B1 58D5
AUD_IPHS_SWITCH_EN_P	AUD_IPHS_SWITCH_EN_PCH -	20A1 20B3 20D6
CH	@mlb_lib.MLB	
AUD_IP_PERIPHERAL_DE	AUD_IP_PERIPHERAL_DET -	19D6 58B1
T	@mlb_lib.MLB	
AUD_J1_DET_RC	AUD_J1_DET_RC - @mlb_lib.MLB	58B7
AUD_J1_PERIPHDET	AUD_J1_PERIPHDET - @mlb_lib.MLB	57C3 58A4
AUD_J1_PERIPHDET_INV	AUD_J1_PERIPHDET_INV - @mlb_lib.MLB	58A2
AUD_J1_SLEEVEDET	AUD_J1_SLEEVEDET - @mlb_lib.MLB	57D3 58C6 58C8
AUD_J1_SLEEVEDET_INV	AUD_J1_SLEEVEDET_INV - @mlb_lib.MLB	58C7
AUD_J1_TIPDET	AUD_J1_TIPDET - @mlb_lib.MLB	57C3 58B8
AUD_J2_DET_RC	AUD_J2_DET_RC - @mlb_lib.MLB	58A6
AUD_J2_OPT_OUT	AUD_J2_OPT_OUT - @mlb_lib.MLB	57B6
AUD_J2_TIPDET_R	AUD_J2_TIPDET_R - @mlb_lib.MLB	57B3 58A7
AUD_LI_GND	AUD_LI_GND - @mlb_lib.MLB	54C6 57B3
AUD_LI_INL	AUD_LI_INL - @mlb_lib.MLB	54D6 57B3
AUD_LI_INR	AUD_LI_INR - @mlb_lib.MLB	54C6 57B3
AUD_LI_LF	AUD_LI_LF - @mlb_lib.MLB	54D5
AUD_LI_N_LR	AUD_LI_N_LR - @mlb_lib.MLB	53C2 54C3
AUD_LI_P_L	AUD_LI_P_L - @mlb_lib.MLB	53C2 54D3
AUD_LI_P_R	AUD_LI_P_R - @mlb_lib.MLB	53C2 54C3
AUD_LI_RF	AUD_LI_RF - @mlb_lib.MLB	54C5
AUD_LO2_N_L	AUD_LO2_N_L - @mlb_lib.MLB	53D2 55C8
AUD_LO2_N_R	AUD_LO2_N_R - @mlb_lib.MLB	53C2 55B8
AUD_LO2_P_L	AUD_LO2_P_L - @mlb_lib.MLB	53D2 55C8
AUD_LO2_P_R	AUD_LO2_P_R - @mlb_lib.MLB	53D2 55B8
AUD_LO3_N_L	AUD_LO3_N_L - @mlb_lib.MLB	53C2 56C7
AUD_LO3_P_L	AUD_LO3_P_L - @mlb_lib.MLB	53C2 56B7
AUD_MIC_INN_L	AUD_MIC_INN_L - @mlb_lib.MLB	53C2 58C4
AUD_MIC_INP_L	AUD_MIC_INP_L - @mlb_lib.MLB	53C2 58C4
AUD_OUTJACK_INSERT_L	AUD_OUTJACK_INSERT_L - @mlb_lib.MLB	58B6
AUD_PERIPH_DET_R	AUD_PERIPH_DET_R - @mlb_lib.MLB	58B2
AUD_PORT_D_DET_L	AUD_PORT_D_DET_L - @mlb_lib.MLB	58C5
AUD_PORT_G_DET_L	AUD_PORT_G_DET_L - @mlb_lib.MLB	58C5
AUD_REG_SHDN_L	AUD_REG_SHDN_L - @mlb_lib.MLB	53A7
AUD_SDI_R	AUD_SDI_R - @mlb_lib.MLB	53C6 93C3
AUD_SENSE_A	AUD_SENSE_A - @mlb_lib.MLB	53C7 58A7 58C8
AUD_SPDIF_IN	AUD_SPDIF_IN - @mlb_lib.MLB	53C7 57B3
AUD_SPDIF_OUT	AUD_SPDIF_OUT - @mlb_lib.MLB	53C7 57C3
AUD_SPKRAMP_INL	AUD_SPKRAMP_INL - @mlb_lib.MLB	56B6
AUD_SPKRAMP_INL_L	AUD_SPKRAMP_INL_L - @mlb_lib.MLB	56B7
AUD_SPKRAMP_INR	AUD_SPKRAMP_INR - @mlb_lib.MLB	56C6
AUD_SPKRAMP_INR_L	AUD_SPKRAMP_INR_L - @mlb_lib.MLB	56C7
AUD_SPKRAMP_SD_H	AUD_SPKRAMP_SD_H - @mlb_lib.MLB	56B7
BCM5764_CLK25M_XTALI	BCM5764_CLK25M_XTALI - @mlb_lib.MLB	26C1 37B6 94D3
	SYSCLK_CLK25M_ENET - @mlb_lib.MLB	26C3
BCM5764_CLK25M_XTALO	BCM5764_CLK25M_XTALO - @mlb_lib.MLB	26C1 37B6 94D3
	TP_ENET_CLK25M_XTALO - @mlb_lib.MLB	26C3
BCM57765_CS_L	BCM57765_CS_L - @mlb_lib.MLB	37A8 37B6
BCM57765_MISO	BCM57765_MISO - @mlb_lib.MLB	37A6 37B6
BCM57765_MOSI	BCM57765_MOSI - @mlb_lib.MLB	37A6 37B6
BCM57765_RDAC	BCM57765_RDAC - @mlb_lib.MLB	37B6
BCM57765_SCLK	BCM57765_SCLK - @mlb_lib.MLB	37A8 37B6
BCM57765_VMAIN_PRSNT	BCM57765_VMAIN_PRSNT - @mlb_lib.MLB	37C6
BCM57765_WAKE_R_L	BCM57765_WAKE_R_L - @mlb_lib.MLB	37B6
BDM57765_SR_DISABLE	BDM57765_SR_DISABLE - @mlb_lib.MLB	37B4
BOOT_1V8S0	BOOT_1V8S0 - @mlb_lib.MLB	71C6
CATERR_LED	CATERR_LED - @mlb_lib.MLB	6B1
CATERR_LED_R	CATERR_LED_R - @mlb_lib.MLB	6B1
CATERR_R	CATERR_R - @mlb_lib.MLB	6B2
CIV_ENET_RESET_L	CIV_ENET_RESET_L - @mlb_lib.MLB	34B2 37B6
CLK98M_FW_XI	CLK98M_FW_XI - @mlb_lib.MLB	39C3 94B3
CLK98M_FW_XI_R	CLK98M_FW_XI_R - @mlb_lib.MLB	39C2 94B3
COMP_1V8S0	COMP_1V8S0 - @mlb_lib.MLB	71C7
COMP_RC_1V8S0	COMP_RC_1V8S0 - @mlb_lib.MLB	71C8
CPUIMVP_ISUMG_IOUT	CPUIMVP_ISUMG_IOUT - @mlb_lib.MLB	50C3
CPUIMVP_ISUMG_RN	CPUIMVP_ISUMG_RN - @mlb_lib.MLB	50B4
CPUIMVP_ISUM_IOUT	CPUIMVP_ISUM_IOUT - @mlb_lib.MLB	50D3
CPUIMVP_ISUM_RN	CPUIMVP_ISUM_RN - @mlb_lib.MLB	50D4
CPUTHMSNS_D2_N	CPUTHMSNS_D2_N - @mlb_lib.MLB	98B1
CPUTHMSNS_D2_P	CPUTHMSNS_D2_P - @mlb_lib.MLB	98B1
CPUVCCIOS0_AGND	CPUVCCIOS0_AGND - @mlb_lib.MLB	70B6
CPUVCCIOS0_CS_N	CPUVCCIOS0_CS_N - @mlb_lib.MLB	50B8 70B2 98D3
CPUVCCIOS0_CS_P	CPUVCCIOS0_CS_P - @mlb_lib.MLB	50B8 70B2 98D3
CPUVCCIOS0_DRVH	CPUVCCIOS0_DRVH - @mlb_lib.MLB	70C5
CPUVCCIOS0_DRVL	CPUVCCIOS0_DRVL - @mlb_lib.MLB	70C5
CPUVCCIOS0_FB	CPUVCCIOS0_FB - @mlb_lib.MLB	70C6
CPUVCCIOS0_FSEL	CPUVCCIOS0_FSEL - @mlb_lib.MLB	70B6
CPUVCCIOS0_LL	CPUVCCIOS0_LL - @mlb_lib.MLB	70C5
CPUVCCIOS0_OCSET	CPUVCCIOS0_OCSET - @mlb_lib.MLB	70C6
CPUVCCIOS0_PGOOD	CPUVCCIOS0_PGOOD - @mlb_lib.MLB	62A6 62B5 70C6
CPUVCCIOS0_RTN	CPUVCCIOS0_RTN - @mlb_lib.MLB	70C6
CPUVCCIOS0_SREF	CPUVCCIOS0_SREF - @mlb_lib.MLB	70C6
CPUVCCIOS0_VBST	CPUVCCIOS0_VBST - @mlb_lib.MLB	70C5
CPUVCCIOS0_VBST_RC	CPUVCCIOS0_VBST_RC - @mlb_lib.MLB	70C5
CPUVCCIOS0_VO	CPUVCCIOS0_VO - @mlb_lib.MLB	70C6
CPUVCCIO_IOUT	CPUVCCIO_IOUT - @mlb_lib.MLB	50B7
CPUVCCSAS0_SNUB	CPUVCCSAS0_SNUB - @mlb_lib.MLB	70C3
CPUVSENSE_IN	CPUVSENSE_IN - @mlb_lib.MLB	50C3
CPU_AXG_SENSE_N	CPU_AXG_SENSE_N - @mlb_lib.MLB	13B4 67D8 90A3
CPU_AXG_SENSE_P	CPU_AXG_SENSE_P - @mlb_lib.MLB	13B4 67D8 90A3
CPU_AXG_VALSENSE_N	CPU_AXG_VALSENSE_N - @mlb_lib.MLB	10C4 90A3
CPU_AXG_VALSENSE_P	CPU_AXG_VALSENSE_P - @mlb_lib.MLB	10C4 90A3
CPU_CATERR_L	CPU_CATERR_L - @mlb_lib.MLB	6B3 11C6 90B3
CPU_CATERR_RL	CPU_CATERR_RL - @mlb_lib.MLB	6B3
CPU_CFG<0>	CPU_CFG<0> - @mlb_lib.MLB	10A7 10D3 24C8
CPU_CFG<11..0>	CPU_CFG<11..0> - @mlb_lib.MLB	90B3
CPU_CFG<1>	CPU_CFG<1> - @mlb_lib.MLB	10A7 10D3
CPU_CFG<2>	CPU_CFG<2> - @mlb_lib.MLB	10A8 10D3
CPU_CFG<3>	CPU_CFG<3> - @mlb_lib.MLB	10A7 10D3
CPU_CFG<4>	CPU_CFG<4> - @mlb_lib.MLB	10A8 10D3
CPU_CFG<5>	CPU_CFG<5> - @mlb_lib.MLB	10A8 10D3
CPU_CFG<6>	CPU_CFG<6> - @mlb_lib.MLB	10A8 10D3
CPU_CFG<7>	CPU_CFG<7> - @mlb_lib.MLB	10A8 10D3
CPU_CFG<16>	CPU_CFG<16> - @mlb_lib.MLB	10A7 10D3
CPU_CFG<17..16>	CPU_CFG<17..16> - @mlb_lib.MLB	90B3
CPU_COMP0	CPU_COMP0 - @mlb_lib.MLB	90B3
CPU_COMP1	CPU_COMP1 - @mlb_lib.MLB	90B3
CPU_COMP2	CPU_COMP2 - @mlb_lib.MLB	90B3
CPU_COMP3	CPU_COMP3 - @mlb_lib.MLB	90B3
CPU_DC_TEST_BE59_BE6	CPU_DC_TEST_BE59_BE61 -	10C2
1	@mlb_lib.MLB	
CPU_DC_TEST_BG59_BG6	CPU_DC_TEST_BG59_BG61 -	10C2
1	@mlb_lib.MLB	
CPU_DC_TEST_C4_BE1_B	CPU_DC_TEST_C4_BE1_BG1 -	10B2
G1	@mlb_lib.MLB	
CPU_DC_TEST_C4_BE3_B	CPU_DC_TEST_C4_BE3_BG3 -	10C2
G3	@mlb_lib.MLB	
CPU_DC_TEST_C4_D3	CPU_DC_TEST_C4_D3 - @mlb_lib.MLB	10C2
CPU_DC_TEST_C59_A59	CPU_DC_TEST_C59_A59 - @mlb_lib.MLB	10C2
CPU_DC_TEST_C61_A61	CPU_DC_TEST_C61_A61 - @mlb_lib.MLB	10C2
CPU_DDR_VREF	CPU_DDR_VREF - @mlb_lib.MLB	13B1 13C1
CPU_MEM_RESET_L	CPU_MEM_RESET_L - @mlb_lib.MLB	11B6 28A8
CPU_MEM_VREFDQ_A	CPU_MEM_VREFDQ_A - @mlb_lib.MLB	10B2 10D1
CPU_MEM_VREFDQ_B	CPU_MEM_VREFDQ_B - @mlb_lib.MLB	10B2 10D1
CPU_PECI	CPU_PECI - @mlb_lib.MLB	11C6 20D3 46A4 90C3
CPU_PECI_R	CPU_PECI_R - @mlb_lib.MLB	46A5 90C3
CPU_PEG_COMP	CPU_PEG_COMP - @mlb_lib.MLB	10D5 90B3
CPU_PEG_RBIAS	CPU_PEG_RBIAS - @mlb_lib.MLB	90B3
CPU_PROCHOT_BUF	CPU_PROCHOT_BUF - @mlb_lib.MLB	47D2
CPU_PROCHOT_L	CPU_PROCHOT_L - @mlb_lib.MLB	11C7 47D4 67B6 90B3
CPU_PROCHOT_L_R	CPU_PROCHOT_L_R - @mlb_lib.MLB	47D3
CPU_PROCHOT_R_L	CPU_PROCHOT_R_L - @mlb_lib.MLB	11C6
CPU_PROC_SEL_L	CPU_PROC_SEL_L - @mlb_lib.MLB	11C6 18B4 90B3
CPU_PROX_THRM_N	CPU_PROX_THRM_N - @mlb_lib.MLB	52D3 52D8
CPU_PROX_THRM_P	CPU_PROX_THRM_P - @mlb_lib.MLB	52D3 52D8
CPU_PSI_L	CPU_PSI_L - @mlb_lib.MLB	90B3
CPU_PWRGD	CPU_PWRGD - @mlb_lib.MLB	11C6 20D3 24C8 90B3
CPU_RESET_L	CPU_RESET_L - @mlb_lib.MLB	11B7 24C3 27C1
	PLT_RST_CPU_BUF_L - @mlb_lib.MLB	27C3
CPU_SM_RCOMP<0>	CPU_SM_RCOMP<0> - @mlb_lib.MLB	11B5
CPU_SM_RCOMP<2..0>	CPU_SM_RCOMP<2..0> - @mlb_lib.MLB	90C3
CPU_SM_RCOMP<1>	CPU_SM_RCOMP<1> - @mlb_lib.MLB	11B5
CPU_SM_RCOMP<2>	CPU_SM_RCOMP<2> - @mlb_lib.MLB	11B5
CPU_THERMD_N	CPU_THERMD_N - @mlb_lib.MLB	10C4 52D2 52D8 98B1
CPU_THERMD_P	CPU_THERMD_P - @mlb_lib.MLB	10C4 52D2 52D8 98B1
CPU_VCCIOSENSE_N	CPU_VCCIOSENSE_N - @mlb_lib.MLB	13A5 70C8 90A3
CPU_VCCIOSENSE_P	CPU_VCCIOSENSE_P - @mlb_lib.MLB	13A5 70C8 90B3
CPU_VCCIO_SEL	CPU_VCCIO_SEL - @mlb_lib.MLB	13B7
CPU_VCCSA_SENSE	CPU_VCCSA_SENSE - @mlb_lib.MLB	13C1 64C8
CPU_VCCSA_VID<0>	CPU_VCCSA_VID<0> - @mlb_lib.MLB	13C1 64A6
	PD_CPU_VCCSA_VID0 - @mlb_lib.MLB	64A5
CPU_VCCSA_VID<1>	CPU_VCCSA_VID<1> - @mlb_lib.MLB	13C1 64B6 90C3
CPU_VCCSENSE_N	CPU_VCCSENSE_N - @mlb_lib.MLB	13A5 67A8 90B3
CPU_VCCSENSE_P	CPU_VCCSENSE_P - @mlb_lib.MLB	13A5 67A8 90B3
CPU_VCC_VALSENSE_N	CPU_VCC_VALSENSE_N - @mlb_lib.MLB	10C4 90A3
CPU_VCC_VALSENSE_P	CPU_VCC_VALSENSE_P - @mlb_lib.MLB	10C4 90A3
CPU_VIDALERT_L	CPU_VIDALERT_L - @mlb_lib.MLB	13B5 67B6 90C3
CPU_VIDALERT_L_R	CPU_VIDALERT_L_R - @mlb_lib.MLB	13B6 90C3
CPU_VIDSCLK	CPU_VIDSCLK - @mlb_lib.MLB	13B5 67C6 90C3
CPU_VIDSCLK_R	CPU_VIDSCLK_R - @mlb_lib.MLB	13B6 90C3
CPU_VIDSOUT	CPU_VIDSOUT - @mlb_lib.MLB	13B5 67B6 90C3
CPU_VIDSOUT_R	CPU_VIDSOUT_R - @mlb_lib.MLB	13B6 90C3
CPU_VTTSELECT	CPU_VTTSELECT - @mlb_lib.MLB	90B3
CS4206_SPDIF_OUT	CS4206_SPDIF_OUT - @mlb_lib.MLB	53C6
CS4206_VCOM	CS4206_VCOM - @mlb_lib.MLB	53C3
CS4206_VREF_ADC	CS4206_VREF_ADC - @mlb_lib.MLB	53C3
DCINVSENS_EN_L	DCINVSENS_EN_L - @mlb_lib.MLB	51C3
DCIN_IOUT	DCIN_IOUT - @mlb_lib.MLB	51D6
DCIN_S5_VSENSE	DCIN_S5_VSENSE - @mlb_lib.MLB	51D3
DDRREG_1V8_VREF	DDRREG_1V8_VREF - @mlb_lib.MLB	66C7
DDRREG_DRVH	DDRREG_DRVH - @mlb_lib.MLB	66C6
DDRREG_DRVL	DDRREG_DRVL - @mlb_l

DP_EXTA_ML_P<0>	DP_EXTA_ML_P<0> - @mlb_lib.MLB	86C7 86D6
DP_EXTA_ML_P<3..0>	DP_EXTA_ML_P<3..0> - @mlb_lib.MLB	92C1
DP_EXTA_ML_P<1>	DP_EXTA_ML_P<1> - @mlb_lib.MLB	86C7 86D6
DP_EXTA_ML_P<2>	DP_EXTA_ML_P<2> - @mlb_lib.MLB	86C7 86D6
DP_EXTA_ML_P<3>	DP_EXTA_ML_P<3> - @mlb_lib.MLB	86C7 86D6
DP_ML_CK_N<3..0>	DP_ML_CK_N<3..0> - @mlb_lib.MLB	92C1
DP_ML_CK_P<3..0>	DP_ML_CK_P<3..0> - @mlb_lib.MLB	92C1
DP_ML_C_N<3..0>	DP_ML_C_N<3..0> - @mlb_lib.MLB	92C1
DP_ML_C_P<3..0>	DP_ML_C_P<3..0> - @mlb_lib.MLB	92C1
DP_SDRVA_AUXCH_C_N	DP_SDRVA_AUXCH_C_N - @mlb_lib.MLB	86B6 95B3
DP_SDRVA_AUXCH_C_P	DP_SDRVA_AUXCH_C_P - @mlb_lib.MLB	86B6 95B3
DP_SDRVA_AUXCH_N	DP_SDRVA_AUXCH_N - @mlb_lib.MLB	86B3 95B3
DP_SDRVA_AUXCH_P	DP_SDRVA_AUXCH_P - @mlb_lib.MLB	86B3 95B3
DP_SDRVA_HPD	DP_SDRVA_HPD - @mlb_lib.MLB	86B3
DP_SDRVA_ML_C_N<0>	DP_SDRVA_ML_C_N<0> - @mlb_lib.MLB	86C6
DP_SDRVA_ML_C_N<3..0>	DP_SDRVA_ML_C_N<3..0> - @mlb_lib.MLB	95B3
DP_SDRVA_ML_C_N<1>	DP_SDRVA_ML_C_N<1> - @mlb_lib.MLB	86C6
DP_SDRVA_ML_C_N<2>	DP_SDRVA_ML_C_N<2> - @mlb_lib.MLB	86C6
DP_SDRVA_ML_C_N<3>	DP_SDRVA_ML_C_N<3> - @mlb_lib.MLB	86C6
DP_SDRVA_ML_C_P<0>	DP_SDRVA_ML_C_P<0> - @mlb_lib.MLB	86C6
DP_SDRVA_ML_C_P<3..0>	DP_SDRVA_ML_C_P<3..0> - @mlb_lib.MLB	95B3
DP_SDRVA_ML_C_P<1>	DP_SDRVA_ML_C_P<1> - @mlb_lib.MLB	86C6
DP_SDRVA_ML_C_P<2>	DP_SDRVA_ML_C_P<2> - @mlb_lib.MLB	86C6
DP_SDRVA_ML_C_P<3>	DP_SDRVA_ML_C_P<3> - @mlb_lib.MLB	86C6
DP_SDRVA_ML_N<0>	DP_SDRVA_ML_N<0> - @mlb_lib.MLB	86C3 95B3
DP_SDRVA_ML_N<1>	DP_SDRVA_ML_N<1> - @mlb_lib.MLB	86B3 95B3
DP_SDRVA_ML_N<2>	DP_SDRVA_ML_N<2> - @mlb_lib.MLB	86C3 95B3
DP_SDRVA_ML_N<3>	DP_SDRVA_ML_N<3> - @mlb_lib.MLB	86B3 95B3
DP_SDRVA_ML_P<0>	DP_SDRVA_ML_P<0> - @mlb_lib.MLB	86C3 95B3
DP_SDRVA_ML_P<1>	DP_SDRVA_ML_P<1> - @mlb_lib.MLB	86B3 95B3
DP_SDRVA_ML_P<2>	DP_SDRVA_ML_P<2> - @mlb_lib.MLB	86C3 95B3
DP_SDRVA_ML_P<3>	DP_SDRVA_ML_P<3> - @mlb_lib.MLB	86B3 95B3
DP_SDRVA_ML_R_N<0>	DP_SDRVA_ML_R_N<0> - @mlb_lib.MLB	86C4
DP_SDRVA_ML_R_N<3..0>	DP_SDRVA_ML_R_N<3..0> - @mlb_lib.MLB	95B3
DP_SDRVA_ML_R_N<2>	DP_SDRVA_ML_R_N<2> - @mlb_lib.MLB	86C4
DP_SDRVA_ML_R_P<0>	DP_SDRVA_ML_R_P<0> - @mlb_lib.MLB	86C4
DP_SDRVA_ML_R_P<3..0>	DP_SDRVA_ML_R_P<3..0> - @mlb_lib.MLB	95B3
DP_SDRVA_ML_R_P<2>	DP_SDRVA_ML_R_P<2> - @mlb_lib.MLB	86C4
DP_T29SNK0_AUXCH_C_N	DP_T29SNK0_AUXCH_C_N - @mlb_lib.MLB	8C6 83B8 92D1
	=EG_DP_T29SNK0_AUXCH_C_N - @mlb_lib.MLB	8C8 79A3
DP_T29SNK0_AUXCH_C_P	DP_T29SNK0_AUXCH_C_P - @mlb_lib.MLB	8C6 83B8 92D1
	=EG_DP_T29SNK0_AUXCH_C_P - @mlb_lib.MLB	8C8 79A3
DP_T29SNK0_AUXCH_N	DP_T29SNK0_AUXCH_N - @mlb_lib.MLB	83B5 83B6 92D1
DP_T29SNK0_AUXCH_P	DP_T29SNK0_AUXCH_P - @mlb_lib.MLB	83B5 83B6 92D1
DP_T29SNK0_DDC_CLK	DP_T29SNK0_DDC_CLK - @mlb_lib.MLB	92C1
DP_T29SNK0_DDC_DATA	DP_T29SNK0_DDC_DATA - @mlb_lib.MLB	92C1
DP_T29SNK0_HPD	DP_T29SNK0_HPD - @mlb_lib.MLB	8B6 83B6 92C1
	=EG_DP_T29SNK0_HPD - @mlb_lib.MLB	8B8 79B6
DP_T29SNK0_ML_C_N<0>	DP_T29SNK0_ML_C_N<0> - @mlb_lib.MLB	83B8
	=EG_DP_T29SNK0_ML_C_N<3..0> - @mlb_lib.MLB	8B8
DP_T29SNK0_ML_C_N<3. .0>	DP_T29SNK0_ML_C_N<3..0> - @mlb_lib.MLB	8B6 92C1
	=EG_DP_T29SNK0_ML_C_N<3..0> - @mlb_lib.MLB	8B8
DP_T29SNK0_ML_C_N<1>	DP_T29SNK0_ML_C_N<1> - @mlb_lib.MLB	83B8
	=EG_DP_T29SNK0_ML_C_N<3..0> - @mlb_lib.MLB	8B8
DP_T29SNK0_ML_C_N<2>	DP_T29SNK0_ML_C_N<2> - @mlb_lib.MLB	83B8
	=EG_DP_T29SNK0_ML_C_N<3..0> - @mlb_lib.MLB	8B8
DP_T29SNK0_ML_C_N<3>	DP_T29SNK0_ML_C_N<3> - @mlb_lib.MLB	83B8
	=EG_DP_T29SNK0_ML_C_N<3..0> - @mlb_lib.MLB	8B8
DP_T29SNK0_ML_C_P<0>	DP_T29SNK0_ML_C_P<0> - @mlb_lib.MLB	83B8
	=EG_DP_T29SNK0_ML_C_P<3..0> - @mlb_lib.MLB	8B8
DP_T29SNK0_ML_C_P<3. .0>	DP_T29SNK0_ML_C_P<3..0> - @mlb_lib.MLB	8B6 92C1
	=EG_DP_T29SNK0_ML_C_P<3..0> - @mlb_lib.MLB	8B8
DP_T29SNK0_ML_C_P<1>	DP_T29SNK0_ML_C_P<1> - @mlb_lib.MLB	83B8
	=EG_DP_T29SNK0_ML_C_P<3..0> - @mlb_lib.MLB	8B8
DP_T29SNK0_ML_C_P<2>	DP_T29SNK0_ML_C_P<2> - @mlb_lib.MLB	83B8
	=EG_DP_T29SNK0_ML_C_P<3..0> - @mlb_lib.MLB	8B8
DP_T29SNK0_ML_C_P<3>	DP_T29SNK0_ML_C_P<3> - @mlb_lib.MLB	83B8
	=EG_DP_T29SNK0_ML_C_P<3..0> - @mlb_lib.MLB	8B8
DP_T29SNK0_ML_N<0>	DP_T29SNK0_ML_N<0> - @mlb_lib.MLB	83B5 83B6
DP_T29SNK0_ML_N<3..0>	DP_T29SNK0_ML_N<3..0> - @mlb_lib.MLB	92C1
DP_T29SNK0_ML_N<1>	DP_T29SNK0_ML_N<1> - @mlb_lib.MLB	83B5 83B6
DP_T29SNK0_ML_N<2>	DP_T29SNK0_ML_N<2> - @mlb_lib.MLB	83B5 83B6
DP_T29SNK0_ML_N<3>	DP_T29SNK0_ML_N<3> - @mlb_lib.MLB	83B5 83B6
DP_T29SNK0_ML_P<0>	DP_T29SNK0_ML_P<0> - @mlb_lib.MLB	83B5 83B6
DP_T29SNK0_ML_P<3..0>	DP_T29SNK0_ML_P<3..0> - @mlb_lib.MLB	92C1
DP_T29SNK0_ML_P<1>	DP_T29SNK0_ML_P<1> - @mlb_lib.MLB	83B5 83B6
DP_T29SNK0_ML_P<2>	DP_T29SNK0_ML_P<2> - @mlb_lib.MLB	83B5 83B6
DP_T29SNK0_ML_P<3>	DP_T29SNK0_ML_P<3> - @mlb_lib.MLB	83B5 83B6
DP_T29SNK1_AUXCH_C_N	DP_T29SNK1_AUXCH_C_N - @mlb_lib.MLB	8B6 83A8 92C1
	=EG_DP_T29SNK1_AUXCH_C_N - @mlb_lib.MLB	8B8 79A3
DP_T29SNK1_AUXCH_C_P	DP_T29SNK1_AUXCH_C_P - @mlb_lib.MLB	8B6 83A8 92C1
	=EG_DP_T29SNK1_AUXCH_C_P - @mlb_lib.MLB	8B8 79A3
DP_T29SNK1_AUXCH_N	DP_T29SNK1_AUXCH_N - @mlb_lib.MLB	83A5 83A6 92C1
DP_T29SNK1_AUXCH_P	DP_T29SNK1_AUXCH_P - @mlb_lib.MLB	83A5 83A6 92C1
DP_T29SNK1_HPD	DP_T29SNK1_HPD - @mlb_lib.MLB	8B6 83A6 92C1
	=EG_DP_T29SNK1_HPD - @mlb_lib.MLB	8B8 79B6
DP_T29SNK1_ML_C_N<0>	DP_T29SNK1_ML_C_N<0> - @mlb_lib.MLB	83A8
	=EG_DP_T29SNK1_ML_C_N<3..0> - @mlb_lib.MLB	8B8
DP_T29SNK1_ML_C_N<3. .0>	DP_T29SNK1_ML_C_N<3..0> - @mlb_lib.MLB	8B6 92C1
	=EG_DP_T29SNK1_ML_C_N<3..0> - @mlb_lib.MLB	8B8
DP_T29SNK1_ML_C_N<1>	DP_T29SNK1_ML_C_N<1> - @mlb_lib.MLB	83A8
	=EG_DP_T29SNK1_ML_C_N<3..0> - @mlb_lib.MLB	8B8
DP_T29SNK1_ML_C_N<2>	DP_T29SNK1_ML_C_N<2> - @mlb_lib.MLB	83A8
	=EG_DP_T29SNK1_ML_C_N<3..0> - @mlb_lib.MLB	8B8
DP_T29SNK1_ML_C_N<3>	DP_T29SNK1_ML_C_N<3> - @mlb_lib.MLB	83A8
	=EG_DP_T29SNK1_ML_C_N<3..0> - @mlb_lib.MLB	8B8

DP_T29SNK1_ML_C_P<0>	DP_T29SNK1_ML_C_P<0> - @mlb_lib.MLB	83A8
	=EG_DP_T29SNK1_ML_C_P<3..0> - @mlb_lib.MLB	8B8
DP_T29SNK1_ML_C_P<3.	DP_T29SNK1_ML_C_P<3..0> - @mlb_lib.MLB	8B6 92C1
.0>	=EG_DP_T29SNK1_ML_C_P<3..0> - @mlb_lib.MLB	8B8
DP_T29SNK1_ML_C_P<1>	DP_T29SNK1_ML_C_P<1> - @mlb_lib.MLB	83A8
	=EG_DP_T29SNK1_ML_C_P<3..0> - @mlb_lib.MLB	8B8
DP_T29SNK1_ML_C_P<2>	DP_T29SNK1_ML_C_P<2> - @mlb_lib.MLB	83A8
	=EG_DP_T29SNK1_ML_C_P<3..0> - @mlb_lib.MLB	8B8
DP_T29SNK1_ML_C_P<3>	DP_T29SNK1_ML_C_P<3> - @mlb_lib.MLB	83A8
	=EG_DP_T29SNK1_ML_C_P<3..0> - @mlb_lib.MLB	8B8
DP_T29SNK1_ML_N<0>	DP_T29SNK1_ML_N<0> - @mlb_lib.MLB	83A5 83A6
DP_T29SNK1_ML_N<3..0	DP_T29SNK1_ML_N<3..0> -	92C1
>	@mlb_lib.MLB	
DP_T29SNK1_ML_N<1>	DP_T29SNK1_ML_N<1> - @mlb_lib.MLB	83A6 83B5
DP_T29SNK1_ML_N<2>	DP_T29SNK1_ML_N<2> - @mlb_lib.MLB	83A6 83B5
DP_T29SNK1_ML_N<3>	DP_T29SNK1_ML_N<3> - @mlb_lib.MLB	83A6 83B5
DP_T29SNK1_ML_P<0>	DP_T29SNK1_ML_P<0> - @mlb_lib.MLB	83A6 83B5
DP_T29SNK1_ML_P<3..0	DP_T29SNK1_ML_P<3..0> -	92C1
>	@mlb_lib.MLB	
DP_T29SNK1_ML_P<1>	DP_T29SNK1_ML_P<1> - @mlb_lib.MLB	83A6 83B5
DP_T29SNK1_ML_P<2>	DP_T29SNK1_ML_P<2> - @mlb_lib.MLB	83A6 83B5
DP_T29SNK1_ML_P<3>	DP_T29SNK1_ML_P<3> - @mlb_lib.MLB	83A6 83B5
DVPDATA<0>	DVPDATA<0> - @mlb_lib.MLB	79D6
DVPDATA<1>	DVPDATA<1> - @mlb_lib.MLB	79D6
DVPDATA<2>	DVPDATA<2> - @mlb_lib.MLB	79D6
DVPDATA<3>	DVPDATA<3> - @mlb_lib.MLB	79D6
EDP_COMP	EDP_COMP - @mlb_lib.MLB	10C7
EG_BKLT_EN	EG_BKLT_EN - @mlb_lib.MLB	79C6 80A2 80B8
ENET_ASF_GPIO	ENET_ASF_GPIO - @mlb_lib.MLB	37B1 46B5
ENET_ASF_GPIO_R	ENET_ASF_GPIO_R - @mlb_lib.MLB	37B3
ENET_ASF_SMB_CLK	ENET_ASF_SMB_CLK - @mlb_lib.MLB	37B6 49D3 96D3
	=SMBUS_SMC_2_SCL - @mlb_lib.MLB	46B5 49D1
ENET_ASF_SMB_DATA	ENET_ASF_SMB_DATA - @mlb_lib.MLB	37B6 49D3 96D3
	=SMBUS_SMC_2_SDA - @mlb_lib.MLB	46B5 49D1
ENET_CENTER_TAP<0>	ENET_CENTER_TAP<0> - @mlb_lib.MLB	36B5
ENET_CENTER_TAP<3..0	ENET_CENTER_TAP<3..0> -	94D3
>	@mlb_lib.MLB	
ENET_CENTER_TAP<1>	ENET_CENTER_TAP<1> - @mlb_lib.MLB	36C4
ENET_CENTER_TAP<2>	ENET_CENTER_TAP<2> - @mlb_lib.MLB	36B5
ENET_CENTER_TAP<3>	ENET_CENTER_TAP<3> - @mlb_lib.MLB	36C4
ENET_CLKREQ_L	ENET_CLKREQ_L - @mlb_lib.MLB	17B4 17B5 37B6
ENET_CMODE_REF	ENET_CMODE_REF - @mlb_lib.MLB	36B4 94D3
ENET_CONN_CTAP	ENET_CONN_CTAP - @mlb_lib.MLB	36D5
ENET_CR_CLK	ENET_CR_CLK - @mlb_lib.MLB	37B3 94C3
ENET_CR_CMD	ENET_CR_CMD - @mlb_lib.MLB	37B3 94C3
ENET_CR_DATA<0>	ENET_CR_DATA<0> - @mlb_lib.MLB	37B3
ENET_CR_DATA<7..0>	ENET_CR_DATA<7..0> - @mlb_lib.MLB	94C3
ENET_CR_DATA<1>	ENET_CR_DATA<1> - @mlb_lib.MLB	37B3
ENET_CR_DATA<2>	ENET_CR_DATA<2> - @mlb_lib.MLB	37B3
ENET_CR_DATA<3>	ENET_CR_DATA<3> - @mlb_lib.MLB	37B3
ENET_CR_DATA<4>	ENET_CR_DATA<4> - @mlb_lib.MLB	37B3
ENET_CR_DATA<5>	ENET_CR_DATA<5> - @mlb_lib.MLB	37B3
ENET_CR_DATA<6>	ENET_CR_DATA<6> - @mlb_lib.MLB	37B3
ENET_CR_DATA<7>	ENET_CR_DATA<7> - @mlb_lib.MLB	37B3
ENET_CR_DETECT_L	ENET_CR_DETECT_L - @mlb_lib.MLB	34B2 37B1
ENET_CR_PWREN	ENET_CR_PWREN - @mlb_lib.MLB	34D4 37B3
ENET_LOW_PWR	ENET_LOW_PWR - @mlb_lib.MLB	20C1 34B5 37B6
ENET_LOW_PWR_PCH	ENET_LOW_PWR_PCH - @mlb_lib.MLB	20A1 20C3 20C6
ENET_MDI_N<0>	ENET_MDI_N<0> - @mlb_lib.MLB	36B8 37C3
ENET_MDI_N<3..0>	ENET_MDI_N<3..0> - @mlb_lib.MLB	94D3
ENET_MDI_N<1>	ENET_MDI_N<1> - @mlb_lib.MLB	36C8 37C3
ENET_MDI_N<2>	ENET_MDI_N<2> - @mlb_lib.MLB	36C8 37C3
ENET_MDI_N<3>	ENET_MDI_N<3> - @mlb_lib.MLB	36B8 37B3
ENET_MDI_P<0>	ENET_MDI_P<0> - @mlb_lib.MLB	36C8 37C3
ENET_MDI_P<3..0>	ENET_MDI_P<3..0> - @mlb_lib.MLB	94D3
ENET_MDI_P<1>	ENET_MDI_P<1> - @mlb_lib.MLB	36C8 37C3
ENET_MDI_P<2>	ENET_MDI_P<2> - @mlb_lib.MLB	36C8 37C3
ENET_MDI_P<3>	ENET_MDI_P<3> - @mlb_lib.MLB	36B8 37C3
ENET_MDI_TRAN_N<0>	ENET_MDI_TRAN_N<0> - @mlb_lib.MLB	36B3
ENET_MDI_TRAN_N<3..0	ENET_MDI_TRAN_N<3..0> -	94D3
>	@mlb_lib.MLB	
ENET_MDI_TRAN_N<1>	ENET_MDI_TRAN_N<1> - @mlb_lib.MLB	36C4
ENET_MDI_TRAN_N<2>	ENET_MDI_TRAN_N<2> - @mlb_lib.MLB	36C4
ENET_MDI_TRAN_N<3>	ENET_MDI_TRAN_N<3> - @mlb_lib.MLB	36B3
ENET_MDI_TRAN_P<0>	ENET_MDI_TRAN_P<0> - @mlb_lib.MLB	36C3
ENET_MDI_TRAN_P<3..0	ENET_MDI_TRAN_P<3..0> -	94D3
>	@mlb_lib.MLB	
ENET_MDI_TRAN_P<1>	ENET_MDI_TRAN_P<1> - @mlb_lib.MLB	36C4
ENET_MDI_TRAN_P<2>	ENET_MDI_TRAN_P<2> - @mlb_lib.MLB	36C4
ENET_MDI_TRAN_P<3>	ENET_MDI_TRAN_P<3> - @mlb_lib.MLB	36B3
ENET_MEDIA_SENSE	ENET_MEDIA_SENSE - @mlb_lib.MLB	37B1 38B5
ENET_MEDIA_SENSE_RDI	ENET_MEDIA_SENSE_RDIV -	17C8 38B3
V	@mlb_lib.MLB	
ENET_MSNS_EN	ENET_MSNS_EN - @mlb_lib.MLB	38A4
ENET_MSNS_EN_L	ENET_MSNS_EN_L - @mlb_lib.MLB	38A4
ENET_PWR_EN	ENET_PWR_EN - @mlb_lib.MLB	19C1 24D4
ENET_RESET_L	ENET_RESET_L - @mlb_lib.MLB	27D1 34B8 94D3
ENET_SR_LX	ENET_SR_LX - @mlb_lib.MLB	37D4 38D5
ENET_SR_VFB	ENET_SR_VFB - @mlb_lib.MLB	37D4 38C5
ENET_WAKE_L	ENET_WAKE_L - @mlb_lib.MLB	37B8 38C1
EXCARD_CLKREQ_L	EXCARD_CLKREQ_L - @mlb_lib.MLB	17B4 17B5
FAN0_CTL_F	FAN0_CTL_F - @mlb_lib.MLB	60C3 100D5
FAN0_TACH_F	FAN0_TACH_F - @mlb_lib.MLB	60C3 100D5
FAN_S0_EN_L	FAN_S0_EN_L - @mlb_lib.MLB	60C6
FAN_S0_EN_L_G	FAN_S0_EN_L_G - @mlb_lib.MLB	60C5
FAN_TACH0	FAN_TACH0 - @mlb_lib.MLB	60C7
FBVDD_ALTVO	FBVDD_ALTVO - @mlb_lib.MLB	76A2 79B6 80A2 80A8
FBVDD_ALTVO_L	FBVDD_ALTVO_L - @mlb_lib.MLB	76A3
FB_1V8S0	FB_1V8S0 - @mlb_lib.MLB	71C7
FB_A_VREFD	FB_A_VREFD - @mlb_lib.MLB	75A7 75B8
FB_A_VREFS	FB_A_VREFS - @mlb_lib.MLB	75A6 75B8
FB_B0_A<0>	FB_B0_A<0> - @mlb_lib.MLB	75D2 78D7
FB_B0_A<8..0>	FB_B0_A<8..0> - @mlb_lib.MLB	97D1
FB_B0_A<1>	FB_B0_A<1> - @mlb_lib.MLB	75D2 78D7
FB_B0_A<2>	FB_B0_A<2> - @mlb_lib.MLB	75D2 78D7
FB_B0_A<3>	FB_B0_A<3> - @mlb_lib.MLB	75D2 78D7
FB_B0_A<4>	FB_B0_A<4> - @mlb_lib.MLB	75D2 78D7
FB_B0_A<5>	FB_B0_A<5> - @mlb_lib.MLB	75D2 78D7
FB_B0_A<6>	FB_B0_A<6> - @mlb_lib.MLB	75D2 78D7
FB_B0_A<7>	FB_B0_A<7> - @mlb_lib.MLB	75D2 78D7
FB_B0_A<8>	FB_B0_A<8> - @mlb_lib.MLB	75B2 78C5
FB_B0_ABI_L	FB_B0_ABI_L - @mlb_lib.MLB	75C2 78C7 97D1
FB_B0_CAS_L	FB_B0_CAS_L - @mlb_lib.MLB	75B2 78D7 97D1
FB_B0_CKE_L	FB_B0_CKE_L - @mlb_lib.MLB	75B2 78D7 97D1
FB_B0_CLK_N	FB_B0_CLK_N - @mlb_lib.MLB	75C2 78D8 97D1
FB_B0_CLK_P	FB_B0_CLK_P - @mlb_lib.MLB	75C2 78D8 97D1
FB_B0_CS_L	FB_B0_CS_L - @mlb_lib.MLB	75B2 78D7 97D1
FB_B0_DBI_L<0>	FB_B0_DBI_L<0> - @mlb_lib.MLB	75C2 78D5 97C1

FB_B0_DBI_L<1>	FB_B0_DBI_L<1> - @mlb_lib.MLB	75C2 78D5 97C1
FB_B0_DBI_L<2>	FB_B0_DBI_L<2> - @mlb_lib.MLB	75C2 78D5 97C1
FB_B0_DBI_L<3>	FB_B0_DBI_L<3> - @mlb_lib.MLB	75C2 78D5 97C1
FB_B0_DQ<0>	FB_B0_DQ<0> - @mlb_lib.MLB	75D5 78D5
FB_B0_DQ<7..0>	FB_B0_DQ<7..0> - @mlb_lib.MLB	97C1
FB_B0_DQ<1>	FB_B0_DQ<1> - @mlb_lib.MLB	75D5 78D5
FB_B0_DQ<2>	FB_B0_DQ<2> - @mlb_lib.MLB	75D5 78D5
FB_B0_DQ<3>	FB_B0_DQ<3> - @mlb_lib.MLB	75D5 78D5
FB_B0_DQ<4>	FB_B0_DQ<4> - @mlb_lib.MLB	75D5 78D5
FB_B0_DQ<5>	FB_B0_DQ<5> - @mlb_lib.MLB	75D5 78D5
FB_B0_DQ<6>	FB_B0_DQ<6> - @mlb_lib.MLB	75D5 78D5
FB_B0_DQ<7>	FB_B0_DQ<7> - @mlb_lib.MLB	75D5 78D5
FB_B0_DQ<8>	FB_B0_DQ<8> - @mlb_lib.MLB	75D5 78D5
FB_B0_DQ<15..8>	FB_B0_DQ<15..8> - @mlb_lib.MLB	97C1
FB_B0_DQ<9>	FB_B0_DQ<9> - @mlb_lib.MLB	75D5 78D5
FB_B0_DQ<10>	FB_B0_DQ<10> - @mlb_lib.MLB	75D5 78D5
FB_B0_DQ<11>	FB_B0_DQ<11> - @mlb_lib.MLB	75D5 78D5
FB_B0_DQ<12>	FB_B0_DQ<12> - @mlb_lib.MLB	75D5 78D5
FB_B0_DQ<13>	FB_B0_DQ<13> - @mlb_lib.MLB	75D5 78D5
FB_B0_DQ<14>	FB_B0_DQ<14> - @mlb_lib.MLB	75D5 78D5
FB_B0_DQ<15>	FB_B0_DQ<15> - @mlb_lib.MLB	75D5 78C5
FB_B0_DQ<16>	FB_B0_DQ<16> - @mlb_lib.MLB	75D5 78C5
FB_B0_DQ<23..16>	FB_B0_DQ<23..16> - @mlb_lib.MLB	97C1
FB_B0_DQ<17>	FB_B0_DQ<17> - @mlb_lib.MLB	75D5 78C5
FB_B0_DQ<18>	FB_B0_DQ<18> - @mlb_lib.MLB	75D5 78C5
FB_B0_DQ<19>	FB_B0_DQ<19> - @mlb_lib.MLB	75D5 78C5
FB_B0_DQ<20>	FB_B0_DQ<20> - @mlb_lib.MLB	75D5 78C5
FB_B0_DQ<21>	FB_B0_DQ<21> - @mlb_lib.MLB	75D5 78C5
FB_B0_DQ<22>	FB_B0_DQ<22> - @mlb_lib.MLB	75D5 78C5
FB_B0_DQ<23>	FB_B0_DQ<23> - @mlb_lib.MLB	75D5 78C5
FB_B0_DQ<24>	FB_B0_DQ<24> - @mlb_lib.MLB	75D5 78C5
FB_B0_DQ<31..24>	FB_B0_DQ<31..24> - @mlb_lib.MLB	97C1
FB_B0_DQ<25>	FB_B0_DQ<25> - @mlb_lib.MLB	75C5 78C5
FB_B0_DQ<26>	FB_B0_DQ<26> - @mlb_lib.MLB	75C5 78C5
FB_B0_DQ<27>	FB_B0_DQ<27> - @mlb_lib.MLB	75C5 78C5
FB_B0_DQ<28>	FB_B0_DQ<28> - @mlb_lib.MLB	75C5 78C5
FB_B0_DQ<29>	FB_B0_DQ<29> - @mlb_lib.MLB	75C5 78C5
FB_B0_DQ<30>	FB_B0_DQ<30> - @mlb_lib.MLB	75C5 78C5
FB_B0_DQ<31>	FB_B0_DQ<31> - @mlb_lib.MLB	75C5 78C5
FB_B0_EDC<0>	FB_B0_EDC<0> - @mlb_lib.MLB	75C2 78C7 97D1
FB_B0_EDC<1>	FB_B0_EDC<1> - @mlb_lib.MLB	75C2 78C7 97D1
FB_B0_EDC<2>	FB_B0_EDC<2> - @mlb_lib.MLB	75C2 78C7 97D1
FB_B0_EDC<3>	FB_B0_EDC<3> - @mlb_lib.MLB	75C2 78C7 97D1
FB_B0_MF	FB_B0_MF - @mlb_lib.MLB	78D7
FB_B0_RAS_L	FB_B0_RAS_L - @mlb_lib.MLB	75B2 78D7 97D1
FB_B0_SEN	FB_B0_SEN - @mlb_lib.MLB	78D7
FB_B0_VREFC	FB_B0_VREFC - @mlb_lib.MLB	78A8 78B6
FB_B0_VREFD1	FB_B0_VREFD1 - @mlb_lib.MLB	78A8 78B6
FB_B0_VREFD2	FB_B0_VREFD2 - @mlb_lib.MLB	78A6 78A8
FB_B0_WCLK_N<0>	FB_B0_WCLK_N<0> - @mlb_lib.MLB	75D2 78C7 97C1
FB_B0_WCLK_N<1>	FB_B0_WCLK_N<1> - @mlb_lib.MLB	75D2 78C7 97C1
FB_B0_WCLK_P<0>	FB_B0_WCLK_P<0> - @mlb_lib.MLB	75D2 78C7 97C1
FB_B0_WCLK_P<1>	FB_B0_WCLK_P<1> - @mlb_lib.MLB	75D2 78C7 97C1
FB_B0_WE_L	FB_B0_WE_L - @mlb_lib.MLB	75B2 78D7 97D1
FB_B0_ZQ	FB_B0_ZQ - @mlb_lib.MLB	78D7
FB_B1_A<0>	FB_B1_A<0> - @mlb_lib.MLB	75D2 78D3
FB_B1_A<8..0>	FB_B1_A<8..0> - @mlb_lib.MLB	97D1
FB_B1_A<1>	FB_B1_A<1> - @mlb_lib.MLB	75D2 78D3
FB_B1_A<2>	FB_B1_A<2> - @mlb_lib.MLB	75D2 78D3
FB_B1_A<3>	FB_B1_A<3> - @mlb_lib.MLB	75D2 78D3
FB_B1_A<4>	FB_B1_A<4> - @mlb_lib.MLB	75D2 78D3
FB_B1_A<5>	FB_B1_A<5> - @mlb_lib.MLB	75D2 78D3
FB_B1_A<6>	FB_B1_A<6> - @mlb_lib.MLB	75D2 78D3
FB_B1_A<7>	FB_B1_A<7> - @mlb_lib.MLB	75D2 78D3
FB_B1_A<8>	FB_B1_A<8> - @mlb_lib.MLB	75B2 78C1
FB_B1_ABI_L	FB_B1_ABI_L - @mlb_lib.MLB	75C2 78C3 97D1
FB_B1_CAS_L	FB_B1_CAS_L - @mlb_lib.MLB	75B2 78D3 97D1
FB_B1_CKE_L	FB_B1_CKE_L - @mlb_lib.MLB	75B2 78D3 97D1
FB_B1_CLK_N	FB_B1_CLK_N - @mlb_lib.MLB	75B2 78D4 97D1
FB_B1_CLK_P	FB_B1_CLK_P - @mlb_lib.MLB	75C2 78D4 97D1
FB_B1_CS_L	FB_B1_CS_L - @mlb_lib.MLB	75B2 78D3 97D1
FB_B1_DBI_L<0>	FB_B1_DBI_L<0> - @mlb_lib.MLB	75C2 78D1 97C1
FB_B1_DBI_L<1>	FB_B1_DBI_L<1> - @mlb_lib.MLB	75C2 78D1 97C1
FB_B1_DBI_L<2>	FB_B1_DBI_L<2> - @mlb_lib.MLB	75C2 78D1 97C1
FB_B1_DBI_L<3>	FB_B1_DBI_L<3> - @mlb_lib.MLB	75C2 78D1 97C1
FB_B1_DQ<0>	FB_B1_DQ<0> - @mlb_lib.MLB	75C5 78D1
FB_B1_DQ<7..0>	FB_B1_DQ<7..0> - @mlb_lib.MLB	97C1
FB_B1_DQ<1>	FB_B1_DQ<1> - @mlb_lib.MLB	75C5 78D1
FB_B1_DQ<2>	FB_B1_DQ<2> - @mlb_lib.MLB	75C5 78D1
FB_B1_DQ<3>	FB_B1_DQ<3> - @mlb_lib.MLB	75C5 78D1
FB_B1_DQ<4>	FB_B1_DQ<4> - @mlb_lib.MLB	75C5 78D1
FB_B1_DQ<5>	FB_B1_DQ<5> - @mlb_lib.MLB	75C5 78D1
FB_B1_DQ<6>	FB_B1_DQ<6> - @mlb_lib.MLB	75C5 78D1
FB_B1_DQ<7>	FB_B1_DQ<7> - @mlb_lib.MLB	75C5 78D1
FB_B1_DQ<8>	FB_B1_DQ<8> - @mlb_lib.MLB	75C5 78D1
FB_B1_DQ<15..8>	FB_B1_DQ<15..8> - @mlb_lib.MLB	97C1
FB_B1_DQ<9>	FB_B1_DQ<9> - @mlb_lib.MLB	75C5 78D1
FB_B1_DQ<10>	FB_B1_DQ<10> - @mlb_lib.MLB	75C5 78D1
FB_B1_DQ<11>	FB_B1_DQ<11> - @mlb_lib.MLB	75C5 78D1
FB_B1_DQ<12>	FB_B1_DQ<12> - @mlb_lib.MLB	75C5 78D1
FB_B1_DQ<13>	FB_B1_DQ<13> - @mlb_lib.MLB	75C5 78D1
FB_B1_DQ<14>	FB_B1_DQ<14> - @mlb_lib.MLB	75C5 78D1
FB_B1_DQ<15>	FB_B1_DQ<15> - @mlb_lib.MLB	75C5 78C1
FB_B1_DQ<16>	FB_B1_DQ<16> - @mlb_lib.MLB	75C5 78C1
FB_B1_DQ<23..16>	FB_B1_DQ<23..16> -

FW_LATEVG_L	FW_LATEVG_L - @mlb_lib.MLB	41A4
FW_LATEVG_PP2V4_RC	FW_LATEVG_PP2V4_RC - @mlb_lib.MLB	41A5
FW_LATEVG_REF	FW_LATEVG_REF - @mlb_lib.MLB	41A5
FW_OC_DR	FW_OC_DR - @mlb_lib.MLB	41C7
FW_P0_TPA_C	FW_P0_TPA_C - @mlb_lib.MLB	40C3
FW_P0_TPA_L_N	FW_P0_TPA_L_N - @mlb_lib.MLB	40D2 94B3
FW_P0_TPA_L_P	FW_P0_TPA_L_P - @mlb_lib.MLB	40D3 94B3
FW_P0_TPBIAS	FW_P0_TPBIAS - @mlb_lib.MLB	39A2 40D4
FW_P0_TPB_L_N	FW_P0_TPB_L_N - @mlb_lib.MLB	40C3 94B3
FW_P0_TPB_L_P	FW_P0_TPB_L_P - @mlb_lib.MLB	40C2 94B3
FW_P12V_FETPWR	FW_P12V_FETPWR - @mlb_lib.MLB	41C6
FW_PHY_DS0	FW_PHY_DS0 - @mlb_lib.MLB	39C2 40B7
FW_PHY_DS1	FW_PHY_DS1 - @mlb_lib.MLB	39C2 40B7
FW_PHY_PC0	FW_PHY_PC0 - @mlb_lib.MLB	39C2 40A7
FW_PME_L	FW_PME_L - @mlb_lib.MLB	20B6 20D6 39B6
FW_PORT0_TPAL_N	FW_PORT0_TPAL_N - @mlb_lib.MLB	41C2 94B3
FW_PORT0_TPAL_P	FW_PORT0_TPAL_P - @mlb_lib.MLB	41C2 94B3
FW_PORT0_TPA_N	FW_PORT0_TPA_N - @mlb_lib.MLB	40C1 41C4 94B3
	FW_P0_TPA_N - @mlb_lib.MLB	39A2 40C3
FW_PORT0_TPA_P	FW_PORT0_TPA_P - @mlb_lib.MLB	40C1 41C4 94B3
	FW_P0_TPA_P - @mlb_lib.MLB	39A2 40C3
FW_PORT0_TPA_R	FW_PORT0_TPA_R - @mlb_lib.MLB	41C2
FW_PORT0_TPBL_N	FW_PORT0_TPBL_N - @mlb_lib.MLB	41C2 94B3
FW_PORT0_TPBL_P	FW_PORT0_TPBL_P - @mlb_lib.MLB	41C2 94B3
FW_PORT0_TPB_N	FW_PORT0_TPB_N - @mlb_lib.MLB	40C1 41C4 94B3
	FW_P0_TPB_N - @mlb_lib.MLB	39A2 40C3
FW_PORT0_TPB_P	FW_PORT0_TPB_P - @mlb_lib.MLB	40C1 41C4 94B3
	FW_P0_TPB_P - @mlb_lib.MLB	39A2 40C3
FW_PORT0_VP	FW_PORT0_VP - @mlb_lib.MLB	41D2 100B5
FW_PORT0_VP_F	FW_PORT0_VP_F - @mlb_lib.MLB	41D2
FW_PORTPWR_DISABLE_L	FW_PORTPWR_DISABLE_L - @mlb_lib.MLB	41A3 41C8
FW_PWR_EN	FW_PWR_EN - @mlb_lib.MLB	20B6 20C6
FW_REF_A	FW_REF_A - @mlb_lib.MLB	41B5
FW_REF_B	FW_REF_B - @mlb_lib.MLB	41B5
FW_RESET_L	FW_RESET_L - @mlb_lib.MLB	27D1 39C6
FW_SNSN	FW_SNSN - @mlb_lib.MLB	41D7
FW_SNSP	FW_SNSP - @mlb_lib.MLB	41D8
FW_V_PD	FW_V_PD - @mlb_lib.MLB	41C5
G3_POWERON_L	G3_POWERON_L - @mlb_lib.MLB	44C7 46B5 47C2
G3_POWERON_R_L	G3_POWERON_R_L - @mlb_lib.MLB	44C6
GFXCORE_N	GFXCORE_N - @mlb_lib.MLB	50A8 82C2
GFXCORE_P	GFXCORE_P - @mlb_lib.MLB	50A8 82C2
GFXCORE_S0_IOUT	GFXCORE_S0_IOUT - @mlb_lib.MLB	50A7
GFXIMVP6_AF_EN	GFXIMVP6_AF_EN - @mlb_lib.MLB	82C7
GFXIMVP6_BOOT	GFXIMVP6_BOOT - @mlb_lib.MLB	82D5
GFXIMVP6_BOOT_RC	GFXIMVP6_BOOT_RC - @mlb_lib.MLB	82D4
GFXIMVP6_COMP	GFXIMVP6_COMP - @mlb_lib.MLB	82B7
GFXIMVP6_COMP_RC	GFXIMVP6_COMP_RC - @mlb_lib.MLB	82B8
GFXIMVP6_DFB	GFXIMVP6_DFB - @mlb_lib.MLB	82B5
GFXIMVP6_DROOP	GFXIMVP6_DROOP - @mlb_lib.MLB	82B5
GFXIMVP6_FB	GFXIMVP6_FB - @mlb_lib.MLB	82B7
GFXIMVP6_FDE	GFXIMVP6_FDE - @mlb_lib.MLB	82C7
GFXIMVP6_LGATE	GFXIMVP6_LGATE - @mlb_lib.MLB	82C5
GFXIMVP6_OCSET	GFXIMVP6_OCSET - @mlb_lib.MLB	82B5
GFXIMVP6_PHASE	GFXIMVP6_PHASE - @mlb_lib.MLB	82C5
GFXIMVP6_PHASE_VSUM	GFXIMVP6_PHASE_VSUM - @mlb_lib.MLB	82C4
GFXIMVP6_RBIAS	GFXIMVP6_RBIAS - @mlb_lib.MLB	82D7
GFXIMVP6_SNUB	GFXIMVP6_SNUB - @mlb_lib.MLB	82C3
GFXIMVP6_SOFT	GFXIMVP6_SOFT - @mlb_lib.MLB	82D7
GFXIMVP6_UGATE	GFXIMVP6_UGATE - @mlb_lib.MLB	82D5
GFXIMVP6_VDIFF	GFXIMVP6_VDIFF - @mlb_lib.MLB	82B7
GFXIMVP6_VDIFF_RC	GFXIMVP6_VDIFF_RC - @mlb_lib.MLB	82B8
GFXIMVP6_VID0	GFXIMVP6_VID0 - @mlb_lib.MLB	82A5 82C7
GFXIMVP6_VID1	GFXIMVP6_VID1 - @mlb_lib.MLB	82A5 82C7
GFXIMVP6_VID2	GFXIMVP6_VID2 - @mlb_lib.MLB	82A5 82C7
GFXIMVP6_VID3	GFXIMVP6_VID3 - @mlb_lib.MLB	82A5 82C7
GFXIMVP6_VID4	GFXIMVP6_VID4 - @mlb_lib.MLB	82A5 82C7
GFXIMVP6_VIN	GFXIMVP6_VIN - @mlb_lib.MLB	82D5
GFXIMVP6_VO	GFXIMVP6_VO - @mlb_lib.MLB	82B5
GFXIMVP6_VSEN_N	GFXIMVP6_VSEN_N - @mlb_lib.MLB	82C7
GFXIMVP6_VSEN_P	GFXIMVP6_VSEN_P - @mlb_lib.MLB	82C7
GFXIMVP6_VSUM	GFXIMVP6_VSUM - @mlb_lib.MLB	82B5
GFXIMVP6_VW	GFXIMVP6_VW - @mlb_lib.MLB	82C7
GFXIMVP_IMON	GFXIMVP_IMON - @mlb_lib.MLB	90A3
GFXVSENSE_IN	GFXVSENSE_IN - @mlb_lib.MLB	50B3
GFX_DPRSLPVR	GFX_DPRSLPVR - @mlb_lib.MLB	90A3
GFX_VID<6..0>	GFX_VID<6..0> - @mlb_lib.MLB	90A3
GFX_VR_EN	GFX_VR_EN - @mlb_lib.MLB	90A3
GMUX_INT	GMUX_INT - @mlb_lib.MLB	20D6 20D8
GND_AUDIO_CODEC	GND_AUDIO_CODEC - @mlb_lib.MLB	53A3 53B7 53D1 53D2 54C6
		57C1 58A4 58A7 58A7 58B3
		58B8 58B8 58C4
GND_AUDIO_HPAMP	GND_AUDIO_HPAMP - @mlb_lib.MLB	53A3 55A6 55C7
GND_CHASSIS_AUDIO_JA	GND_CHASSIS_AUDIO_JACK -	57A3 57B3 57C3
CK	@mlb_lib.MLB	
GND_DDRREG_SGND	GND_DDRREG_SGND - @mlb_lib.MLB	66B7
GND_DPACONN_1	GND_DPACONN_1 - @mlb_lib.MLB	87C3
GND_DPACONN_7	GND_DPACONN_7 - @mlb_lib.MLB	87B3
GND_DPACONN_8	GND_DPACONN_8 - @mlb_lib.MLB	87B6
GND_DPACONN_13	GND_DPACONN_13 - @mlb_lib.MLB	87B3
GND_DPACONN_14	GND_DPACONN_14 - @mlb_lib.MLB	87B6
GND_DPACONN_19	GND_DPACONN_19 - @mlb_lib.MLB	87A3
GND_GFXIMVP6_AGND	GND_GFXIMVP6_AGND - @mlb_lib.MLB	82B5
GND_GPU_DPLL	GND_GPU_DPLL - @mlb_lib.MLB	79A8
GND_GPU_PLL	GND_GPU_PLL - @mlb_lib.MLB	74B6 74C7
GND_GPU_TSVSS	GND_GPU_TSVSS - @mlb_lib.MLB	79A8
GND_GPU_TVSSQ	GND_GPU_TVSSQ - @mlb_lib.MLB	79B4
GND_IR_F	GND_IR_F - @mlb_lib.MLB	45C2
GND_SMC_AVSS	GND_SMC_AVSS - @mlb_lib.MLB	46C2 47D6 50A3 50A3 50A5
		50A5 50B1 50B2 50B5 50B5
		50C2 50C5 50D1 50D5 51A5
		51C1 51C5 51D5
GPIO29_SLP_LAN_L	GPIO29_SLP_LAN_L - @mlb_lib.MLB	18A6 18C5
GPIO_23_NC	GPIO_23_NC - @mlb_lib.MLB	79B6 80A8
GPUTHMSNS_D_N	GPUTHMSNS_D_N - @mlb_lib.MLB	98B1
GPUTHMSNS_D_P	GPUTHMSNS_D_P - @mlb_lib.MLB	98B1
GPUVCORE_EN	GPUVCORE_EN - @mlb_lib.MLB	76A6 82C7
GPUVCORE_PGOOD	GPUVCORE_PGOOD - @mlb_lib.MLB	76C7 82C7
GPU_AC_BATT	GPU_AC_BATT - @mlb_lib.MLB	79C6 80B8
GPU_AUD_0	GPU_AUD_0 - @mlb_lib.MLB	79C4
GPU_AUD_1	GPU_AUD_1 - @mlb_lib.MLB	79C4
GPU_CLK27M	GPU_CLK27M - @mlb_lib.MLB	79A6 80C1 97B1
GPU_CLK27M_R	GPU_CLK27M_R - @mlb_lib.MLB	80C2
GPU_CLK100M	GPU_CLK100M - @mlb_lib.MLB	79A6 80C1 97B1
GPU_CLK100M_R	GPU_CLK100M_R - @mlb_lib.MLB	80C2
GPU_CLK_TEST_N	GPU_CLK_TEST_N - @mlb_lib.MLB	75B5 97B1
GPU_CLK_TEST_P	GPU_CLK_TEST_P - @mlb_lib.MLB	75B5 97B1
GPU_CLK_TEST_RC_N	GPU_CLK_TEST_RC_N - @mlb_lib.MLB	75A3
GPU_CLK_TEST_RC_P	GPU_CLK_TEST_RC_P - @mlb_lib.MLB	75A4
GPU_CONFIG_0	GPU_CONFIG_0 - @mlb_lib.MLB	79C6 80A8
GPU_CONFIG_1	GPU_CONFIG_1 - @mlb_lib.MLB	79C6 80A8
GPU_CONFIG_2	GPU_CONFIG_2 - @mlb_lib.MLB	79C6 80A8
GPU_DP_AB_CALR	GPU_DP_AB_CALR - @mlb_lib.MLB	81D5
GPU_DP_CD_CALR	GPU_DP_CD_CALR - @mlb_lib.MLB	81D7

GPU_DP_EF_CALR	GPU_DP_EF_CALR - @mlb_lib.MLB	81C7
GPU_FB_RESET_L	GPU_FB_RESET_L - @mlb_lib.MLB	75B3
GPU_GPIO_TX_DEEMP	GPU_GPIO_TX_DEEMP - @mlb_lib.MLB	79C6 80C8
GPU_I2C_SCL	GPU_I2C_SCL - @mlb_lib.MLB	79C6
GPU_I2C_SDA	GPU_I2C_SDA - @mlb_lib.MLB	79C6
GPU_JTAG_TCK	GPU_JTAG_TCK - @mlb_lib.MLB	79B6 80D8
GPU_JTAG_TDI	GPU_JTAG_TDI - @mlb_lib.MLB	79B6 80D8
GPU_JTAG_TDO	GPU_JTAG_TDO - @mlb_lib.MLB	79B6 80D8
GPU_JTAG_TMS	GPU_JTAG_TMS - @mlb_lib.MLB	79B6 80D8
GPU_JTAG_TRST_L	GPU_JTAG_TRST_L - @mlb_lib.MLB	79B6 80D8
GPU_OSC_27M_XTALIN	GPU_OSC_27M_XTALIN - @mlb_lib.MLB	80C3
GPU_OSC_27M_XTALOUT	GPU_OSC_27M_XTALOUT - @mlb_lib.MLB	80C3
GPU_PCIE_GEN2	GPU_PCIE_GEN2 - @mlb_lib.MLB	79C6 80C8
GPU_PCIE_TX_PWR	GPU_PCIE_TX_PWR - @mlb_lib.MLB	79C6 80C8
GPU_RESET_R_L	GPU_RESET_R_L - @mlb_lib.MLB	73B3
GPU_ROM_CS_L	GPU_ROM_CS_L - @mlb_lib.MLB	79B6 80A2 80C7
GPU_ROM_CS_L_R	GPU_ROM_CS_L_R - @mlb_lib.MLB	80C6
GPU_ROM_SCLK	GPU_ROM_SCLK - @mlb_lib.MLB	79C6 80A8 80C7
GPU_ROM_SCLK_R	GPU_ROM_SCLK_R - @mlb_lib.MLB	80C6
GPU_ROM_SI	GPU_ROM_SI - @mlb_lib.MLB	79C6 80B8 80C7
GPU_ROM_SI_R	GPU_ROM_SI_R - @mlb_lib.MLB	80C6
GPU_ROM_SO	GPU_ROM_SO - @mlb_lib.MLB	79C6 80B8 80C4
GPU_ROM_SO_R	GPU_ROM_SO_R - @mlb_lib.MLB	80C5
GPU_ROM_WP_L	GPU_ROM_WP_L - @mlb_lib.MLB	80C6
GPU_SMB_CLK	GPU_SMB_CLK - @mlb_lib.MLB	79C6 80A7 80B8
GPU_SMB_DAT	GPU_SMB_DAT - @mlb_lib.MLB	79C6 80B7 80B8
GPU_TDIODE_N	GPU_TDIODE_N - @mlb_lib.MLB	52B7 79A6 98B1
GPU_TDIODE_P	GPU_TDIODE_P - @mlb_lib.MLB	52B7 79A6 98B1
GPU_TEST_EN	GPU_TEST_EN - @mlb_lib.MLB	75B5
GPU_TS_FDO	GPU_TS_FDO - @mlb_lib.MLB	79A6 80A6
GPU_VCORE_VID0	GPU_VCORE_VID0 - @mlb_lib.MLB	79C6 82A8
GPU_VCORE_VID1	GPU_VCORE_VID1 - @mlb_lib.MLB	79B6 82A8
GPU_VCORE_VID2	GPU_VCORE_VID2 - @mlb_lib.MLB	79B6 82A8
GPU_VCORE_VID3	GPU_VCORE_VID3 - @mlb_lib.MLB	79B6 82A8
GPU_VDD_SENSE_N	GPU_VDD_SENSE_N - @mlb_lib.MLB	74B6 82C8
GPU_VDD_SENSE_P	GPU_VDD_SENSE_P - @mlb_lib.MLB	74B6 82C8
GPU_VREF6	GPU_VREF6 - @mlb_lib.MLB	79B6
HDA_BIT_CLK	HDA_BIT_CLK - @mlb_lib.MLB	17A4 53C7 93C3
HDA_BIT_CLK_R	HDA_BIT_CLK_R - @mlb_lib.MLB	17A5 17D8 93C3
HDA_RST_L	HDA_RST_L - @mlb_lib.MLB	17A4 53C7 93C3
HDA_RST_R_L	HDA_RST_R_L - @mlb_lib.MLB	17A5 17D8 93C3
HDA_SDIN0	HDA_SDIN0 - @mlb_lib.MLB	17D8 53C7 93C3
HDA_SDOUT	HDA_SDOUT - @mlb_lib.MLB	17A4 53C7 93C3
HDA_SDOUT_R	HDA_SDOUT_R - @mlb_lib.MLB	17A3 17A5 17C8 93C3
HDA_SYNC	HDA_SYNC - @mlb_lib.MLB	17A4 53C7 93C3
HDA_SYNC_R	HDA_SYNC_R - @mlb_lib.MLB	17A3 17A5 17D8 93C3
HDD_THRMD_N	HDD_THRMD_N - @mlb_lib.MLB	100A7
HDD_THRMD_P	HDD_THRMD_P - @mlb_lib.MLB	100A7
HDMI_CLK_CONN_N	HDMI_CLK_CONN_N - @mlb_lib.MLB	89B5 89C1 92B1
HDMI_CLK_CONN_P	HDMI_CLK_CONN_P - @mlb_lib.MLB	89C1 89C5 92B1
HDMI_CLK_C_N	HDMI_CLK_C_N - @mlb_lib.MLB	8B2 88D8 92B1
	=EG_HDMI_CLK_N - @mlb_lib.MLB	8B5 79D3
HDMI_CLK_C_P	HDMI_CLK_C_P - @mlb_lib.MLB	8B2 88D8 92B1
	=EG_HDMI_CLK_P - @mlb_lib.MLB	8B5 79D3
HDMI_CLK_LS_N	HDMI_CLK_LS_N - @mlb_lib.MLB	88D6 92B1
HDMI_CLK_LS_P	HDMI_CLK_LS_P - @mlb_lib.MLB	88D6 92B1
HDMI_CLK_N	HDMI_CLK_N - @mlb_lib.MLB	88D2 89B8 92B1
HDMI_CLK_P	HDMI_CLK_P - @mlb_lib.MLB	88D2 89C8 92B1
HDMI_DATA_CONN_N<0>	HDMI_DATA_CONN_N<0> - @mlb_lib.MLB	89C4 89D5
HDMI_DATA_CONN_N<2..0>	HDMI_DATA_CONN_N<2..0> - @mlb_lib.MLB	92B1
HDMI_DATA_CONN_P<1>	HDMI_DATA_CONN_P<1> - @mlb_lib.MLB	89C1 89D5
HDMI_DATA_CONN_P<2>	HDMI_DATA_CONN_P<2> - @mlb_lib.MLB	89C1 89C5
HDMI_DATA_C_N<0>	HDMI_DATA_C_N<0> - @mlb_lib.MLB	88C8
	=EG_HDMI_C_N<2..0> - @mlb_lib.MLB	8B5
HDMI_DATA_C_N<2..0>	HDMI_DATA_C_N<2..0> - @mlb_lib.MLB	8B2 92B1
	=EG_HDMI_C_N<2..0> - @mlb_lib.MLB	8B5
HDMI_DATA_C_N<1>	HDMI_DATA_C_N<1> - @mlb_lib.MLB	88C8
	=EG_HDMI_C_N<2..0> - @mlb_lib.MLB	8B5
HDMI_DATA_C_N<2>	HDMI_DATA_C_N<2> - @mlb_lib.MLB	88C8
	=EG_HDMI_C_N<2..0> - @mlb_lib.MLB	8B5
HDMI_DATA_C_P<0>	HDMI_DATA_C_P<0> - @mlb_lib.MLB	88D8
	=EG_HDMI_C_P<2..0> - @mlb_lib.MLB	8B5
HDMI_DATA_C_P<2..0>	HDMI_DATA_C_P<2..0> - @mlb_lib.MLB	8B2 92A1
	=EG_HDMI_C_P<2..0> - @mlb_lib.MLB	8B5
HDMI_DATA_C_P<1>	HDMI_DATA_C_P<1> - @mlb_lib.MLB	88C8
	=EG_HDMI_C_P<2..0> - @mlb_lib.MLB	8B5
HDMI_DATA_C_P<2>	HDMI_DATA_C_P<2> - @mlb_lib.MLB	88C8
	=EG_HDMI_C_P<2..0> - @mlb_lib.MLB	8B5
HDMI_DATA_LS_N<0>	HDMI_DATA_LS_N<0> - @mlb_lib.MLB	88C6
HDMI_DATA_LS_N<2..0>	HDMI_DATA_LS_N<2..0> - @mlb_lib.MLB	92A1
HDMI_DATA_LS_N<1>	HDMI_DATA_LS_N<1> - @mlb_lib.MLB	88C6
HDMI_DATA_LS_N<2>	HDMI_DATA_LS_N<2> - @mlb_lib.MLB	88C6
HDMI_DATA_LS_P<0>	HDMI_DATA_LS_P<0> - @mlb_lib.MLB	88D6
HDMI_DATA_LS_P<2..0>	HDMI_DATA_LS_P<2..0> - @mlb_lib.MLB	92A1
HDMI_DATA_LS_P<1>	HDMI_DATA_LS_P<1> - @mlb_lib.MLB	88C6
HDMI_DATA_LS_P<2>	HDMI_DATA_LS_P<2> - @mlb_lib.MLB	88C6
HDMI_DATA_N<0>	HDMI_DATA_N<0> - @mlb_lib.MLB	88C2 89D8
HDMI_DATA_N<2..0>	HDMI_DATA_N<2..0> - @mlb_lib.MLB	92A1
HDMI_DATA_N<1>	HDMI_DATA_N<1> - @mlb_lib.MLB	88C2 89C8
HDMI_DATA_N<2>	HDMI_DATA_N<2> - @mlb_lib.MLB	88C2 89C8
HDMI_DATA_P<0>	HDMI_DATA_P<0> - @mlb_lib.MLB	88D2 89D8
HDMI_DATA_P<2..0>	HDMI_DATA_P<2..0> - @mlb_lib.MLB	92A1
HDMI_DATA_P<1>	HDMI_DATA_P<1> - @mlb_lib.MLB	88C2 89D8
HDMI_DATA_P<2>	HDMI_DATA_P<2> - @mlb_lib.MLB	88C2 89C8
HDMI_DDC_CLK_5V	HDMI_DDC_CLK_5V - @mlb_lib.MLB	88C2 89B4
HDMI_DDC_CLK_CONN	HDMI_DDC_CLK_CONN - @mlb_lib.MLB	89B8 89C4
HDMI_DDC_CLK_F	HDMI_DDC_CLK_F - @mlb_lib.MLB	89B6
HDMI_DDC_DATA_5V	HDMI_DDC_DATA_5V - @mlb_lib.MLB	88C2 89B4
HDMI_DDC_DATA_CONN	HDMI_DDC_DATA_CONN - @mlb_lib.MLB	89A8 89C1
HDMI_DDC_DATA_F	HDMI_DDC_DATA_F - @mlb_lib.MLB	89B6
HDMI_HPD	HDMI_HPD - @mlb_lib.MLB	88C2 89A4
HDMI_HPD_CONN	HDMI_HPD_CONN - @mlb_lib.MLB	89A8 89C4
HDMI_HPD_Q	HDMI_HPD_Q - @mlb_lib.MLB	89A6
HDMI_LS_APD	HDMI_LS_APD - @mlb_lib.MLB	88B6
HDMI_LS_CEXT	HDMI_LS_CEXT - @mlb_lib.MLB	88B5
HDMI_LS_DDCBUF	HDMI_LS_DDCBUF - @mlb_lib.MLB	88C6
HDMI_LS_DDC_EN	HDMI_LS_DDC_EN - @mlb_lib.MLB	88C6
HDMI_LS_EMI0	HDMI_LS_EMI0 - @mlb_lib.MLB	88B4
HDMI_LS_EMI1	HDMI_LS_EMI1 - @mlb_lib.MLB	88B4
HDMI_LS_HPD	HDMI_LS_HPD - @mlb_lib.MLB	8B2 88B5 88C8 92A1
	=EG_HDMI_HPD - @mlb_lib.MLB	8B5 79B6
HDMI_LS_OE_L	HDMI_LS_OE_L - @mlb_lib.MLB	88C4
HDMI_LS_PEQ	HDMI_LS_PEQ - @mlb_lib.MLB	88B6
HDMI_LS_PIO	HDMI_LS_PIO - @mlb_lib.MLB	88C6
HDMI_LS_PRE	HDMI_LS_PRE - @mlb_lib.MLB	88C4
HDMI_LS_REXT	HDMI_LS_REXT - @mlb_lib.MLB	88B5
HDMI_LS_SCL	HDMI_LS_SCL - @mlb_lib.MLB	8B2 88A6 88C8 92A1
	=EG_HDMI_DDC_CLK - @mlb_lib.MLB	8B5 79A3

HDMI_LS_SDA	HDMI_LS_SDA - @mlb_lib.MLB	8B2 88A6 88C8 92A1
	=EG_HDMI_DDC_DATA - @mlb_lib.MLB	8B5 79A3
HPAMP_B4GAIN_INL_N	HPAMP_B4GAIN_INL_N - @mlb_lib.MLB	55C7
HPAMP_B4GAIN_INL_P	HPAMP_B4GAIN_INL_P - @mlb_lib.MLB	55C7
HPAMP_B4GAIN_INR_N	HPAMP_B4GAIN_INR_N - @mlb_lib.MLB	55B7
HPAMP_B4GAIN_INR_P	HPAMP_B4GAIN_INR_P - @mlb_lib.MLB	55B7
HPAMP_BIAS	HPAMP_BIAS - @mlb_lib.MLB	55C4
HPAMP_CN	HPAMP_CN - @mlb_lib.MLB	55B4
HPAMP_CP	HPAMP_CP - @mlb_lib.MLB	55B4
HPAMP_PVSS	HPAMP_PVSS - @mlb_lib.MLB	55B4
HS_CPUDDR_IOUT	HS_CPUDDR_IOUT - @mlb_lib.MLB	51C6
HS_GPU_IOUT	HS_GPU_IOUT - @mlb_lib.MLB	51A6
HS_MIC_BIAS	HS_MIC_BIAS - @mlb_lib.MLB	58D2
HS_MIC_HI	HS_MIC_HI - @mlb_lib.MLB	57D3 58C1
HS_MIC_HI_R	HS_MIC_HI_R - @mlb_lib.MLB	58C3
HS_MIC_LO	HS_MIC_LO - @mlb_lib.MLB	57D3 58C1
HS_RX_BP	HS_RX_BP - @mlb_lib.MLB	58D2
HS_SW_DET	HS_SW_DET - @mlb_lib.MLB	58D2
I2C_T29_SCL	I2C_T29_SCL - @mlb_lib.MLB	49B3 83A5 95C3
	=I2C_T29AMCU_SCL - @mlb_lib.MLB	49B1 86A7
I2C_T29_SDA	I2C_T29_SDA - @mlb_lib.MLB	49B3 83A5 95C3
	=I2C_T29AMCU_SDA - @mlb_lib.MLB	49B1 86A7
ICT_SEL	ICT_SEL - @mlb_lib.MLB	24A5 24A8 24B8
IRRCVR_OUT	IRRCVR_OUT - @mlb_lib.MLB	44B7 45D4 100B7
IRRCVR_OUT_RC	IRRCVR_OUT_RC - @mlb_lib.MLB	44B6
IRUC_VREG	IRUC_VREG - @mlb_lib.MLB	44C4
ISNS_HS_CPUDDR_N	ISNS_HS_CPUDDR_N - @mlb_lib.MLB	51C7
ISNS_HS_CPUDDR_P	ISNS_HS_CPUDDR_P - @mlb_lib.MLB	51C7
ISNS_HS_GPU_N	ISNS_HS_GPU_N - @mlb_lib.MLB	51A7 98C3
ISNS_HS_GPU_P	ISNS_HS_GPU_P - @mlb_lib.MLB	51A7 98C3
ISNS_P1V05PCH_N	ISNS_P1V05PCH_N - @mlb_lib.MLB	50C7
ISNS_P1V05PCH_P	ISNS_P1V05PCH_P - @mlb_lib.MLB	50C7
ISNS_P12VG3H_N	ISNS_P12VG3H_N - @mlb_lib.MLB	51D7
ISNS_P12VG3H_P	ISNS_P12VG3H_P - @mlb_lib.MLB	51D7
ISNS_VDDQ_N	ISNS_VDDQ_N - @mlb_lib.MLB	50D7
ISNS_VDDQ_P	ISNS_VDDQ_P - @mlb_lib.MLB	50D7
ISOLATE_CPU_MEM_L	ISOLATE_CPU_MEM_L - @mlb_lib.MLB	20C6 28C8
ITPCPU_CLK100M_N	ITPCPU_CLK100M_N - @mlb_lib.MLB	11C2 17A4 90C1
ITPCPU_CLK100M_P	ITPCPU_CLK100M_P - @mlb_lib.MLB	11C2 17A4 90C1
ITPXDP_CLK100M_N	ITPXDP_CLK100M_N - @mlb_lib.MLB	17A5 17B1 24C3 90C1
ITPXDP_CLK100M_P	ITPXDP_CLK100M_P - @mlb_lib.MLB	17A5 17B1 24C3 90C1
ITS_ALIVE	ITS_ALIVE - @mlb_lib.MLB	6C2
ITS_BREATHING	ITS_BREATHING - @mlb_lib.MLB	6C1
ITS_BREATHING_Q	ITS_BREATHING_Q - @mlb_lib.MLB	6C1
ITS_PLUGGED_IN	ITS_PLUGGED_IN - @mlb_lib.MLB	6C2
JTAG_GMUX_TMS	JTAG_GMUX_TMS - @mlb_lib.MLB	19D6
JTAG_ISP_TCK	JTAG_ISP_TCK - @mlb_lib.MLB	20C6 20D8 83C2
JTAG_ISP_TDI	JTAG_ISP_TDI - @mlb_lib.MLB	20A2 20C6 83C2
JTAG_ISP_TDO	JTAG_ISP_TDO - @mlb_lib.MLB	20B6 20C6 83C2
JTAG_T29_TMS	JTAG_T29_TMS - @mlb_lib.MLB	17B5 17C8 83C2
LPCPLUS_GPIO	LPCPLUS_GPIO - @mlb_lib.MLB	20D7 48C3
LPCPLUS_RESET_L	LPCPLUS_RESET_L - @mlb_lib.MLB	27C1 48C5 93D3
LPC_AD<0>	LPC_AD<0> - @mlb_lib.MLB	17D5 46C8 48C5
LPC_AD<3..0>	LPC_AD<3..0> - @mlb_lib.MLB	93D3
LPC_AD<1>	LPC_AD<1> - @mlb_lib.MLB	17D5 46C8 48C5
LPC_AD<2>	LPC_AD<2> - @mlb_lib.MLB	17D5 46C8 48C3
LPC_AD<3>	LPC_AD<3> - @mlb_lib.MLB	17D5 46C8 48C3
LPC_CLK33M_LPCPLUS	LPC_CLK33M_LPCPLUS - @mlb_lib.MLB	27B1 48C3 93D3
LPC_CLK33M_LPCPLUS_R	LPC_CLK33M_LPCPLUS_R - @mlb_lib.MLB	19C6 27B4 93D3
LPC_CLK33M_SMC	LPC_CLK33M_SMC - @mlb_lib.MLB	27B1 46C8 93D3
LPC_CLK33M_SMC_R	LPC_CLK33M_SMC_R - @mlb_lib.MLB	19C6 27B4 93D3
LPC_FRAME_L	LPC_FRAME_L - @mlb_lib.MLB	17D5 46C8 48C5 93D3
LPC_FRAME_R_L	LPC_FRAME_R_L - @mlb_lib.MLB	17D6 93D3
LPC_PWRDWN_L	LPC_PWRDWN_L - @mlb_lib.MLB	18C5 46C5 48C3
LPC_R_AD<0>	LPC_R_AD<0> - @mlb_lib.MLB	17D6
LPC_R_AD<3..0>	LPC_R_AD<3..0> - @mlb_lib.MLB	93D3
LPC_R_AD<1>	LPC_R_AD<1> - @mlb_lib.MLB	17D6
LPC_R_AD<2>	LPC_R_AD<2> - @mlb_lib.MLB	17D6
LPC_R_AD<3>	LPC_R_AD<3> - @mlb_lib.MLB	17D6
LPC_SERIRQ	LPC_SERIRQ - @mlb_lib.MLB	17D5 46C8 48C3
MAX8840_BP	MAX8840_BP - @mlb_lib.MLB	53A5
MEMRESET_ISOL_LS5V_L	MEMRESET_ISOL_LS5V_L - @mlb_lib.MLB	28B7
MEMVTT_EN	MEMVTT_EN - @mlb_lib.MLB	28A4 28C5 66C8
MEMVTT_EN_L	MEMVTT_EN_L - @mlb_lib.MLB	28B6
MEM_A_A<0>	MEM_A_A<0> - @mlb_lib.MLB	12C5 30C5
MEM_A_A<15..0>	MEM_A_A<15..0> - @mlb_lib.MLB	91D3
MEM_A_A<1>	MEM_A_A<1> - @mlb_lib.MLB	12C5 30C7
MEM_A_A<2>	MEM_A_A<2> - @mlb_lib.MLB	12C5 30C5
MEM_A_A<3>	MEM_A_A<3> - @mlb_lib.MLB	12C5 30C7
MEM_A_A<4>	MEM_A_A<4> - @mlb_lib.MLB	12C5 30C5
MEM_A_A<5>	MEM_A_A<5> - @mlb_lib.MLB	12C5 30C7
MEM_A_A<6>	MEM_A_A<6> - @mlb_lib.MLB	12C5 30C5
MEM_A_A<7>	MEM_A_A<7> - @mlb_lib.MLB	12C5 30C5
MEM_A_A<8>	MEM_A_A<8> - @mlb_lib.MLB	12C5 30C7
MEM_A_A<9>	MEM_A_A<9> - @mlb_lib.MLB	12C5 30C7
MEM_A_A<10>	MEM_A_A<10> - @mlb_lib.MLB	12C5 30B7
MEM_A_A<11>	MEM_A_A<11> - @mlb_lib.MLB	12B5 30C5
MEM_A_A<12>	MEM_A_A<12> - @mlb_lib.MLB	12B5 30C7
MEM_A_A<13>	MEM_A

MEM_B_DQ<9>	MEM_B_DQ<9> - @mlb_lib.MLB	12D4 29D5
MEM_B_DQ<10>	MEM_B_DQ<10> - @mlb_lib.MLB	12D4 29D5
MEM_B_DQ<11>	MEM_B_DQ<11> - @mlb_lib.MLB	12D4 29D5
MEM_B_DQ<12>	MEM_B_DQ<12> - @mlb_lib.MLB	12D4 29D5
MEM_B_DQ<13>	MEM_B_DQ<13> - @mlb_lib.MLB	12D4 29D5
MEM_B_DQ<14>	MEM_B_DQ<14> - @mlb_lib.MLB	12D4 29D5
MEM_B_DQ<15>	MEM_B_DQ<15> - @mlb_lib.MLB	12D4 29D5
MEM_B_DQ<16>	MEM_B_DQ<16> - @mlb_lib.MLB	12D4 29C5
MEM_B_DQ<23..16>	MEM_B_DQ<23..16> - @mlb_lib.MLB	91B3
MEM_B_DQ<17>	MEM_B_DQ<17> - @mlb_lib.MLB	12D4 29C5
MEM_B_DQ<18>	MEM_B_DQ<18> - @mlb_lib.MLB	12C4 29C5
MEM_B_DQ<19>	MEM_B_DQ<19> - @mlb_lib.MLB	12C4 29C5
MEM_B_DQ<20>	MEM_B_DQ<20> - @mlb_lib.MLB	12C4 29C5
MEM_B_DQ<21>	MEM_B_DQ<21> - @mlb_lib.MLB	12C4 29C5
MEM_B_DQ<22>	MEM_B_DQ<22> - @mlb_lib.MLB	12C4 29C5
MEM_B_DQ<23>	MEM_B_DQ<23> - @mlb_lib.MLB	12C4 29C5
MEM_B_DQ<24>	MEM_B_DQ<24> - @mlb_lib.MLB	12C4 29C5
MEM_B_DQ<31..24>	MEM_B_DQ<31..24> - @mlb_lib.MLB	91B3
MEM_B_DQ<25>	MEM_B_DQ<25> - @mlb_lib.MLB	12C4 29C5
MEM_B_DQ<26>	MEM_B_DQ<26> - @mlb_lib.MLB	12C4 29C5
MEM_B_DQ<27>	MEM_B_DQ<27> - @mlb_lib.MLB	12C4 29C5
MEM_B_DQ<28>	MEM_B_DQ<28> - @mlb_lib.MLB	12C4 29C5
MEM_B_DQ<29>	MEM_B_DQ<29> - @mlb_lib.MLB	12C4 29C5
MEM_B_DQ<30>	MEM_B_DQ<30> - @mlb_lib.MLB	12C4 29C5
MEM_B_DQ<31>	MEM_B_DQ<31> - @mlb_lib.MLB	12C4 29C5
MEM_B_DQ<32>	MEM_B_DQ<32> - @mlb_lib.MLB	12C4 29B5
MEM_B_DQ<39..32>	MEM_B_DQ<39..32> - @mlb_lib.MLB	91B3
MEM_B_DQ<33>	MEM_B_DQ<33> - @mlb_lib.MLB	12C4 29B5
MEM_B_DQ<34>	MEM_B_DQ<34> - @mlb_lib.MLB	12C4 29B5
MEM_B_DQ<35>	MEM_B_DQ<35> - @mlb_lib.MLB	12C4 29B5
MEM_B_DQ<36>	MEM_B_DQ<36> - @mlb_lib.MLB	12C4 29B5
MEM_B_DQ<37>	MEM_B_DQ<37> - @mlb_lib.MLB	12C4 29B5
MEM_B_DQ<38>	MEM_B_DQ<38> - @mlb_lib.MLB	12C4 29B5
MEM_B_DQ<39>	MEM_B_DQ<39> - @mlb_lib.MLB	12C4 29B5
MEM_B_DQ<40>	MEM_B_DQ<40> - @mlb_lib.MLB	12C4 29B5
MEM_B_DQ<47..40>	MEM_B_DQ<47..40> - @mlb_lib.MLB	91B3
MEM_B_DQ<41>	MEM_B_DQ<41> - @mlb_lib.MLB	12C4 29B5
MEM_B_DQ<42>	MEM_B_DQ<42> - @mlb_lib.MLB	12C4 29B5
MEM_B_DQ<43>	MEM_B_DQ<43> - @mlb_lib.MLB	12C4 29B5
MEM_B_DQ<44>	MEM_B_DQ<44> - @mlb_lib.MLB	12B4 29B5
MEM_B_DQ<45>	MEM_B_DQ<45> - @mlb_lib.MLB	12B4 29B5
MEM_B_DQ<46>	MEM_B_DQ<46> - @mlb_lib.MLB	12B4 29B5
MEM_B_DQ<47>	MEM_B_DQ<47> - @mlb_lib.MLB	12B4 29B5
MEM_B_DQ<48>	MEM_B_DQ<48> - @mlb_lib.MLB	12B4 29A5
MEM_B_DQ<55..48>	MEM_B_DQ<55..48> - @mlb_lib.MLB	91B3
MEM_B_DQ<49>	MEM_B_DQ<49> - @mlb_lib.MLB	12B4 29A5
MEM_B_DQ<50>	MEM_B_DQ<50> - @mlb_lib.MLB	12B4 29A5
MEM_B_DQ<51>	MEM_B_DQ<51> - @mlb_lib.MLB	12B4 29A5
MEM_B_DQ<52>	MEM_B_DQ<52> - @mlb_lib.MLB	12B4 29A5
MEM_B_DQ<53>	MEM_B_DQ<53> - @mlb_lib.MLB	12B4 29A5
MEM_B_DQ<54>	MEM_B_DQ<54> - @mlb_lib.MLB	12B4 29A5
MEM_B_DQ<55>	MEM_B_DQ<55> - @mlb_lib.MLB	12B4 29A5
MEM_B_DQ<56>	MEM_B_DQ<56> - @mlb_lib.MLB	12B4 29A5
MEM_B_DQ<63..56>	MEM_B_DQ<63..56> - @mlb_lib.MLB	91B3
MEM_B_DQ<57>	MEM_B_DQ<57> - @mlb_lib.MLB	12B4 29A5
MEM_B_DQ<58>	MEM_B_DQ<58> - @mlb_lib.MLB	12B4 29A5
MEM_B_DQ<59>	MEM_B_DQ<59> - @mlb_lib.MLB	12B4 29A5
MEM_B_DQ<60>	MEM_B_DQ<60> - @mlb_lib.MLB	12B4 29A5
MEM_B_DQ<61>	MEM_B_DQ<61> - @mlb_lib.MLB	12B4 29A5
MEM_B_DQ<62>	MEM_B_DQ<62> - @mlb_lib.MLB	12B4 29A5
MEM_B_DQ<63>	MEM_B_DQ<63> - @mlb_lib.MLB	12B4 29A5
MEM_B_DQS_N<0>	MEM_B_DQS_N<0> - @mlb_lib.MLB	12D2 29D5 91B3
MEM_B_DQS_N<1>	MEM_B_DQS_N<1> - @mlb_lib.MLB	12D2 29D5 91B3
MEM_B_DQS_N<2>	MEM_B_DQS_N<2> - @mlb_lib.MLB	12D2 29C5 91B3
MEM_B_DQS_N<3>	MEM_B_DQS_N<3> - @mlb_lib.MLB	12C2 29C5 91B3
MEM_B_DQS_N<4>	MEM_B_DQS_N<4> - @mlb_lib.MLB	12C2 29B5 91A3
MEM_B_DQS_N<5>	MEM_B_DQS_N<5> - @mlb_lib.MLB	12C2 29B5 91A3
MEM_B_DQS_N<6>	MEM_B_DQS_N<6> - @mlb_lib.MLB	12C2 29A5 91A3
MEM_B_DQS_N<7>	MEM_B_DQS_N<7> - @mlb_lib.MLB	12C2 29A5 91A3
MEM_B_DQS_P<0>	MEM_B_DQS_P<0> - @mlb_lib.MLB	12C2 29D5 91B3
MEM_B_DQS_P<1>	MEM_B_DQS_P<1> - @mlb_lib.MLB	12C2 29D5 91B3
MEM_B_DQS_P<2>	MEM_B_DQS_P<2> - @mlb_lib.MLB	12C2 29C5 91B3
MEM_B_DQS_P<3>	MEM_B_DQS_P<3> - @mlb_lib.MLB	12C2 29C5 91B3
MEM_B_DQS_P<4>	MEM_B_DQS_P<4> - @mlb_lib.MLB	12C2 29B5 91B3
MEM_B_DQS_P<5>	MEM_B_DQS_P<5> - @mlb_lib.MLB	12C2 29B5 91A3
MEM_B_DQS_P<6>	MEM_B_DQS_P<6> - @mlb_lib.MLB	12C2 29A5 91A3
MEM_B_DQS_P<7>	MEM_B_DQS_P<7> - @mlb_lib.MLB	12C2 29A5 91A3
MEM_B_ODT<0>	MEM_B_ODT<0> - @mlb_lib.MLB	12D2 31B5
MEM_B_ODT<3..0>	MEM_B_ODT<3..0> - @mlb_lib.MLB	91B3
MEM_B_ODT<1>	MEM_B_ODT<1> - @mlb_lib.MLB	12D2 31B5
MEM_B_RAS_L	MEM_B_RAS_L - @mlb_lib.MLB	12B4 31B5 91B3
MEM_B_SA<0>	MEM_B_SA<0> - @mlb_lib.MLB	31A7 31B3
MEM_B_SA<1>	MEM_B_SA<1> - @mlb_lib.MLB	31A7 31B3
MEM_B_WE_L	MEM_B_WE_L - @mlb_lib.MLB	12A4 31B7 91B3
MEM_EVENT_L	MEM_EVENT_L - @mlb_lib.MLB	30A5 31A5 46B8
MEM_RESET_L	MEM_RESET_L - @mlb_lib.MLB	28A5 30D5 31D5
MUX_PSU_TEMP_I1V05PC	MUX_PSU_TEMP_I1V05PCH -	46C5 47A3
H	@mlb_lib.MLB	
MUX_PSU_TEMP_I1V05PC	MUX_PSU_TEMP_I1V05PCH_SR -	47A4
H_SR	@mlb_lib.MLB	
NC_AUD_GPIO_0	NC_AUD_GPIO_0 - @mlb_lib.MLB	53D7 100D3
NC_AUD_GPIO_2	NC_AUD_GPIO_2 - @mlb_lib.MLB	53D7 100D2
NC_AUD_HP_PORT_L	NC_AUD_HP_PORT_L - @mlb_lib.MLB	53D2 100D1
NC_AUD_HP_PORT_R	NC_AUD_HP_PORT_R - @mlb_lib.MLB	53D2 100D3
NC_AUD_LO3_N_R	NC_AUD_LO3_N_R - @mlb_lib.MLB	53C2 100D2
NC_AUD_LO3_P_R	NC_AUD_LO3_P_R - @mlb_lib.MLB	53C2 100D1
NC_AUD_MIC_INN_R	NC_AUD_MIC_INN_R - @mlb_lib.MLB	53C2 100D3
NC_AUD_MIC_INP_R	NC_AUD_MIC_INP_R - @mlb_lib.MLB	53C2 100D2
NC_BCM57765_CE_L_MS_	NC_BCM57765_CE_L_MS_INS_L -	37B3 100D1
INS_L	@mlb_lib.MLB	
NC_CLINK_CLK	NC_CLINK_CLK - @mlb_lib.MLB	17B1 100D3
NC_CLINK_DATA	NC_CLINK_DATA - @mlb_lib.MLB	17B1 100D2
NC_CLINK_RESET_L	NC_CLINK_RESET_L - @mlb_lib.MLB	17B1 100D1
NC_CPU_AXG_SENSEN	NC_CPU_AXG_SENSEN - @mlb_lib.MLB	100B3
NC_CPU_AXG_SENSEP	NC_CPU_AXG_SENSEP - @mlb_lib.MLB	100B2
NC_CPU_AXG_VALSENSEN	NC_CPU_AXG_VALSENSEN - @mlb_lib.MLB	100B2
NC_CPU_AXG_VALSENSEP	NC_CPU_AXG_VALSENSEP - @mlb_lib.MLB	100B3
NC_CRT_IG_BLUE	NC_CRT_IG_BLUE - @mlb_lib.MLB	18C4 100D3
NC_CRT_IG_DDC_CLK	NC_CRT_IG_DDC_CLK - @mlb_lib.MLB	18B4 100D2
NC_CRT_IG_DDC_DATA	NC_CRT_IG_DDC_DATA - @mlb_lib.MLB	18B4 100D1
NC_CRT_IG_GREEN	NC_CRT_IG_GREEN - @mlb_lib.MLB	18C4 100D3
NC_CRT_IG_HSYNC	NC_CRT_IG_HSYNC - @mlb_lib.MLB	18B4 100D2
NC_CRT_IG_RED	NC_CRT_IG_RED - @mlb_lib.MLB	18B4 100D1
NC_CRT_IG_VSYNC	NC_CRT_IG_VSYNC - @mlb_lib.MLB	18B4 100D3
NC_CS4206_FP	NC_CS4206_FP - @mlb_lib.MLB	53D5 100D2
NC_CS4206_MICBIAS	NC_CS4206_MICBIAS - @mlb_lib.MLB	53C2 100D1
NC_DP_OC	NC_DP_OC - @mlb_lib.MLB	100D3
NC_DP_T29SNK1_AUXCHN	NC_DP_T29SNK1_AUXCHN - @mlb_lib.MLB	100A1
NC_DP_T29SNK1_AUXCHP	NC_DP_T29SNK1_AUXCHP - @mlb_lib.MLB	100A1
NC_DP_T29SNK1_MLN<3.	NC_DP_T29SNK1_MLN<3..0> -	100A1
.0>	@mlb_lib.MLB	
NC_DP_T29SNK1_MLP<3.	NC_DP_T29SNK1_MLP<3..0> -	100A1
.0>	@mlb_lib.MLB	
NC_DP_T29SRC_AUXCH_C	NC_DP_T29SRC_AUXCH_CN -	83B3 100A1
N	@mlb_lib.MLB	
NC_DP_T29SRC_AUXCH_C	NC_DP_T29SRC_AUXCH_CP -	83B3 100A1
P	@mlb_lib.MLB	
NC_DP_T29SRC_ML_CN<0	NC_DP_T29SRC_ML_CN<0> -	83B3
>	@mlb_lib.MLB	
NC_DP_T29SRC_ML_CN<3	NC_DP_T29SRC_ML_CN<3..0> -	100A1
..0>	@mlb_lib.MLB	
NC_DP_T29SRC_ML_CN<1	NC_DP_T29SRC_ML_CN<1> -	83B3
>	@mlb_lib.MLB	
NC_DP_T29SRC_ML_CN<2	NC_DP_T29SRC_ML_CN<2> -	83B3
>	@mlb_lib.MLB	
NC_DP_T29SRC_ML_CN<3	NC_DP_T29SRC_ML_CN<3> -	83B3
>	@mlb_lib.MLB	
NC_DP_T29SRC_ML_CP<0	NC_DP_T29SRC_ML_CP<0> -	83B3
>	@mlb_lib.MLB	
NC_DP_T29SRC_ML_CP<3	NC_DP_T29SRC_ML_CP<3..0> -	100A1
..0>	@mlb_lib.MLB	
NC_DP_T29SRC_ML_CP<1	NC_DP_T29SRC_ML_CP<1> -	83B3
>	@mlb_lib.MLB	
NC_DP_T29SRC_ML_CP<2	NC_DP_T29SRC_ML_CP<2> -	83B3
>	@mlb_lib.MLB	
NC_DP_T29SRC_ML_CP<3	NC_DP_T29SRC_ML_CP<3> -	83B3
>	@mlb_lib.MLB	
NC_EDP_AUXN	NC_EDP_AUXN - @mlb_lib.MLB	10B7 100D2
NC_EDP_AUXP	NC_EDP_AUXP - @mlb_lib.MLB	10B7 100D1
NC_EDP_HPD	NC_EDP_HPD - @mlb_lib.MLB	10B7 100A2
NC_EDP_TXN<0>	NC_EDP_TXN<0> - @mlb_lib.MLB	10B7
NC_EDP_TXN<3..0>	NC_EDP_TXN<3..0> - @mlb_lib.MLB	100D3
NC_EDP_TXN<1>	NC_EDP_TXN<1> - @mlb_lib.MLB	10B7
NC_EDP_TXN<2>	NC_EDP_TXN<2> - @mlb_lib.MLB	10B7
NC_EDP_TXN<3>	NC_EDP_TXN<3> - @mlb_lib.MLB	10B7
NC_EDP_TXP<0>	NC_EDP_TXP<0> - @mlb_lib.MLB	10B7
NC_EDP_TXP<3..0>	NC_EDP_TXP<3..0> - @mlb_lib.MLB	100D2
NC_EDP_TXP<1>	NC_EDP_TXP<1> - @mlb_lib.MLB	10B7
NC_EDP_TXP<2>	NC_EDP_TXP<2> - @mlb_lib.MLB	10B7
NC_EDP_TXP<3>	NC_EDP_TXP<3> - @mlb_lib.MLB	10B7
NC_EG_DP_T29SNK0_AUX	NC_EG_DP_T29SNK0_AUXCH_CN -	100B2
CH_CN	@mlb_lib.MLB	
NC_EG_DP_T29SNK0_AUX	NC_EG_DP_T29SNK0_AUXCH_CP -	100B3
CH_CP	@mlb_lib.MLB	
NC_EG_DP_T29SNK0_ML_	NC_EG_DP_T29SNK0_ML_CN<3..0> -	100B2
CN<3..0>	@mlb_lib.MLB	
NC_EG_DP_T29SNK0_ML_	NC_EG_DP_T29SNK0_ML_CP<3..0> -	100B3
CP<3..0>	@mlb_lib.MLB	
NC_FB_A0_A<0>	NC_FB_A0_A<0> - @mlb_lib.MLB	75D5
NC_FB_A0_A<8..0>	NC_FB_A0_A<8..0> - @mlb_lib.MLB	100B2
NC_FB_A0_A<1>	NC_FB_A0_A<1> - @mlb_lib.MLB	75D5
NC_FB_A0_A<2>	NC_FB_A0_A<2> - @mlb_lib.MLB	75D5
NC_FB_A0_A<3>	NC_FB_A0_A<3> - @mlb_lib.MLB	75D5
NC_FB_A0_A<4>	NC_FB_A0_A<4> - @mlb_lib.MLB	75D5
NC_FB_A0_A<5>	NC_FB_A0_A<5> - @mlb_lib.MLB	75D5
NC_FB_A0_A<6>	NC_FB_A0_A<6> - @mlb_lib.MLB	75D5
NC_FB_A0_A<7>	NC_FB_A0_A<7> - @mlb_lib.MLB	75D5
NC_FB_A0_A<8>	NC_FB_A0_A<8> - @mlb_lib.MLB	75B5
NC_FB_A0_ABI_L	NC_FB_A0_ABI_L - @mlb_lib.MLB	75C5 100B3
NC_FB_A0_CAS_L	NC_FB_A0_CAS_L - @mlb_lib.MLB	75B5 100B2
NC_FB_A0_CKE_L	NC_FB_A0_CKE_L - @mlb_lib.MLB	75B5 100B3
NC_FB_A0_CLKN	NC_FB_A0_CLKN - @mlb_lib.MLB	75C5 100B2
NC_FB_A0_CLKP	NC_FB_A0_CLKP - @mlb_lib.MLB	75C5 100B3
NC_FB_A0_CS_L	NC_FB_A0_CS_L - @mlb_lib.MLB	75B5 100B2
NC_FB_A0_DBI_L<0>	NC_FB_A0_DBI_L<0> - @mlb_lib.MLB	75C5
NC_FB_A0_DBI_L<3..0>	NC_FB_A0_DBI_L<3..0> - @mlb_lib.MLB	100B3
NC_FB_A0_DBI_L<1>	NC_FB_A0_DBI_L<1> - @mlb_lib.MLB	75C5
NC_FB_A0_DBI_L<2>	NC_FB_A0_DBI_L<2> - @mlb_lib.MLB	75C5
NC_FB_A0_DBI_L<3>	NC_FB_A0_DBI_L<3> - @mlb_lib.MLB	75C5
NC_FB_A0_DQ<0>	NC_FB_A0_DQ<0> - @mlb_lib.MLB	75D8
NC_FB_A0_DQ<31..0>	NC_FB_A0_DQ<31..0> - @mlb_lib.MLB	100A2
NC_FB_A0_DQ<1>	NC_FB_A0_DQ<1> - @mlb_lib.MLB	75D8
NC_FB_A0_DQ<2>	NC_FB_A0_DQ<2> - @mlb_lib.MLB	75D8
NC_FB_A0_DQ<3>	NC_FB_A0_DQ<3> - @mlb_lib.MLB	75D8
NC_FB_A0_DQ<4>	NC_FB_A0_DQ<4> - @mlb_lib.MLB	75D8
NC_FB_A0_DQ<5>	NC_FB_A0_DQ<5> - @mlb_lib.MLB	75D8
NC_FB_A0_DQ<6>	NC_FB_A0_DQ<6> - @mlb_lib.MLB	75D8
NC_FB_A0_DQ<7>	NC_FB_A0_DQ<7> - @mlb_lib.MLB	75D8
NC_FB_A0_DQ<8>	NC_FB_A0_DQ<8> - @mlb_lib.MLB	75D8
NC_FB_A0_DQ<9>	NC_FB_A0_DQ<9> - @mlb_lib.MLB	75D8
NC_FB_A0_DQ<10>	NC_FB_A0_DQ<10> - @mlb_lib.MLB	75D8
NC_FB_A0_DQ<11>	NC_FB_A0_DQ<11> - @mlb_lib.MLB	75D8
NC_FB_A0_DQ<12>	NC_FB_A0_DQ<12> - @mlb_lib.MLB	75D8
NC_FB_A0_DQ<13>	NC_FB_A0_DQ<13> - @mlb_lib.MLB	75D8
NC_FB_A0_DQ<14>	NC_FB_A0_DQ<14> - @mlb_lib.MLB	75D8
NC_FB_A0_DQ<15>	NC_FB_A0_DQ<15> - @mlb_lib.MLB	75D8
NC_FB_A0_DQ<16>	NC_FB_A0_DQ<16> - @mlb_lib.MLB	75D8
NC_FB_A0_DQ<17>	NC_FB_A0_DQ<17> - @mlb_lib.MLB	75D8
NC_FB_A0_DQ<18>	NC_FB_A0_DQ<18> - @mlb_lib.MLB	75D8
NC_FB_A0_DQ<19>	NC_FB_A0_DQ<19> - @mlb_lib.MLB	75D8
NC_FB_A0_DQ<20>	NC_FB_A0_DQ<20> - @mlb_lib.MLB	75D8
NC_FB_A0_DQ<21>	NC_FB_A0_DQ<21> - @mlb_lib.MLB	75D8
NC_FB_A0_DQ<22>	NC_FB_A0_DQ<22> - @mlb_lib.MLB	75D8
NC_FB_A0_DQ<23>	NC_FB_A0_DQ<23> - @mlb_lib.MLB	75D8
NC_FB_A0_DQ<24>	NC_FB_A0_DQ<24> - @mlb_lib.MLB	75C8
NC_FB_A0_DQ<25>	NC_FB_A0_DQ<25> - @mlb_lib.MLB	75C8
NC_FB_A0_DQ<26>	NC_FB_A0_DQ<26> - @mlb_lib.MLB	75C8
NC_FB_A0_DQ<27>	NC_FB_A0_DQ<27> - @mlb_lib.MLB	75C8
NC_FB_A0_DQ<28>	NC_FB_A0_DQ<28> - @mlb_lib.MLB	75C8
NC_FB_A0_DQ<29>	NC_FB_A0_DQ<29> - @mlb_lib.MLB	75C8
NC_FB_A0_DQ<30>	NC_FB_A0_DQ<30> - @mlb_lib.MLB	75C8
NC_FB_A0_DQ<31>	NC_FB_A0_DQ<31> - @mlb_lib.MLB	75C8
NC_FB_A0_EDC<0>	NC_FB_A0_EDC<0> - @mlb_lib.MLB	75C5
NC_FB_A0_EDC<3..0>	NC_FB_A0_EDC<3..0> - @mlb_lib.MLB	100A3
NC_FB_A0_EDC<1>	NC_FB_A0_EDC<1> - @mlb_lib.MLB	75C5
NC_FB_A0_EDC<2>	NC_FB_A0_EDC<2> - @mlb_lib.MLB	75C5
NC_FB_A0_EDC<3>	NC_FB_A0_EDC<3> - @mlb_lib.MLB	75C5
NC_FB_A0_RAS_L	NC_FB_A0_RAS_L - @mlb_lib.MLB	75B5 100A2
NC_FB_A0_WCLKN<0>	NC_FB_A0_WCLKN<0> - @mlb_lib.MLB	75D5
NC_FB_A0_WCLKN<1..0>	NC_FB_A0_WCLKN<1..0> - @mlb_lib.MLB	100A3
NC_FB_A0_WCLKN<1>	NC_FB_A0_WCLKN<1> - @mlb_lib.MLB	75D5
NC_FB_A0_WCLKP<0>	NC_FB_A0_WCLKP<0> - @mlb_lib.MLB	75D5
NC_FB_A0_WCLKP<1..0>	NC_FB_A0_WCLKP<1..0> - @mlb_lib.MLB	100A2
NC_FB_A0_WCLKP<1>	NC_FB_A0_WCLKP<1> - @mlb_lib.MLB	75D5
NC_FB_A0_WE_L	NC_FB_A0_WE_L - @mlb_lib.MLB	75B5 100A3
NC_FB_A1_A<0>	NC_FB_A1_A<0> - @mlb_lib.MLB	75D5
NC_FB_A1_A<8..0>	NC_FB_A1_A<8..0> - @mlb_lib.MLB	100A2
NC_FB_A1_A<1>	NC_FB_A1_A<1> - @mlb_lib.MLB	75D5
NC_FB_A1_A<2>	NC_FB_A1_A<2> - @mlb_lib.MLB	75D5
NC_FB_A1_A<3>	NC_FB_A1_A<3> - @mlb_lib.MLB	75D5
NC_FB_A1_A<4>	NC_FB_A1_A<4> - @mlb_lib.MLB	75D5
NC_FB_A1_A<5>	NC_FB_A1_A<5> - @mlb_lib.MLB	75D5
NC_FB_A1_A<6>	NC_FB_A1_A<6> - @mlb_lib.MLB	75D5
NC_FB_A1_A<7>	NC_FB_A1_A<7> - @mlb_lib.MLB	75D5
NC_FB_A1_A<8>	NC_FB_A1_A<8> - @mlb_lib.MLB	75B5
NC_FB_A1_ABI_L	NC_FB_A1_ABI_L - @mlb_lib.MLB	75C5 100A3
NC_FB_A1_CAS_L	NC_FB_A1_CAS_L - @mlb_lib.MLB	75B5 100A2
NC_FB_A1_CKE_L	NC_FB_A1_CKE_L - @mlb_lib.MLB	75B5 100A3
NC_FB_A1_CLKN	NC_FB_A1_CLKN - @mlb_lib.MLB	75B5 100A2
NC_FB_A1_CLKP	NC_FB_A1_CLKP - @mlb_lib.MLB	75C5 100A3
NC_FB_A1_CS_L	NC_FB_A1_CS_L - @mlb_lib.MLB	75B5 100A2
NC_FB_A1_DBI_L<0>	NC_FB_A1_DBI_L<0> - @mlb_lib.MLB	75C5
NC_FB_A1_DBI_L<3..0>	NC_FB_A1_DBI_L<3..0> - @mlb_lib.MLB	100A3
NC_FB_A1_DBI_L<1>	NC_FB_A1_DBI_L<1> - @mlb_lib.MLB	75C5
NC_FB_A1_DBI_L<2>	NC_FB_A1_DBI_L<2> - @mlb_lib.MLB	75C5
NC_FB_A1_DBI_L<3>	NC_FB_A1_DBI_L<3> - @mlb_lib.MLB	75C5
NC_FB_A1_DQ<0>	NC_FB_A1_DQ<0> - @mlb_lib.MLB	75C8
NC_FB_A1_DQ<31..0>	NC_FB_A1_DQ<31..0> - @mlb_lib.MLB	100A2
NC_FB_A1_DQ<1>	NC_FB_A1_DQ<1> - @mlb_lib.MLB	75C8
NC_FB_A1_DQ<2>	NC_FB_A1_DQ<2> - @mlb_lib.MLB	75C8
NC_FB_A1_DQ<3>	NC_FB_A1_DQ<3> - @mlb_lib.MLB	75C8
NC_FB_A1_DQ<4>	NC_FB_A1_DQ<4> - @mlb_lib.MLB	75C8
NC_FB_A1_DQ<5>	NC_FB_A1_DQ<5> - @mlb_lib.MLB	75C8
NC_FB_A1_DQ<6>	NC_FB_A1_DQ<6> - @mlb_lib.MLB	75C8
NC_FB_A1_DQ<7>	NC_FB_A1_DQ<7> - @mlb_lib.MLB	75C8
NC_FB_A1_DQ<8>	NC_FB_A1_DQ<8> - @mlb_lib.MLB	75C8
NC_FB_A1_DQ<9>	NC_FB_A1_DQ<9> - @mlb_lib.MLB	75C8
NC_FB_A1_DQ<10>	NC_FB_A1_DQ<10> - @mlb_lib.MLB	75C8
NC_FB_A1_DQ<11>	NC_FB_A1_DQ<11> - @mlb_lib.MLB	75C8
NC_FB_A1_DQ<12>	NC_FB_A1_DQ<12> - @mlb_lib.MLB	75C8
NC_FB_A1_DQ<13>	NC_FB_A1_DQ<13> - @mlb_lib.MLB	75C8
NC_FB_A1_DQ<14>	NC_FB_A1_DQ<14> - @mlb_lib.MLB	75C8
NC_FB_A1_DQ<15>	NC_FB_A1_DQ<15> - @mlb_lib.MLB	75C8
NC_FB_A1_DQ<16>	NC_FB_A1_DQ<16> - @mlb_lib.MLB	75C8
NC_FB_A1_DQ<17>	NC_FB_A1_DQ<17> - @mlb_lib.MLB	75C8
NC_FB_A1_DQ<18>	NC_FB_A1_DQ<18> - @mlb_lib.MLB	75B8
NC_FB_A1_DQ<19>	NC_FB_A1_DQ<19> - @mlb_lib.MLB	75B8
NC_FB_A1_DQ<20>	NC_FB_A1_DQ<20> - @mlb_lib.MLB	75B8
NC_FB_A1_DQ<21>	NC_FB_A1_DQ<21> - @mlb_lib.MLB	75B8
NC_FB_A1_DQ<22>	NC_FB_A1_DQ<22> - @mlb_lib.MLB	75B8
NC_FB_A1_DQ<23>	NC_FB_A1_DQ<23> - @mlb_lib.MLB	75B8
NC_FB_A1_DQ<24>	NC_FB_A1_DQ<24> - @mlb_lib.MLB	75B8
NC_FB_A1_DQ<25>	NC_FB_A1_DQ<25> - @mlb_lib.MLB	75B8
NC_FB_A1_DQ<26>	NC_FB_A1_DQ<26> - @mlb_lib.MLB	75B8
NC_FB_A1_DQ<27>	NC_FB_A1_DQ<27> - @mlb_lib.MLB	75B8
NC_FB_A1_DQ<28>	NC_FB_A1_DQ<28> - @mlb_lib.MLB	75B8
NC_FB_A1_DQ<29>	NC_FB_A1_DQ<29> - @mlb_lib.MLB	75B8
NC_FB_A1_DQ<30>	NC_FB_A1_DQ<30> - @mlb_lib.MLB	75B8
NC_FB_A1_DQ<31>	NC_FB_A1_DQ<31> - @mlb_lib.MLB	75B8
NC_FB_A1_EDC<0>	NC_FB_A1_EDC<0> - @mlb_lib.MLB	75C5
NC_FB_A1_EDC<3..0>	NC_FB_A1_EDC<3..0> - @mlb_lib.MLB	100A3
NC_FB_A1_EDC<1>	NC_FB_A1_EDC<1> - @mlb_lib.MLB	75C5
NC_FB_A1_EDC<2>	NC_FB_A1_EDC<2> - @mlb_lib.MLB	75C5
NC_FB_A1_EDC<3>	NC_FB_A1_EDC<3> - @mlb_lib.MLB	75C5
NC_FB_A1_RAS_L	NC_FB_A1_RAS_L - @mlb_lib.MLB	75B5 100A2
NC_FB_A1_WCLKN<0>	NC_FB_A1_WCLKN<0> - @mlb_lib.MLB	75D5
NC_FB_A1_WCLKN<1..0>	NC_FB_A1_WCLKN<1..0> - @mlb_lib.MLB	100A3
NC_FB_A1_WCLKN<1>	NC_FB_A1_WCLKN<1> - @mlb_lib.MLB	75C5
NC_FB_A1_WCLKP<0>	NC_FB_A1_WCLKP<0> - @mlb_lib.MLB	75D5
NC_FB_A1_WCLKP<1..0>	NC_FB_A1_WCLKP<1..0> - @mlb_lib.MLB	100A2
NC_FB_A1_WCLKP<1>	NC_FB_A1_WCLKP<1> - @mlb_lib.MLB	75C5
NC_FB_A1_WE_L	NC_FB_A1_WE_L - @mlb_lib.MLB	75B5 100A3
NC_FW_P1_TPAN	NC_FW_P1_TPAN - @mlb_lib.MLB	39A3 100D1
NC_FW_P1_TPAP	NC_FW_P1_TPAP - @mlb_lib.MLB	39A3 100D3
NC_FW_P1_TPBIAS	NC_FW_P1_TPBIAS - @mlb_lib.MLB	39A3 100D2
NC_FW_P2_TPAN	NC_FW_P2_TPAN - @mlb_lib.MLB	39A3 100D1
NC_FW_P2_TPAP	NC_FW_P2_TPAP - @mlb_lib.MLB	39A3 100D3
NC_FW_P2_TPBIAS	NC_FW_P2_TPBIAS - @mlb_lib.MLB	39A3 100D2
NC_GPIO35	NC_GPIO35 - @mlb_lib.MLB	20C6 100D1
NC_GPU_GENERICB	NC_GPU_GENERICB - @mlb_lib.MLB	79B6 100A3
NC_GPU_GENERICC	NC_GPU_GENERICC - @mlb_lib.MLB	79B6 100A3
NC_GPU_GENERICE	NC_GPU_GENERICE - @mlb_lib.MLB	100A3
NC_GPU_GENERICF	NC_GPU_GENERICF - @mlb_lib.MLB	79B6 100A3
NC_GPU_GENERICG	NC_GPU_GENERICG - @mlb_lib.MLB	79B6 100A3
NC_HDA_SDIN1	NC_HDA_SDIN1 - @mlb_lib.MLB	17C8 100D2
NC_HDA_SDIN2	NC_HDA_SDIN2 - @mlb_lib.MLB	17C8 100D1
NC_HDA_SDIN3	NC_HDA_SDIN3 - @mlb_lib.MLB	17C8 100D3
NC_HD_OC	NC_HD_OC - @mlb_lib.MLB	89D3 100D3
NC_IG_DP_T29SNK0_AUX	NC_IG_DP_T29SNK0_AUXCH_CN -	8C5 100D3
CH_CN	@mlb_lib.MLB	
	=IG_DP_T29SNK0_AUXCH_C_N -	8C8 18C1
	@mlb_l

NC_PCIE_CLK100M_PE5P	NC_PCIE_CLK100M_PE5P - @mlb_lib.MLB	17B4	100C2
NC_PCIE_CLK100M_PE6N	NC_PCIE_CLK100M_PE6N - @mlb_lib.MLB	20D3	100C1
NC_PCIE_CLK100M_PE6P	NC_PCIE_CLK100M_PE6P - @mlb_lib.MLB	20D3	100C3
NC_PCIE_CLK100M_PE7N	NC_PCIE_CLK100M_PE7N - @mlb_lib.MLB	20D3	100C2
NC_PCIE_CLK100M_PE7P	NC_PCIE_CLK100M_PE7P - @mlb_lib.MLB	20D3	100C1
NC_PCIE_CLK100M_PEBN	NC_PCIE_CLK100M_PEBN - @mlb_lib.MLB	17B4	100C3
NC_PCIE_CLK100M_PEBP	NC_PCIE_CLK100M_PEBP - @mlb_lib.MLB	17B4	100C2
NC_PCIE_CLK100M_T29N	NC_PCIE_CLK100M_T29N - @mlb_lib.MLB	100C1	
NC_PCIE_CLK100M_T29P	NC_PCIE_CLK100M_T29P - @mlb_lib.MLB	100C3	
NC_PCIE_T29_D2RN<3..	NC_PCIE_T29_D2RN<3..0> -	100C2	
0>	@mlb_lib.MLB		
NC_PCIE_T29_D2RP<3..	NC_PCIE_T29_D2RP<3..0> -	100C1	
0>	@mlb_lib.MLB		
NC_PCIE_T29_R2D_CN<3	NC_PCIE_T29_R2D_CN<3..0> -	100C3	
..0>	@mlb_lib.MLB		
NC_PCIE_T29_R2D_CP<3	NC_PCIE_T29_R2D_CP<3..0> -	100C2	
..0>	@mlb_lib.MLB		
NC_PCI_PME_L	NC_PCI_PME_L - @mlb_lib.MLB	19D6	100C2
NC_PEG_CLK100MN	NC_PEG_CLK100MN - @mlb_lib.MLB	100C1	
NC_PEG_CLK100MP	NC_PEG_CLK100MP - @mlb_lib.MLB	100C3	
NC_PEG_D2RN<7..0>	NC_PEG_D2RN<7..0> - @mlb_lib.MLB	100C2	
NC_PEG_D2RN<12>	NC_PEG_D2RN<12> - @mlb_lib.MLB	10D5	
NC_PEG_D2RN<15..12>	NC_PEG_D2RN<15..12> - @mlb_lib.MLB	100C1	
NC_PEG_D2RN<13>	NC_PEG_D2RN<13> - @mlb_lib.MLB	10D5	
NC_PEG_D2RN<14>	NC_PEG_D2RN<14> - @mlb_lib.MLB	10C5	
NC_PEG_D2RN<15>	NC_PEG_D2RN<15> - @mlb_lib.MLB	10C5	
NC_PEG_D2RP<7..0>	NC_PEG_D2RP<7..0> - @mlb_lib.MLB	100C3	
NC_PEG_D2RP<12>	NC_PEG_D2RP<12> - @mlb_lib.MLB	10C5	
NC_PEG_D2RP<15..12>	NC_PEG_D2RP<15..12> - @mlb_lib.MLB	100C2	
NC_PEG_D2RP<13>	NC_PEG_D2RP<13> - @mlb_lib.MLB	10C5	
NC_PEG_D2RP<14>	NC_PEG_D2RP<14> - @mlb_lib.MLB	10C5	
NC_PEG_D2RP<15>	NC_PEG_D2RP<15> - @mlb_lib.MLB	10C5	
NC_PEG_R2D_CN<7..0>	NC_PEG_R2D_CN<7..0> - @mlb_lib.MLB	100C1	
NC_PEG_R2D_CN<12>	NC_PEG_R2D_CN<12> - @mlb_lib.MLB	10B5	
NC_PEG_R2D_CN<15..12	NC_PEG_R2D_CN<15..12> -	100C3	
>	@mlb_lib.MLB		
NC_PEG_R2D_CN<13>	NC_PEG_R2D_CN<13> - @mlb_lib.MLB	10B5	
NC_PEG_R2D_CN<14>	NC_PEG_R2D_CN<14> - @mlb_lib.MLB	10B5	
NC_PEG_R2D_CN<15>	NC_PEG_R2D_CN<15> - @mlb_lib.MLB	10B5	
NC_PEG_R2D_CP<7..0>	NC_PEG_R2D_CP<7..0> - @mlb_lib.MLB	100C2	
NC_PEG_R2D_CP<12>	NC_PEG_R2D_CP<12> - @mlb_lib.MLB	10B5	
NC_PEG_R2D_CP<15..12	NC_PEG_R2D_CP<15..12> -	100C1	
>	@mlb_lib.MLB		
NC_PEG_R2D_CP<13>	NC_PEG_R2D_CP<13> - @mlb_lib.MLB	10B5	
NC_PEG_R2D_CP<14>	NC_PEG_R2D_CP<14> - @mlb_lib.MLB	10B5	
NC_PEG_R2D_CP<15>	NC_PEG_R2D_CP<15> - @mlb_lib.MLB	10B5	
NC_SATA_C_D2RN	NC_SATA_C_D2RN - @mlb_lib.MLB	17C5	100C3
NC_SATA_C_D2RP	NC_SATA_C_D2RP - @mlb_lib.MLB	17C5	100C2
NC_SATA_C_R2D_CN	NC_SATA_C_R2D_CN - @mlb_lib.MLB	17C5	100C1
NC_SATA_C_R2D_CP	NC_SATA_C_R2D_CP - @mlb_lib.MLB	17C5	100C3
NC_SATA_D_D2RN	NC_SATA_D_D2RN - @mlb_lib.MLB	17C5	100C2
NC_SATA_D_D2RP	NC_SATA_D_D2RP - @mlb_lib.MLB	17C5	100C1
NC_SATA_D_R2D_CN	NC_SATA_D_R2D_CN - @mlb_lib.MLB	17C5	100C3
NC_SATA_D_R2D_CP	NC_SATA_D_R2D_CP - @mlb_lib.MLB	17C5	100C2
NC_SATA_E_D2RN	NC_SATA_E_D2RN - @mlb_lib.MLB	17C5	100C1
NC_SATA_E_D2RP	NC_SATA_E_D2RP - @mlb_lib.MLB	17C5	100C3
NC_SATA_E_R2D_CN	NC_SATA_E_R2D_CN - @mlb_lib.MLB	17C5	100C2
NC_SATA_E_R2D_CP	NC_SATA_E_R2D_CP - @mlb_lib.MLB	17C5	100C1
NC_SATA_F_D2RN	NC_SATA_F_D2RN - @mlb_lib.MLB	17C5	100C3
NC_SATA_F_D2RP	NC_SATA_F_D2RP - @mlb_lib.MLB	17C5	100C2
NC_SATA_F_R2D_CN	NC_SATA_F_R2D_CN - @mlb_lib.MLB	17C5	100C1
NC_SATA_F_R2D_CP	NC_SATA_F_R2D_CP - @mlb_lib.MLB	17C5	100C3
NC_SDVO_INTN	NC_SDVO_INTN - @mlb_lib.MLB	18D1	100C2
NC_SDVO_INTP	NC_SDVO_INTP - @mlb_lib.MLB	18D1	100C1
NC_SDVO_STALLN	NC_SDVO_STALLN - @mlb_lib.MLB	18D1	100C3
NC_SDVO_STALLP	NC_SDVO_STALLP - @mlb_lib.MLB	18D1	100C2
NC_SDVO_TVCLKINN	NC_SDVO_TVCLKINN - @mlb_lib.MLB	18D1	100C1
NC_SDVO_TVCLKINP	NC_SDVO_TVCLKINP - @mlb_lib.MLB	18D1	100B3
NC_SMC_BMON_MUX_SEL	NC_SMC_BMON_MUX_SEL - @mlb_lib.MLB	100B2	
NC_SMC_FAN_1_CTL	NC_SMC_FAN_1_CTL - @mlb_lib.MLB	46A8	100B1
NC_SMC_FAN_1_TACH	NC_SMC_FAN_1_TACH - @mlb_lib.MLB	46A8	100B3
NC_SMC_FAN_2_CTL	NC_SMC_FAN_2_CTL - @mlb_lib.MLB	46A8	100B2
NC_SMC_FAN_2_TACH	NC_SMC_FAN_2_TACH - @mlb_lib.MLB	46A8	100B1
NC_SMC_FAN_3_CTL	NC_SMC_FAN_3_CTL - @mlb_lib.MLB	46A8	100B3
NC_SMC_FAN_3_TACH	NC_SMC_FAN_3_TACH - @mlb_lib.MLB	46A8	100B2
NC_SMC_P10	NC_SMC_P10 - @mlb_lib.MLB	46D8	100B1
NC_SMC_P20	NC_SMC_P20 - @mlb_lib.MLB	46C8	100B3
NC_SMC_P24	NC_SMC_P24 - @mlb_lib.MLB	46C8	100B2
NC_SMC_P41	NC_SMC_P41 - @mlb_lib.MLB	46C8	100B1
NC_SMC_P43	NC_SMC_P43 - @mlb_lib.MLB	46C8	100B3
NC_SMC_PF5	NC_SMC_PF5 - @mlb_lib.MLB	46B5	100B2
NC_SMC_RSTGATE_L	NC_SMC_RSTGATE_L - @mlb_lib.MLB	46D8	100B1
NC_SMC_SYS_KBDLED	NC_SMC_SYS_KBDLED - @mlb_lib.MLB	46C8	100B3
NC_SPI_DESCRIPTOR_OV	NC_SPI_DESCRIPTOR_OVERRIDE_L -	46B8	100B2
ERRIDE_L	@mlb_lib.MLB		
NC_T29_D2RN0	NC_T29_D2RN0 - @mlb_lib.MLB	83A5	100A1
NC_T29_D2RN1	NC_T29_D2RN1 - @mlb_lib.MLB	83A5	100A1
NC_T29_D2RP0	NC_T29_D2RP0 - @mlb_lib.MLB	83A5	100A1
NC_T29_D2RP1	NC_T29_D2RP1 - @mlb_lib.MLB	83A5	100A1
NC_T29_PCIE_RESET0_L	NC_T29_PCIE_RESET0_L - @mlb_lib.MLB	83C3	100B1
NC_T29_PCIE_RESET1_L	NC_T29_PCIE_RESET1_L - @mlb_lib.MLB	83C3	100B1
NC_T29_PCIE_RESET2_L	NC_T29_PCIE_RESET2_L - @mlb_lib.MLB	83C3	100B1
NC_T29_PCIE_RESET3_L	NC_T29_PCIE_RESET3_L - @mlb_lib.MLB	83C3	100B1
NC_T29_PWR_EN	NC_T29_PWR_EN - @mlb_lib.MLB	100B1	
NC_T29_R2D_CN0	NC_T29_R2D_CN0 - @mlb_lib.MLB	83A5	100B1
NC_T29_R2D_CN1	NC_T29_R2D_CN1 - @mlb_lib.MLB	83A5	100B1
NC_T29_R2D_CP0	NC_T29_R2D_CP0 - @mlb_lib.MLB	83A5	100B1
NC_T29_R2D_CP1	NC_T29_R2D_CP1 - @mlb_lib.MLB	83A5	100B1
NC_USB_1N	NC_USB_1N - @mlb_lib.MLB	19D4	100B3
NC_USB_1P	NC_USB_1P - @mlb_lib.MLB	19D4	100B2
NC_USB_2N	NC_USB_2N - @mlb_lib.MLB	19D4	100B1
NC_USB_2P	NC_USB_2P - @mlb_lib.MLB	19D4	100B3
NC_USB_3N	NC_USB_3N - @mlb_lib.MLB	19D4	100B2
NC_USB_3P	NC_USB_3P - @mlb_lib.MLB	19D4	100B1
NC_USB_4N	NC_USB_4N - @mlb_lib.MLB	19D4	100B3
NC_USB_4P	NC_USB_4P - @mlb_lib.MLB	19D4	100B2
NC_USB_5N	NC_USB_5N - @mlb_lib.MLB	19D4	100B1
NC_USB_5P	NC_USB_5P - @mlb_lib.MLB	19D4	100B3
NC_USB_6N	NC_USB_6N - @mlb_lib.MLB	19D4	100B2
NC_USB_6P	NC_USB_6P - @mlb_lib.MLB	19D4	100B1
NC_USB_7N	NC_USB_7N - @mlb_lib.MLB	19D4	100B3
NC_USB_7P	NC_USB_7P - @mlb_lib.MLB	19D4	100B2
NC_USB_9N	NC_USB_9N - @mlb_lib.MLB	19C4	100B1
NC_USB_9P	NC_USB_9P - @mlb_lib.MLB	19C4	100B3
NC_USB_10N	NC_USB_10N - @mlb_lib.MLB	19C4	100B2
NC_USB_10P	NC_USB_10P - @mlb_lib.MLB	19C4	100B1
NC_USB_11N	NC_USB_11N - @mlb_lib.MLB	19C4	100B3
NC_USB_11P	NC_USB_11P - @mlb_lib.MLB	19C4	100B2
NC_USB_12N	NC_USB_12N - @mlb_lib.MLB	19C4	100B1
NC_USB_12P	NC_USB_12P - @mlb_lib.MLB	19C4	100B3
NC_USB_13N	NC_USB_13N - @mlb_lib.MLB	19C4	100B2
NC_USB_13P	NC_USB_13P - @mlb_lib.MLB	19C4	100B1
ODD_PWR_EN_L	ODD_PWR_EN_L - @mlb_lib.MLB	20D6	20D8
P1V0GPU_EN	P1V0GPU_EN - @mlb_lib.MLB	76A6	76D5

P1V0GPU_PGOOD	P1V0GPU_PGOOD - @mlb_lib.MLB	76C7	76D5
P1V05_DIV_VMON	P1V05_DIV_VMON - @mlb_lib.MLB	62A7	
P1V5CPU_EN	P1V5CPU_EN - @mlb_lib.MLB	28C5	61B8
P1V5CPU_EN_L	P1V5CPU_EN_L - @mlb_lib.MLB	28C6	
P1V5FB_EN	P1V5FB_EN - @mlb_lib.MLB	76A6	76B6
P1V5FB_PGOOD	P1V5FB_PGOOD - @mlb_lib.MLB	76B6	76C7
P1V5S0FET_GATE	P1V5S0FET_GATE - @mlb_lib.MLB	61B7	
P1V5S0FET_GATE_R	P1V5S0FET_GATE_R - @mlb_lib.MLB	61B6	
P1V5S0_EN	P1V5S0_EN - @mlb_lib.MLB	62C1	71A7
P1V5S3_CS_N	P1V5S3_CS_N - @mlb_lib.MLB	50C8	66C1
P1V5S3_CS_P	P1V5S3_CS_P - @mlb_lib.MLB	50C8	66C1
P1V5S3_IOUT	P1V5S3_IOUT - @mlb_lib.MLB	50C7	
P1V5VDDQCPU_RAMP_DON	P1V5VDDQCPU_RAMP_DONE -	28C5	61B6
E	@mlb_lib.MLB		
P1V5_DIV_VMON	P1V5_DIV_VMON - @mlb_lib.MLB	62A7	
P1V5_S0_DIV	P1V5_S0_DIV - @mlb_lib.MLB	28C4	
P1V8GPU_EN	P1V8GPU_EN - @mlb_lib.MLB	76A6	77C6
P1V8GPU_PGOOD	P1V8GPU_PGOOD - @mlb_lib.MLB	76C7	77C6
P1V8S0_EN	P1V8S0_EN - @mlb_lib.MLB	62C1	71C8
P1V8S0_PGOOD	P1V8S0_PGOOD - @mlb_lib.MLB	62A6	71C8
P1V95_FW_NR	P1V95_FW_NR - @mlb_lib.MLB	40D6	
P3V3ENET_SS	P3V3ENET_SS - @mlb_lib.MLB	62B2	
P3V3S0_EN	P3V3S0_EN - @mlb_lib.MLB	61C4	62C1
	PM_SLP_S3_R_L - @mlb_lib.MLB	62C2	
	P5VS0_EN - @mlb_lib.MLB	61A4	62C1
	PM_SLP_S3_R_L - @mlb_lib.MLB	62C2	
	P5VS0_EN - @mlb_lib.MLB	61A4	62C1
P3V3S0_EN_L	P3V3S0_EN_L - @mlb_lib.MLB	61C3	
P3V3S0_SS	P3V3S0_SS - @mlb_lib.MLB	61C2	
P3V3S3_EN_RC	P3V3S3_EN_RC - @mlb_lib.MLB	25B2	
P3V3S4_EN	P3V3S4_EN - @mlb_lib.MLB	61D4	62D1
P3V3S4_EN_L	P3V3S4_EN_L - @mlb_lib.MLB	61D3	
P3V3S4_GATE	P3V3S4_GATE - @mlb_lib.MLB	61D3	
P3V3S5_EN	P3V3S5_EN - @mlb_lib.MLB	61D8	62D6
P3V3S5_EN_L	P3V3S5_EN_L - @mlb_lib.MLB	61D7	
P3V3S5_SS	P3V3S5_SS - @mlb_lib.MLB	61D6	
P3V3WLAN_SS	P3V3WLAN_SS - @mlb_lib.MLB	35C2	
P3V3WLAN_VMON	P3V3WLAN_VMON - @mlb_lib.MLB	35B4	
P5V0S0_EN_L	P5V0S0_EN_L - @mlb_lib.MLB	61B3	
P5V0S0_SS	P5V0S0_SS - @mlb_lib.MLB	61B3	
P5VS5_EN_L	P5VS5_EN_L - @mlb_lib.MLB	61B3	
P5VS5_SS	P5VS5_SS - @mlb_lib.MLB	61B2	
P5V_DIV_VMON	P5V_DIV_VMON - @mlb_lib.MLB	62A8	
P12V_S5_FW_CL	P12V_S5_FW_CL - @mlb_lib.MLB	41D5	
P12V_S5_FW_R	P12V_S5_FW_R - @mlb_lib.MLB	41D7	
P12V_T29	P12V_T29 - @mlb_lib.MLB	87D2	
P33V_S5_FW_D	P33V_S5_FW_D - @mlb_lib.MLB	41D4	
PCA9557D_RESET_L	PCA9557D_RESET_L - @mlb_lib.MLB	27C1	33B7
PCH1V05_IOUT	PCH1V05_IOUT - @mlb_lib.MLB	50C6	
PCH_A20GATE	PCH_A20GATE - @mlb_lib.MLB	20D4	
PCH_CLK14P3M_REFCLK	PCH_CLK14P3M_REFCLK - @mlb_lib.MLB	17A8	17C1 93B3
PCH_CLK25M_X1	PCH_CLK25M_X1 - @mlb_lib.MLB	17B1	26D1
PCH_CLK25M_X2	PCH_CLK25M_X2 - @mlb_lib.MLB	17B1	26D1
	TP_PCH_CLK25M_X2 - @mlb_lib.MLB	26D3	
PCH_CLK32K_RTCX1	PCH_CLK32K_RTCX1 - @mlb_lib.MLB	17D8	27C8
PCH_CLK32K_RTCX2	PCH_CLK32K_RTCX2 - @mlb_lib.MLB	17D8	27C8
PCH_CLK32K_RTCX2_R	PCH_CLK32K_RTCX2_R - @mlb_lib.MLB	27C7	
PCH_CLK33M_PCIIN	PCH_CLK33M_PCIIN - @mlb_lib.MLB	17C1	27B1 93B3
PCH_CLK33M_PCIOUT	PCH_CLK33M_PCIOUT - @mlb_lib.MLB	19C6	27B4
PCH_CLK96M_DOT_N	PCH_CLK96M_DOT_N - @mlb_lib.MLB	17A8	17C1 93B3
PCH_CLK96M_DOT_P	PCH_CLK96M_DOT_P - @mlb_lib.MLB	17A8	17C1 93B3
PCH_CLK100M_SATA_N	PCH_CLK100M_SATA_N - @mlb_lib.MLB	17A8	17C1 93B3
PCH_CLK100M_SATA_P	PCH_CLK100M_SATA_P - @mlb_lib.MLB	17A8	17C1 93B3
PCH_CLKIN_GNDN1	PCH_CLKIN_GNDN1 - @mlb_lib.MLB	17B1	
PCH_CLKIN_GNDP1	PCH_CLKIN_GNDP1 - @mlb_lib.MLB	17B1	
PCH_DAC_IREF	PCH_DAC_IREF - @mlb_lib.MLB	18B4	
PCH_DF_TVS	PCH_DF_TVS - @mlb_lib.MLB	18B6	
PCH_DMI2RBIAS	PCH_DMI2RBIAS - @mlb_lib.MLB	18C8	
PCH_DMI_COMP	PCH_DMI_COMP - @mlb_lib.MLB	18C8	
PCH_DSWVRMEN	PCH_DSWVRMEN - @mlb_lib.MLB	18B6	
PCH_GPIO0	PCH_GPIO0 - @mlb_lib.MLB	20B6	20D6
PCH_GPIO10_OC6_L	PCH_GPIO10_OC6_L - @mlb_lib.MLB	19C1	24C4
PCH_GPIO11	PCH_GPIO11 - @mlb_lib.MLB	17A3	17D1
PCH_GPIO12	PCH_GPIO12 - @mlb_lib.MLB	20C7	20D6
PCH_GPIO14_OC7_L	PCH_GPIO14_OC7_L - @mlb_lib.MLB	19C1	24C4
PCH_GPIO15	PCH_GPIO15 - @mlb_lib.MLB	20A6	20D6 24D4
PCH_GPIO24	PCH_GPIO24 - @mlb_lib.MLB	20C6	20C7
PCH_GPIO36_SATA2GP	PCH_GPIO36_SATA2GP - @mlb_lib.MLB	20A1	20C6
PCH_GPIO43_OC4_L	PCH_GPIO43_OC4_L - @mlb_lib.MLB	19C1	24C4
PCH_GPIO46	PCH_GPIO46 - @mlb_lib.MLB	20A6	20C6
PCH_GPIO52	PCH_GPIO52 - @mlb_lib.MLB	19D6	
PCH_GPIO68_TACH4	PCH_GPIO68_TACH4 - @mlb_lib.MLB	20A6	20C6
PCH_GPIO69_TACH5	PCH_GPIO69_TACH5 - @mlb_lib.MLB	20A6	20C6
PCH_GPIO70_TACH6	PCH_GPIO70_TACH6 - @mlb_lib.MLB	20A6	20C6
PCH_GPIO71_TACH7	PCH_GPIO71_TACH7 - @mlb_lib.MLB	20A6	20C6
PCH_INTRUDER_L	PCH_INTRUDER_L - @mlb_lib.MLB	17A7	17D8
PCH_INTVRMEN_L	PCH_INTVRMEN_L - @mlb_lib.MLB	17A7	17D8
PCH_PCI_GNT1_L	PCH_PCI_GNT1_L - @mlb_lib.MLB	19B8	19D6
PCH_PCI_GNT2_L	PCH_PCI_GNT2_L - @mlb_lib.MLB	19B8	19D6
PCH_PCI_GNT3_L	PCH_PCI_GNT3_L - @mlb_lib.MLB	19B8	19D6
PCH_PECI	PCH_PECI - @mlb_lib.MLB	20D4	
PCH_PROCPWRGD	PCH_PROCPWRGD - @mlb_lib.MLB	20D4	
PCH_RCIN_L	PCH_RCIN_L - @mlb_lib.MLB	20D4	
PCH_RI_L	PCH_RI_L - @mlb_lib.MLB	18C8	
PCH_SATA3COMP	PCH_SATA3COMP - @mlb_lib.MLB	17B6	92C3
PCH_SATA3RBIAS	PCH_SATA3RBIAS - @mlb_lib.MLB	17B6	
PCH_SATAICOMP	PCH_SATAICOMP - @mlb_lib.MLB	17C6	92C3
PCH_SATALED_L	PCH_SATALED_L - @mlb_lib.MLB	17B5	17C5
PCH_SPKR	PCH_SPKR - @mlb_lib.MLB	17B5	17D8
PCH_SRTCRST_L	PCH_SRTCRST_L - @mlb_lib.MLB	17A7	17D8
PCH_SUSACK_L	PCH_SUSACK_L - @mlb_lib.MLB	18B5	18B5
PCH_THRMD_N	PCH_THRMD_N - @mlb_lib.MLB	52B3	52C8
PCH_THRMD_P	PCH_THRMD_P - @mlb_lib.MLB	52C3	52C8
PCH_USB_RBIAS	PCH_USB_RBIAS - @mlb_lib.MLB	19C4	92C3
PCH_XCLK_RCOMP	PCH_XCLK_RCOMP - @mlb_lib.MLB	17B2	
PCIECLKRQ5_L_GPIO44	PCIECLKRQ5_L_GPIO44 - @mlb_lib.MLB	17A5	17B4
PCIE_AP_D2R_N	PCIE_AP_D2R_N - @mlb_lib.MLB	17D4	35D4 93D1 100D7
PCIE_AP_D2R_P	PCIE_AP_D2R_P - @mlb_lib.MLB	17D4	35D4 93D1 100D7
PCIE_AP_R2D_C_N	PCIE_AP_R2D_C_N - @mlb_lib.MLB	17D4	35C4 93D1
PCIE_AP_R2D_C_P	PCIE_AP_R2D_C_P - @mlb_lib.MLB	17D4	35C4 93D1
PCIE_AP_R2D_N	PCIE_AP_R2D_N - @mlb_lib.MLB	35C6	93D1 100D7
PCIE_AP_R2D_P	PCIE_AP_R2D_P - @mlb_lib.MLB	35C6	93D1 100D7
PCIE_CLK100M_AP_CONN	PCIE_CLK100M_AP_CONN_N -	35C6	93C1 100D7
_N	@mlb_lib.MLB		
PCIE_CLK100M_AP_CONN	PCIE_CLK100M_AP_CONN_P -	35C6	93C1 100D7
_P	@mlb_lib.MLB		
PCIE_CLK100M_AP_N	PCIE_CLK100M_AP_N - @mlb_lib.MLB	17C4	35D4 93C1
PCIE_CLK100M_AP_P	PCIE_CLK100M_AP_P - @mlb_lib.MLB	17C4	35D4 93C1
PCIE_CLK100M_ENET_N	PCIE_CLK100M_ENET_N - @mlb_lib.MLB	17C4	37B6 93C1
PCIE_CLK100M_ENET_P	PCIE_CLK100M_ENET_P - @mlb_lib.MLB	17C4	37B6 93C1
PCIE_CLK100M_FW_N	PCIE_CLK100M_FW_N - @mlb_lib.MLB	17C4	39C6 93C1
PCIE_CLK100M_FW_P	PCIE_CLK100M_FW_P - @mlb_lib.MLB	17C4	39C6 93C1
PCIE_CLK100M_PCH_N	PCIE_CLK100M_PCH_N - @mlb_lib.MLB	17A8	17C1 93C1
PCIE_CLK100M_PCH_P	PCIE_CLK100M_PCH_P - @mlb_lib.MLB	17A8	17C1 93C1

PCIE_CLK100M_T29_N	PCIE_CLK100M_T29_N - @mlb_lib.MLB	17B4	83C2 93C1
PCIE_CLK100M_T29_P	PCIE_CLK100M_T29_P - @mlb_lib.MLB	17B4	83C2 93C1
PCIE_ENET_D2R_C_N	PCIE_ENET_D2R_C_N - @mlb_lib.MLB	37C6	93D1
PCIE_ENET_D2R_C_P	PCIE_ENET_D2R_C_P - @mlb_lib.MLB	37C6	93D1
PCIE_ENET_D2R_N	PCIE_ENET_D2R_N - @mlb_lib.MLB	17D4	37C8 93D1
PCIE_ENET_D2R_P	PCIE_ENET_D2R_P - @mlb_lib.MLB	17D4	37C8 93D1
PCIE_ENET_R2D_C_N	PCIE_ENET_R2D_C_N - @mlb_lib.MLB	17D4	37B8 93D1
PCIE_ENET_R2D_C_P	PCIE_ENET_R2D_C_P - @mlb_lib.MLB	17D4	37C8 93D1
PCIE_ENET_R2D_N	PCIE_ENET_R2D_N - @mlb_lib.MLB	37C6	93D1
PCIE_ENET_R2D_P	PCIE_ENET_R2D_P - @mlb_lib.MLB	37C6	93D1
PCIE_FW_D2R_C_N	PCIE_FW_D2R_C_N - @mlb_lib.MLB	39C6	93D1
PCIE_FW_D2R_C_P	PCIE_FW_D2R_C_P - @mlb_lib.MLB	39C6	93C1
PCIE_FW_D2R_N	PCIE_FW_D2R_N - @mlb_lib.MLB	17D4	39C8 93D1
PCIE_FW_D2R_P	PCIE_FW_D2R_P - @mlb_lib.MLB	17D4	39C8 93D1
PCIE_FW_R2D_C_N	PCIE_FW_R2D_C_N - @mlb_lib.MLB	17D4	39C8 93D1
PCIE_FW_R2D_C_P	PCIE_FW_R2D_C_P - @mlb_lib.MLB	17D4	39C8 93D1
PCIE_FW_R2D_N	PCIE_FW_R2D_N - @mlb_lib.MLB	39C6	93D1
PCIE_FW_R2D_P	PCIE_FW_R2D_P - @mlb_lib.MLB	39C6	93D1
PCIE_T29_D2R_C_N<0>	PCIE_T29_D2R_C_N<0> - @mlb_lib.MLB	83D3	
PCIE_T29_D2R_C_N<3..	PCIE_T29_D2R_C_N<3..0> -	93C1	
0>	@mlb_lib.MLB		
PCIE_T29_D2R_C_N<1>	PCIE_T29_D2R_C_N<1> - @mlb_lib.MLB	83D3	
PCIE_T29_D2R_C_N<2>	PCIE_T29_D2R_C_N<2> - @mlb_lib.MLB	83D3	
PCIE_T29_D2R_C_N<3>	PCIE_T29_D2R_C_N<3> - @mlb_lib.MLB	83D3	
PCIE_T29_D2R_C_P<0>	PCIE_T29_D2R_C_P<0> - @mlb_lib.MLB	83D3	
PCIE_T29_D2R_C_P<3..	PCIE_T29_D2R_C_P<3..0> -	93C1	
0>	@mlb_lib.MLB		
PCIE_T29_D2R_C_P<1>	PCIE_T29_D2R_C_P<1> - @mlb_lib.MLB	83D3	
PCIE_T29_D2R_C_P<2>	PCIE_T29_D2R_C_P<2> - @mlb_lib.MLB	83D3	
PCIE_T29_D2R_C_P<3>	PCIE_T29_D2R_C_P<3> - @mlb_lib.MLB	83D3	
PCIE_T29_D2R_N<0>	PCIE_T29_D2R_N<0> - @mlb_lib.MLB	83D1	
	=PCIE_T29_D2R_N<3..0> -	8C8	
	@mlb_lib.MLB		
PCIE_T29_D2R_N<3..0>	PCIE_T29_D2R_N<3..0> - @mlb_lib.MLB	8C6	93C1
	=PCIE_T29_D2R_N<3..0> -	8C8	
	@mlb_lib.MLB		
PCIE_T29_D2R_N<1>	PCIE_T29_D2R_N<1> - @mlb_lib.MLB	83D1	
	=PCIE_T29_D2R_N<3..0> -	8C8	
	@mlb_lib.MLB		
PCIE_T29_D2R_N<2>	PCIE_T29_D2R_N<2> - @mlb_lib.MLB	83D1	
	=PCIE_T29_D2R_N<3..0> -	8C8	
	@mlb_lib.MLB		
PCIE_T29_D2R_N<3>	PCIE_T29_D2R_N<3> - @mlb_lib.MLB	83D1	
	=PCIE_T29_D2R_N<3..0> -	8C8	
	@mlb_lib.MLB		
PCIE_T29_D2R_P<0>	PCIE_T29_D2R_P<0> - @mlb_lib.MLB	83D1	
	=PCIE_T29_D2R_P<3..0> -	8C8	
	@mlb_lib.MLB		
PCIE_T29_D2R_P<3..0>	PCIE_T29_D2R_P<3..0> - @mlb_lib.MLB	8C6	93C1
	=PCIE_T29_D2R_P<3..0> -	8C8	
	@mlb_lib.MLB		
PCIE_T29_D2R_P<1>	PCIE_T29_D2R_P<1> - @mlb_lib.MLB	83D1	
	=PCIE_T29_D2R_P<3..0> -	8C8	
	@mlb_lib.MLB		
PCIE_T29_D2R_P<2>	PCIE_T29_D2R_P<2> - @mlb_lib.MLB	83D1	
	=PCIE_T29_D2R_P<3..0> -	8C8	
	@mlb_lib.MLB		
PCIE_T29_D2R_P<3>	PCIE_T29_D2R_P<3> - @mlb_lib.MLB	83D1	
	=PCIE_T29_D2R_P<3..0> -	8C8	
	@mlb_lib.MLB		
PCIE_T29_R2D_C_N<0>	PCIE_T29_R2D_C_N<0> - @mlb_lib.MLB	83D7	
	=PCIE_T29_R2D_C_N<3..0> -	8C8	
	@mlb_lib.MLB		
PCIE_T29_R2D_C_N<3..	PCIE_T29_R2D_C_N<3..0> -	8C6	93C1
0>	@mlb_lib.MLB		
	=PCIE_T29_R2D_C_N<3..0> -	8C8	
	@mlb_lib.MLB		
PCIE_T29_R2D_C_N<1>	PCIE_T29_R2D_C_N<1> - @mlb_lib.MLB	83D7	
	=PCIE_T29_R2D_C_N<3..0> -	8C8	
	@mlb_lib.MLB		
PCIE_T29_R2D_C_N<2>	PCIE_T29_R2D_C_N<2> - @mlb_lib.MLB	83D7	
	=PCIE_T29_R2D_C_N<3..0> -	8C8	
	@mlb_lib.MLB		
PCIE_T29_R2D_C_N<3>	PCIE_T29_R2D_C_N<3> - @mlb_lib.MLB	83D7	
	=PCIE_T29_R2D_C_N<3..0> -	8C8	
	@mlb_lib.MLB		
PCIE_T29_R2D_C_P<0>	PCIE_T29_R2D_C_P<0> - @mlb_lib.MLB	83D7	
	=PCIE_T29_R2D_C_P<3..0> -	8C8	
	@mlb_lib.MLB		
PCIE_T29_

			27A5
PM_PCH_SYS_PWROK	PM_PCH_SYS_PWROK - @mlb_lib.MLB		18C8 24C8 27A5
PM_PECI_PWRGD	PM_PECI_PWRGD - @mlb_lib.MLB		46A4 62C4
PM_PECI_PWRGD_R	PM_PECI_PWRGD_R - @mlb_lib.MLB		46A5
PM_PGOOD_P3V3_2V8_A	PM_PGOOD_P3V3_2V8_A - @mlb_lib.MLB		87C7
PM_PGOOD_PVAXG	PM_PGOOD_PVAXG - @mlb_lib.MLB		67B3
PM_PGOOD_PVCORE_CPU	PM_PGOOD_PVCORE_CPU - @mlb_lib.MLB		27A8 62B6 67C6
PM_PWRBTN_L	PM_PWRBTN_L - @mlb_lib.MLB		18A6 18C8 24C8 46C8
PM_RSMRST_L	PM_RSMRST_L - @mlb_lib.MLB		18C8 46D8
PM_S0_PGOOD	PM_S0_PGOOD - @mlb_lib.MLB		27A7
PM_SLP_S3_L	PM_SLP_S3_L - @mlb_lib.MLB		18A5 18C5 28C5 46C5 51C4
			62A4 62C4 100B5
PM_SLP_S4_L	PM_SLP_S4_L - @mlb_lib.MLB		18A5 18C5 28D6 46C5 62D6
			100B5
	DDRREG_EN - @mlb_lib.MLB		62D4 66C8
PM_SLP_S5_L	PM_SLP_S5_L - @mlb_lib.MLB		18A5 18C5 46C5 62D3 100B5
	P5VS4_EN - @mlb_lib.MLB		62D1 65B8
PM_SYNC	PM_SYNC - @mlb_lib.MLB		11C6 18C5 90C3
PM_SYSRST_L	PM_SYSRST_L - @mlb_lib.MLB		18C8 27A3 46B8
PM_THRMTRIP_L	PM_THRMTRIP_L - @mlb_lib.MLB		11C6 20C2 90B3
PM_THRMTRIP_L_R	PM_THRMTRIP_L_R - @mlb_lib.MLB		20D4 47C4 80B2
PM_WLAN_EN_L	PM_WLAN_EN_L - @mlb_lib.MLB		35C1 62A2
POWER_BTN_N	POWER_BTN_N - @mlb_lib.MLB		45A3 100B7
POWER_BTN_P	POWER_BTN_P - @mlb_lib.MLB		45B3 100B7
PP0V75_S0_DDRVTT	PP0V75_S0_DDRVTT - @mlb_lib.MLB		7C4 28B3 30A5 30A7 30C2
			31A5 31A7 31C2 66C5 100B5
PP0V75_S3_MEM_VREFCA	PP0V75_S3_MEM_VREFCA_A -		30B5 30C2 33C1
_A	@mlb_lib.MLB		
PP0V75_S3_MEM_VREFCA	PP0V75_S3_MEM_VREFCA_B -		31B5 31C2 33C1
_B	@mlb_lib.MLB		
PP0V75_S3_MEM_VREFDQ	PP0V75_S3_MEM_VREFDQ_A -		10B3 30D2 30D7 33D1
_A	@mlb_lib.MLB		
PP0V75_S3_MEM_VREFDQ	PP0V75_S3_MEM_VREFDQ_B -		10B3 31D2 31D7 33D1
_B	@mlb_lib.MLB		
PP1V0_GPU_DPLL	PP1V0_GPU_DPLL - @mlb_lib.MLB		79A6
PP1V0_GPU_DP_AB	PP1V0_GPU_DP_AB - @mlb_lib.MLB		81B4 81D5 81D5
PP1V0_GPU_DP_CD	PP1V0_GPU_DP_CD - @mlb_lib.MLB		81B4 81D7 81D7
PP1V0_GPU_DP_EF	PP1V0_GPU_DP_EF - @mlb_lib.MLB		81A4 81C7 81C7
PP1V0_GPU_PCIE_VDDC	PP1V0_GPU_PCIE_VDDC - @mlb_lib.MLB		74A7
PP1V0_GPU_PLL	PP1V0_GPU_PLL - @mlb_lib.MLB		74B6 74C6
PP1V0_S0_GPU	PP1V0_S0_GPU - @mlb_lib.MLB		73B2 74A7 74C8 76D1 79A8
			81A6 81B6 81B6
PP1V2_ENET	PP1V2_ENET - @mlb_lib.MLB		6D3 37D2 38C5 100C5
PP1V2_ENET_PHY_AVDDL	PP1V2_ENET_PHY_AVDDL - @mlb_lib.MLB		37D3
PP1V2_ENET_PHY_GPHYP	PP1V2_ENET_PHY_GPHYPLL -		37C3
LL	@mlb_lib.MLB		
PP1V2_ENET_PHY_PCIEP	PP1V2_ENET_PHY_PCIEPLL -		37D3
LL	@mlb_lib.MLB		
PP1V05_S0_PCH	PP1V05_S0_PCH - @mlb_lib.MLB		7D4 17C5 17C5 17D2 18D8
			21B1 21B1 21B5 21B7 21B7
			21B7 21B7 21C1 21C4 21C4
			21C4 21C5 21C5 21C5 21C5
			21C7 21C7 23B2 23B2 23B6
			23C1 23C2 23C2 23C5 23D1
			23D2 23D2 23D5 23D8 50C8
PP1V05_S0_PCH_VCCADP	PP1V05_S0_PCH_VCCADPLLA_F -		21B8 23B3
LLA_F	@mlb_lib.MLB		
PP1V05_S0_PCH_VCCADP	PP1V05_S0_PCH_VCCADPLLA_R -		23B5
LLA_R	@mlb_lib.MLB		
PP1V05_S0_PCH_VCCADP	PP1V05_S0_PCH_VCCADPLLB_F -		21B8 23B3
LLB_F	@mlb_lib.MLB		
PP1V05_S0_PCH_VCCADP	PP1V05_S0_PCH_VCCADPLLB_R -		23B5
LLB_R	@mlb_lib.MLB		
PP1V05_S0_PCH_VCCCLK	PP1V05_S0_PCH_VCCCLKDMI_F -		21C1 23D6
DMI_F	@mlb_lib.MLB		
PP1V05_S0_PCH_VCCCLK	PP1V05_S0_PCH_VCCCLKDMI_R -		23D7
DMI_R	@mlb_lib.MLB		
PP1V05_S0_VCCIO	PP1V05_S0_VCCIO - @mlb_lib.MLB		7D4 10C8 10D4 11B7 11C7
			13B5 13B5 13D6 15B8 67B6
			100B5
	PP1V05_S0 - @mlb_lib.MLB		7D4 24B3 24B4 24D1 24D6
			46A4 50C8 62A7 62B8 70C1
			85A8
PP1V05_S0_VCCQ	PP1V05_S0_VCCQ - @mlb_lib.MLB		11D3 13B6 15A6
PP1V05_S5_PCH	PP1V05_S5_PCH - @mlb_lib.MLB		24B3
PP1V05_T29	PP1V05_T29 - @mlb_lib.MLB		84D8 85A6 85C6
PP1V05_T29_VDD_DP	PP1V05_T29_VDD_DP - @mlb_lib.MLB		84C7
PP1V05_T29_VDD_DPPLL	PP1V05_T29_VDD_DPPLL - @mlb_lib.MLB		84C7
PP1V5_FW_VDDA	PP1V5_FW_VDDA - @mlb_lib.MLB		39D2
PP1V5_S0	PP1V5_S0 - @mlb_lib.MLB		7C7 17B4 21B5 23D4 39D1
			53D7 71B5 72B3 100B5
PP1V5_S0_GPU	PP1V5_S0_GPU - @mlb_lib.MLB		74D7 75A5 75A6 75A7 75A8
			75B8 76B1 78A6 78B2 78B6
			78C1 78C2 78C5 78C6 78C8
			78D4 78D8
PP1V5_S3	PP1V5_S3 - @mlb_lib.MLB		6B3 28B5 30C5 30C7 30D4
			31C5 31C7 31D4 32B6 61B7
			66C1 66C6 72B3 100B5
PP1V5_S3_CPU_VCCDQ	PP1V5_S3_CPU_VCCDQ - @mlb_lib.MLB		13C1 16A6
PP1V5_S3_REG	PP1V5_S3_REG - @mlb_lib.MLB		66C3
PP1V5_VDDQ_CPU	PP1V5_VDDQ_CPU - @mlb_lib.MLB		7A4 11C7 13B2 13D2 16B8
			28D4 31A5 32B6 50D8 62A8
			62C8
PP1V5_VDDQ_CPU_R	PP1V5_VDDQ_CPU_R - @mlb_lib.MLB		7B4 50D8 61B5
PP1V8_GPU_DPLL	PP1V8_GPU_DPLL - @mlb_lib.MLB		79A6
PP1V8_GPU_DP_AB	PP1V8_GPU_DP_AB - @mlb_lib.MLB		81B6 81C5 81C5 81D5 81D5
PP1V8_GPU_DP_CD	PP1V8_GPU_DP_CD - @mlb_lib.MLB		81B6 81C5 81C5 81D7 81D7
PP1V8_GPU_DP_EF	PP1V8_GPU_DP_EF - @mlb_lib.MLB		81A6 81C5 81C5 81C7 81C7
PP1V8_GPU_MEM_PLL	PP1V8_GPU_MEM_PLL - @mlb_lib.MLB		74B7
PP1V8_GPU_PCIE_VDDR	PP1V8_GPU_PCIE_VDDR - @mlb_lib.MLB		74A7
PP1V8_GPU_PLL	PP1V8_GPU_PLL - @mlb_lib.MLB		74B7
PP1V8_GPU_TSVDD	PP1V8_GPU_TSVDD - @mlb_lib.MLB		79A6
PP1V8_GPU_VDDR4	PP1V8_GPU_VDDR4 - @mlb_lib.MLB		74B6 74D2
PP1V8_GPU_VDD_CT	PP1V8_GPU_VDD_CT - @mlb_lib.MLB		74C7
PP1V8_S0	PP1V8_S0 - @mlb_lib.MLB		7D4 15B3 18C5 21B1 21B7
			21C1 21C1 21C5 23D3 26D7
			71B7 71D4
PP1V8_S0_CPU_VCCPLL_	PP1V8_S0_CPU_VCCPLL_R -		7C4 13B4 15B1
R	@mlb_lib.MLB		
PP1V8_S0_GPU	PP1V8_S0_GPU - @mlb_lib.MLB		74A8 74B8 74B8 74C8 74D4
			77C2 79A8 79B3 79B7 79B8
			79D7 81A8 81B8 81B8
PP1V96_FW_PLLVDD	PP1V96_FW_PLLVDD - @mlb_lib.MLB		39D2
PP1V96_FW_XTAL	PP1V96_FW_XTAL - @mlb_lib.MLB		39C1
PP1V96_S0_FW	PP1V96_S0_FW - @mlb_lib.MLB		39D1 40D5
PP2V2_FW_ESD	PP2V2_FW_ESD - @mlb_lib.MLB		41A6 41B2 41C4 41C4
PP3V3R1V8_ENET_LR_OU	PP3V3R1V8_ENET_LR_OUT -		37C1 37D5
T	@mlb_lib.MLB		
PP3V3R2V8_DPAPWR_D	PP3V3R2V8_DPAPWR_D - @mlb_lib.MLB		87D7
PP3V3R12V_SW_DPAPWR	PP3V3R12V_SW_DPAPWR - @mlb_lib.MLB		87C6 87D1 87D4
PP3V3R12V_SW_DPAPWR_	PP3V3R12V_SW_DPAPWR_F -		87C4 100B5
F	@mlb_lib.MLB		
PP3V3_ENET	PP3V3_ENET - @mlb_lib.MLB		6D3 26D7 26D7 37A8 37D8
			38C2 38D7 62B1 100C5

PP3V3_ENET_PHY_AVDDH	PP3V3_ENET_PHY_AVDDH - @mlb_lib.MLB		37C6
PP3V3_ENET_PHY_BIASV	PP3V3_ENET_PHY_BIASVDDH -		37D6
DDH	@mlb_lib.MLB		
PP3V3_ENET_PHY_XTALV	PP3V3_ENET_PHY_XTALVDDH -		37D6
DDH	@mlb_lib.MLB		
PP3V3_FW_AVDD	PP3V3_FW_AVDD - @mlb_lib.MLB		39D7
PP3V3_FW_PLLVDD	PP3V3_FW_PLLVDD - @mlb_lib.MLB		39D7
PP3V3_FW_VDDA	PP3V3_FW_VDDA - @mlb_lib.MLB		39D7
PP3V3_G3H	PP3V3_G3H - @mlb_lib.MLB		6B7 6D2 6D3 27D7 43D5
			45B2 46D4 47B5 47C1 47D8
			48D5 61C4 61D4 61D8 65C3
			65D7 100A5 100C5
PP3V3_G3_RTC	PP3V3_G3_RTC - @mlb_lib.MLB		6D7 17B8 18B5 21B8 27D6
			100C5
PP3V3_GPU_OSC_27M	PP3V3_GPU_OSC_27M - @mlb_lib.MLB		80C3
PP3V3_GPU_OSC_100M	PP3V3_GPU_OSC_100M - @mlb_lib.MLB		80C3
PP3V3_S0	PP3V3_S0 - @mlb_lib.MLB		6C2 7C7 13B6 17A6 17B7
			17C5 17D5 18B5 19D8 20A5
			20A8 20B8 20D2 20D7 21B4
			21C1 21C5 21C5 23A6 23A6
			23A8 23A8 23C6 23C8 23C8
			24D7 27A4 27A7 27C4 27C4
			30A7 30B3 31A7 31B3 34D4
			37C7 38A5 39B8 39C1 39D8
			40B7 40D7 41B4 47D3 49A5
			49A8 49B3 49B8 49D5 49D8
			50A7 50B7 50B7 50D3 50D7
			50D8 51B7 51C7 51D7 52B6
			52D7 53A8 53D1 57B8 58A4
			58D4 60C7 60C7 61C1 62A7
			62B6 62C8 67D2 67D5 71D8
			72C7 74C6 76A8 79C2 79C7
			80A6 80B5 80C4 80C6 80C8
			80D8 82A7 82C8 85B8 85C8
			86B5 86C4 86C8 86D6 88A7
			88C2 88C7 88D1 98C1 100C5
PP3V3_S0_AUDIO_F	PP3V3_S0_AUDIO_F - @mlb_lib.MLB		58A3 58A7 58B4 58B8 58C8
PP3V3_S0_HS_RX	PP3V3_S0_HS_RX - @mlb_lib.MLB		58D3
PP3V3_S0_PCH_VCC3_3_	PP3V3_S0_PCH_VCC3_3_CLK_F -		21D8 23C3
CLK_F	@mlb_lib.MLB		
PP3V3_S0_PCH_VCC3_3_	PP3V3_S0_PCH_VCC3_3_CLK_R -		23C5
CLK_R	@mlb_lib.MLB		
PP3V3_S0_PCH_VCCA_DA	PP3V3_S0_PCH_VCCA_DAC_F -		21B1 23C6
C_F	@mlb_lib.MLB		
PP3V3_S4	PP3V3_S4 - @mlb_lib.MLB		6B3 6D2 19C2 20B3 20C3
			20C3 25A3 25B3 25C3 25C3
			25C3 25C8 25D8 28B8 28C7
			28C7 33D8 34B6 34C5 35B3
			35C1 35C4 38B4 47B5 47C5
			49C3 49C5 50C7 50D8 61D1
			86B6 86C2 87C6 100C5
PP3V3_S4_BT_F	PP3V3_S4_BT_F - @mlb_lib.MLB		35C6 100D7
PP3V3_S4_VREFMRGN_CT	PP3V3_S4_VREFMRGN_CTRL -		33C7
RL	@mlb_lib.MLB		
PP3V3_S4_VREFMRGN_DA	PP3V3_S4_VREFMRGN_DAC -		33D7
C	@mlb_lib.MLB		
PP3V3_S5	PP3V3_S5 - @mlb_lib.MLB		6A7 17A3 17A6 17B7 18A8
			18A8 18D8 19C2 20A7 20B7
			20C8 21B5 21B5 21C1 21D5
			21D8 23B8 23C4 23D1 23D4
			23D5 24B3 24B8 24C2 25C3
			27A6 27A7 28D4 59C6 61D5
			62B3 62C7 62D8 87C7 98C1
			100C5
PP3V3_S5_AVREF_SMC	PP3V3_S5_AVREF_SMC - @mlb_lib.MLB		46D4 47D6 100B5
PP3V3_S5_SMC_AVCC	PP3V3_S5_SMC_AVCC - @mlb_lib.MLB		46D3
PP3V3_SW_SD_PWR	PP3V3_SW_SD_PWR - @mlb_lib.MLB		34D2 100C7
PP3V3_T29	PP3V3_T29 - @mlb_lib.MLB		17B6 20B3 20B8 26D7 83C2
			83C6 83D2 84D1 85B6 85C6
PP3V3_T29_DP	PP3V3_T29_DP - @mlb_lib.MLB		84D3
PP3V3_T29_DPBIAS	PP3V3_T29_DPBIAS - @mlb_lib.MLB		84C4
PP3V3_T29_PLL	PP3V3_T29_PLL - @mlb_lib.MLB		84C4
PP3V3_U5300	PP3V3_U5300 - @mlb_lib.MLB		50D6
PP3V3_WLAN	PP3V3_WLAN - @mlb_lib.MLB		35C6 35D7 47A1 100D7
PP3V3_WLAN_FET	PP3V3_WLAN_FET - @mlb_lib.MLB		35C3
PP4V5_AUDIO_ANALOG	PP4V5_AUDIO_ANALOG - @mlb_lib.MLB		53A3 53C5 53D1 53D7 100B5
PP5V_AUDIO_HPAMP	PP5V_AUDIO_HPAMP - @mlb_lib.MLB		53A6 55D6
PP5V_G3H	PP5V_G3H - @mlb_lib.MLB		6B7 45D6 47D8 61C4 65B7
			65D5 100C5
PP5V_HDMI_DDC_CONN	PP5V_HDMI_DDC_CONN - @mlb_lib.MLB		89B6 89C1 100B5
PP5V_HDMI_DDC_FUSE	PP5V_HDMI_DDC_FUSE - @mlb_lib.MLB		89B5 89D2
PP5V_S0	PP5V_S0 - @mlb_lib.MLB		7D7 23C8 24B4 24B4 41A5
			41B8 42D3 42D6 48D5 61B1
			62A8 64C6 67D5 68C7 68D7
			69D8 70C6 71B7 76A2 76B6
			76D5 77D6 89D4 100B7
			100C5 100C7
PP5V_S0_AUDIO	PP5V_S0_AUDIO - @mlb_lib.MLB		7D7 53A8
PP5V_S0_AUDIO_AMP	PP5V_S0_AUDIO_AMP - @mlb_lib.MLB		7C7 56C6
PP5V_S0_CPUVCCIOS0_V	PP5V_S0_CPUVCCIOS0_VCC -		70C6
CC	@mlb_lib.MLB		
PP5V_S0_CPU_VCORE_VC	PP5V_S0_CPU_VCORE_VCC -		67B1 67B4 67B8 67C7 67D4
C	@mlb_lib.MLB		
PP5V_S0_PCH_VSREF	PP5V_S0_PCH_VSREF - @mlb_lib.MLB		21D5 23B6
PP5V_S0_VCCSAS0_VCC	PP5V_S0_VCCSAS0_VCC - @mlb_lib.MLB		64C6
PP5V_S4	PP5V_S4 - @mlb_lib.MLB		6C3 28B3 28B6 43C8 43D8
			44C6 45D4 61B4 61B8 65B2
			66C7 82D8 87D6 87D8 100C5
PP5V_S4_DDRREG_V5IN	PP5V_S4_DDRREG_V5IN - @mlb_lib.MLB		66C7
PP5V_S4_GFXIMVP6_PVC	PP5V_S4_GFXIMVP6_PVCC -		82D7
C	@mlb_lib.MLB		
PP5V_S4_GFXIMVP6_VDD	PP5V_S4_GFXIMVP6_VDD - @mlb_lib.MLB		82D7
PP5V_S4_IR_R	PP5V_S4_IR_R - @mlb_lib.MLB		44C3 44C5
PP5V_S5	PP5V_S5 - @mlb_lib.MLB		6A7 23B8 61C1
PP5V_SUS_PCH_V5REFSU	PP5V_SUS_PCH_V5REFSUS -		21B5 23B7
S	@mlb_lib.MLB		
PP5V_U7100_PVCC	PP5V_U7100_PVCC - @mlb_lib.MLB		64C5
PP5V_U7700_PVCC	PP5V_U7700_PVCC - @mlb_lib.MLB		70C6
PP5V_USB2_PORT0	PP5V_USB2_PORT0 - @mlb_lib.MLB		43B6
PP5V_USB2_PORT0_F	PP5V_USB2_PORT0_F - @mlb_lib.MLB		43B4
PP5V_USB2_PORT1	PP5V_USB2_PORT1 - @mlb_lib.MLB		43C6
PP5V_USB2_PORT1_F	PP5V_USB2_PORT1_F - @mlb_lib.MLB		43C4
PP5V_USB2_PORT2	PP5V_USB2_PORT2 - @mlb_lib.MLB		43C6
PP5V_USB2_PORT2_F	PP5V_USB2_PORT2_F - @mlb_lib.MLB		43C2
PP5V_USB2_PORT3	PP5V_USB2_PORT3 - @mlb_lib.MLB		43D5
PP5V_USB2_PORT3_F	PP5V_USB2_PORT3_F - @mlb_lib.MLB		43D2
PP12V_G3H	PP12V_G3H - @mlb_lib.MLB		6C7 41D8 51B8 51C8 51D4
			51D8 60D7 65B8 65C4 65D3
			72C3 87D4
PP12V_G3H_CPUDDR	PP12V_G3H_CPUDDR - @mlb_lib.MLB		6C6 51C8 64D5 66D6 68D6
			69D3 70D5
PP12V_G3H_DDRS3REG_F	PP12V_G3H_DDRS3REG_FILT -		66D4
ILT	@mlb_lib.MLB		
PP12V_G3H_GPU	PP12V_G3H_GPU - @mlb_lib.MLB		6C6 51A8 76B7 76D3 77D4

			82D2
PP12V_G3H_PSU	PP12V_G3H_PSU - @mlb_lib.MLB		6C7 51D8 72B5 100D5
PP12V_S0_CPU_FLTRD	PP12V_S0_CPU_FLTRD - @mlb_lib.MLB		67B2 68C3 68D2
PP12V_S0_FAN	PP12V_S0_FAN - @mlb_lib.MLB		60D4
PP12V_S0_FAN0_F	PP12V_S0_FAN0_F - @mlb_lib.MLB		60C3 100D5
PPCPUVCCIO_S0_REG_R	PPCPUVCCIO_S0_REG_R - @mlb_lib.MLB		70C3
PPDDRVREF_S3	PPDDRVREF_S3 - @mlb_lib.MLB		6A3 33D3 66B5 100C5
PPIRRCVR_F	PPIRRCVR_F - @mlb_lib.MLB		45D2 100B7
PPIRRCVR_G3H_LED	PPIRRCVR_G3H_LED - @mlb_lib.MLB		45D3
PPUSB_HUB1_CRFILT	PPUSB_HUB1_CRFILT - @mlb_lib.MLB		25D5
PPUSB_HUB1_PLLFILT	PPUSB_HUB1_PLLFILT - @mlb_lib.MLB		25D5
PPUSB_HUB2_CRFILT	PPUSB_HUB2_CRFILT - @mlb_lib.MLB		25B5
PPUSB_HUB2_PLLFILT	PPUSB_HUB2_PLLFILT - @mlb_lib.MLB		25B5
PPVAXG_S0_CPU	PPVAXG_S0_CPU - @mlb_lib.MLB		7B7 13D4 16D8 50B4 67D8
			69C1
PPVAXG_S0_CPU_RS	PPVAXG_S0_CPU_RS - @mlb_lib.MLB		69C4
PPVBATT_G3_RTC	PPVBATT_G3_RTC - @mlb_lib.MLB		6D7 27D8
PPVBATT_G3_RTC_R	PPVBATT_G3_RTC_R - @mlb_lib.MLB		27D7
PPVCCSA_S0_CPU	PPVCCSA_S0_CPU - @mlb_lib.MLB		7B7 13B4 13C1 16B4 50A5
			64C1
PPVCCSA_S0_REG_R	PPVCCSA_S0_REG_R - @mlb_lib.MLB		64C3
PPVCORE_GPU	PPVCORE_GPU - @mlb_lib.MLB		50A5 74D3 82C1 82C8
PPVCORE_GPU_REG_R	PPVCORE_GPU_REG_R - @mlb_lib.MLB		82C4
PPVCORE_S0_CPU	PPVCORE_S0_CPU - @mlb_lib.MLB		7B7 10D4 10D4 13D8 15D8
			50C4 67A8 68A4 68C2 68D2
			100B5
PPVIN_S5_GPU	PPVIN_S5_GPU - @mlb_lib.MLB		82D4
PPVOUT_G3_PCH_DCPRTC	PPVOUT_G3_PCH_DCPRTC - @mlb_lib.MLB		21C8
PPVOUT_S0_PCH_DCPSST	PPVOUT_S0_PCH_DCPSST - @mlb_lib.MLB		21B8
PPVP_FW_PHY_CPS	PPVP_FW_PHY_CPS - @mlb_lib.MLB		39B1 41D3
PSU_TEMP	PSU_TEMP - @mlb_lib.MLB		47A6 72C5 100C5
PU_FW_VP	PU_FW_VP - @mlb_lib.MLB		39D2
PU_HDMI_LS_RSV1	PU_HDMI_LS_RSV1 - @mlb_lib.MLB		88B6
PU_SDCONN_OC_L	PU_SDCONN_OC_L - @mlb_lib.MLB		34D3
PU_USB1_PRT4N	PU_USB1_PRT4N - @mlb_lib.MLB		25C5
PU_USB1_PRT4P	PU_USB1_PRT4P - @mlb_lib.MLB		25C5
PU_USB2_PRT4N	PU_USB2_PRT4N - @mlb_lib.MLB		25A5
PU_USB2_PRT4P	PU_USB2_PRT4P - @mlb_lib.MLB		25A5
PVCCIO_S0_SMC_R	PVCCIO_S0_SMC_R - @mlb_lib.MLB		46A5
PVCCSA_EN	PVCCSA_EN - @mlb_lib.MLB		62C1 64C6
PVCCSA_PGOOD	PVCCSA_PGOOD - @mlb_lib.MLB		62A6 64C6
RTC_RESET_L	RTC_RESET_L - @mlb_lib.MLB		17A7 17D8
RT_1V8S0	RT_1V8S0 - @mlb_lib.MLB		71C6
S0PGD_BJT_GND_R	S0PGD_BJT_GND_R - @mlb_lib.MLB		62B6
S0PGD_C	S0PGD_C - @mlb_lib.MLB		62C7
S5_PWRGD	S5_PWRGD - @mlb_lib.MLB		46D8 62D7
SATARDRVR_EN	SATARDRVR_EN - @mlb_lib.MLB		17A5 17C5
SATA_HDD1_D2R_CONN_N	SATA_HDD1_D2R_CONN_N - @mlb_lib.MLB		42B5 42D7 92D3 100C7
SATA_HDD1_D2R_CONN_P	SATA_HDD1_D2R_CONN_P - @mlb_lib.MLB		42B5 42D7 92D3 100C7
SATA_HDD1_D2R_DF_N	SATA_HDD1_D2R_DF_N - @mlb_lib.MLB		42B7 92D3
SATA_HDD1_D2R_DF_P	SATA_HDD1_D2R_DF_P - @mlb_lib.MLB		42B7 92D3
SATA_HDD1_D2R_N	SATA_HDD1_D2R_N - @mlb_lib.MLB		17D5 42B8 92D3
SATA_HDD1_D2R_P	SATA_HDD1_D2R_P - @mlb_lib.MLB		17D5 42B8 92D3
SATA_HDD1_R2D_CONN_N	SATA_HDD1_R2D_CONN_N - @mlb_lib.MLB		42C5 42D7 92D3 100C7
SATA_HDD1_R2D_CONN_P	SATA_HDD1_R2D_CONN_P - @mlb_lib.MLB		42C5 42D7 92D3 100C7
SATA_HDD1_R2D_C_N	SATA_HDD1_R2D_C_N - @mlb_lib.MLB		17D5 42C8 92D3
SATA_HDD1_R2D_C_P	SATA_HDD1_R2D_C_P - @mlb_lib.MLB		17D5 42C8 92D3
SATA_HDD1_R2D_DF_N	SATA_HDD1_R2D_DF_N - @mlb_lib.MLB		42C7 92D3
SATA_HDD1_R2D_DF_P	SATA_HDD1_R2D_DF_P - @mlb_lib.MLB		42C7 92D3
SATA_HDD2_D2R_CONN_N	SATA_HDD2_D2R_CONN_N - @mlb_lib.MLB		42B1 42D4 92D3 100B7
SATA_HDD2_D2R_CONN_P	SATA_HDD2_D2R_CONN_P - @mlb_lib.MLB		42B1 42D4 92D3 100B7
SATA_HDD2_D2R_DF_N	SATA_HDD2_D2R_DF_N - @mlb_lib.MLB		42B3 92D3
SATA_HDD2_D2R_DF_P	SATA_HDD2_D2R_DF_P - @mlb_lib.MLB		42B3 92C3
SATA_HDD2_D2R_N	SATA_HDD2_D2R_N - @mlb_lib.MLB		17D5 42B4 92D3
SATA_HDD2_D2R_P	SATA_HDD2_D2R_P - @mlb_lib.MLB		17D5 42B4 92D3
SATA_HDD2_R2D_CONN_N	SATA_HDD2_R2D_CONN_N - @mlb_lib.MLB		42C1 42D4 92D3 100B7
SATA_HDD2_R2D_CONN_P	SATA_HDD2_R2D_CONN_P - @mlb_lib.MLB		42C1 42D4 92D3 100B7
SATA_HDD2_R2D_C_N	SATA_HDD2_R2D_C_N - @mlb_lib.MLB		17D5 42C4 92D3
SATA_HDD2_R2D_C_P	SATA_HDD2_R2D_C_P - @mlb_lib.MLB		17D5 42C4 92D3
SATA_HDD2_R2D_DF_N	SATA_HDD2_R2D_DF_N - @mlb_lib.MLB		42C3 92C3
SATA_HDD2_R2D_DF_P	SATA_HDD2_R2D_DF_P - @mlb_lib.MLB		42C3 92C3
SDCONNF_CLK	SDCONNF_CLK - @mlb_lib.MLB		34C5 94C3
SDCONNF_CLK_FF	SDCONNF_CLK_FF - @mlb_lib.MLB		34C6 94C3
SDCONN_CLK	SDCONN_CLK - @mlb_lib.MLB		34C7 37B1 94C3 100C7
SDCONN_CLK_FF	SDCONN_CLK_FF - @mlb_lib.MLB		34C4 94C3
SDCONN_CLK_R	SDCONN_CLK_R - @mlb_lib.MLB		34C3 94C3
SDCONN_CMD	SDCONN_CMD - @mlb_lib.MLB		34C5 37B1 94C3 100C7
SDCONN_CMD_R	SDCONN_CMD_R - @mlb_lib.MLB		34C3 34D7 94C3
SDCONN_DATA<0>	SDCONN_DATA<0> - @mlb_lib.MLB		34C5 37B1
SDCONN_DATA<7..0>	SDCONN_DATA<7..0> - @mlb_lib.MLB		94C3 100C7
SDCONN_DATA<1>	SDCONN_DATA<1> - @mlb_lib.MLB		34C5 37B1
SDCONN_DATA<2>	SDCONN_DATA<2> - @mlb_lib.MLB		34C5 37B1
SDCONN_DATA<3>	SDCONN_DATA<3> - @mlb_lib.MLB		34C5 37B1
SDCONN_DATA<4>	SDCONN_DATA<4> - @mlb_lib.MLB		34C5 37B1
SDCONN_DATA<5>	SDCONN_DATA<5> - @mlb_lib.MLB		34C5 37B1
SDCONN_DATA<6>	SDCONN_DATA<6> - @mlb_lib.MLB		34C5 37B1
SDCONN_DATA<7>	SDCONN_DATA<7> - @mlb_lib.MLB		34C5 37B1
SDCONN_DATA_R<0>	SDCONN_DATA_R<0> - @mlb_lib.MLB		34C3 34D7
SDCONN_DATA_R<7..0>	SDCONN_DATA_R<7..0> - @mlb_lib.MLB		94C3
SDCONN_DATA_R<1>	SDCONN_DATA_R<1> - @mlb_lib.MLB		34C3 34D7
SDCONN_DATA_R<2>	SDCONN_DATA_R<2> - @mlb_lib.MLB		34C3 34D7
SDCONN_DATA_R<3>	SDCONN_DATA_R<3> - @mlb_lib.MLB		34C3 34C7
SDCONN_DATA_R<4>	SDCONN_DATA_R<4> - @mlb_lib.MLB		34C3 34C7
SDCONN_DATA_R<5>	SDCONN_DATA_R<5> - @mlb_lib.MLB		34C3 34C7
SDCONN_DATA_R<6>	SDCONN_DATA_R<6> - @mlb_lib.MLB		34C3 34C7
SDCONN_DATA_R<7>	SDCONN_DATA_R<7> - @mlb_lib.MLB		34C3 34C7
SDCONN_DETECT	SDCONN_DETECT - @mlb_lib.MLB		34B6 34C3 34C7 100C7
SDCONN_DETECT_L	SDCONN_DETECT_L - @mlb_lib.MLB		34B5
SDCONN_STATE_CHANGE	SDCONN_STATE_CHANGE - @mlb_lib.MLB		19C1 24C4 34B2
SDCONN_STATE_CHANGE_	SDCONN_STATE_CHANGE_S1R -		34B4
S1R	@mlb_lib.MLB		
SDCONN_STATE_CHANGE_	SDCONN_STATE_CHANGE_S2R -		34A4
S2R	@mlb_lib.MLB		
SDCONN_WP	SDCONN_WP - @mlb_lib.MLB		34C3 34C7

SPI_CS0_R_L	SPI_CS0_R_L - @mlb_lib.MLB	17C8	48B6 93C3
SPI_MISO	SPI_MISO - @mlb_lib.MLB	17C8	48A6 93C3 100A5
SPI_MLB_CLK	SPI_MLB_CLK - @mlb_lib.MLB	48B3	59C5
SPI_MLB_CS_L	SPI_MLB_CS_L - @mlb_lib.MLB	48B3	59C5
SPI_MLB_MISO	SPI_MLB_MISO - @mlb_lib.MLB	48A3	59C4
SPI_MLB_MOSI	SPI_MLB_MOSI - @mlb_lib.MLB	48A3	59C4
SPI_MOSI	SPI_MOSI - @mlb_lib.MLB	48A5	93C3 100A5
SPI_MOSI_R	SPI_MOSI_R - @mlb_lib.MLB	17C8	48A6 93C3
SPI_WP_L	SPI_WP_L - @mlb_lib.MLB	59C5	
SPKRAMP_M_N_OUT	SPKRAMP_M_N_OUT - @mlb_lib.MLB	56B3	57B2 100D5
SPKRAMP_M_P_OUT	SPKRAMP_M_P_OUT - @mlb_lib.MLB	56B3	57B2 100D5
SS_1V8S0	SS_1V8S0 - @mlb_lib.MLB	71C7	
SUSWARN_L	SUSWARN_L - @mlb_lib.MLB	18A6	18B7 18C8
SW_1V8S0	SW_1V8S0 - @mlb_lib.MLB	71D6	
SYSCLK_CLK25M_ENET_SR	SYSCLK_CLK25M_ENET_SR - @mlb_lib.MLB	26C4	
SYSCLK_CLK25M_SB	SYSCLK_CLK25M_SB - @mlb_lib.MLB	26C4	
SYSCLK_CLK25M_T29	SYSCLK_CLK25M_T29 - @mlb_lib.MLB	26C2	83C1
SYSCLK_CLK25M_T29_R	SYSCLK_CLK25M_T29_R - @mlb_lib.MLB	83C3	
SYSCLK_CLK25M_T29_SR	SYSCLK_CLK25M_T29_SR - @mlb_lib.MLB	26C4	
SYSCLK_CLK25M_X1	SYSCLK_CLK25M_X1 - @mlb_lib.MLB	26C6	
SYSCLK_CLK25M_X2	SYSCLK_CLK25M_X2 - @mlb_lib.MLB	26C7	
SYSCLK_CLK25M_X2_R	SYSCLK_CLK25M_X2_R - @mlb_lib.MLB	26C6	
SYS_ONEWIRE	SYS_ONEWIRE - @mlb_lib.MLB	46B8	47B2
SYS_PWROK_R	SYS_PWROK_R - @mlb_lib.MLB	27A6	
T29DPA_CONFIG1_RC	T29DPA_CONFIG1_RC - @mlb_lib.MLB	86A4	87A8
T29DPA_CONFIG2_RC	T29DPA_CONFIG2_RC - @mlb_lib.MLB	86A4	87A8
T29DPA_D2R1_AUXCH_CC_N	T29DPA_D2R1_AUXCH_CC_N - @mlb_lib.MLB	95A3	
T29DPA_D2R1_AUXCH_CC_P	T29DPA_D2R1_AUXCH_CC_P - @mlb_lib.MLB	95A3	
T29DPA_D2R1_AUXCH_N	T29DPA_D2R1_AUXCH_N - @mlb_lib.MLB	87B6	95B3
T29DPA_D2R1_AUXCH_P	T29DPA_D2R1_AUXCH_P - @mlb_lib.MLB	87B6	95B3
T29DPA_HPD	T29DPA_HPD - @mlb_lib.MLB	86A7	87A8
T29DPA_HPD_R	T29DPA_HPD_R - @mlb_lib.MLB	87A5	
T29DPA_ML_C_N<0>	T29DPA_ML_C_N<0> - @mlb_lib.MLB	86D1	87B1
T29DPA_ML_C_N<3..0>	T29DPA_ML_C_N<3..0> - @mlb_lib.MLB	95B3	
T29DPA_ML_C_N<2>	T29DPA_ML_C_N<2> - @mlb_lib.MLB	86D1	87B1
T29DPA_ML_C_P<0>	T29DPA_ML_C_P<0> - @mlb_lib.MLB	86D1	87B1
T29DPA_ML_C_P<3..0>	T29DPA_ML_C_P<3..0> - @mlb_lib.MLB	95B3	
T29DPA_ML_C_P<2>	T29DPA_ML_C_P<2> - @mlb_lib.MLB	86D1	87B1
T29DPA_ML_N<0>	T29DPA_ML_N<0> - @mlb_lib.MLB	87B2	
T29DPA_ML_N<3..0>	T29DPA_ML_N<3..0> - @mlb_lib.MLB	95B3	
T29DPA_ML_N<1>	T29DPA_ML_N<1> - @mlb_lib.MLB	86B1	87B1
T29DPA_ML_N<2>	T29DPA_ML_N<2> - @mlb_lib.MLB	87B2	
T29DPA_ML_N<3>	T29DPA_ML_N<3> - @mlb_lib.MLB	86B1	87B8
T29DPA_ML_P<0>	T29DPA_ML_P<0> - @mlb_lib.MLB	87B2	
T29DPA_ML_P<3..0>	T29DPA_ML_P<3..0> - @mlb_lib.MLB	95B3	
T29DPA_ML_P<1>	T29DPA_ML_P<1> - @mlb_lib.MLB	86B1	87B1
T29DPA_ML_P<2>	T29DPA_ML_P<2> - @mlb_lib.MLB	87B2	
T29DPA_ML_P<3>	T29DPA_ML_P<3> - @mlb_lib.MLB	86B1	87B8
T29ROM_HOLD_L	T29ROM_HOLD_L - @mlb_lib.MLB	83C8	
T29ROM_WP_L	T29ROM_WP_L - @mlb_lib.MLB	83C8	
T29_A_BIAS	T29_A_BIAS - @mlb_lib.MLB	85B3	86A8 86B3 87C6
T29_A_BIASON	T29_A_BIASON - @mlb_lib.MLB	85B1	86D4
T29_A_BIASOP	T29_A_BIASOP - @mlb_lib.MLB	85B1	86D4
T29_A_BIASIN	T29_A_BIASIN - @mlb_lib.MLB	85B1	87B8
T29_A_BIASIP	T29_A_BIASIP - @mlb_lib.MLB	85B1	87B8
T29_A_BIASZN	T29_A_BIASZN - @mlb_lib.MLB	85A1	86C4
T29_A_BIASZP	T29_A_BIASZP - @mlb_lib.MLB	85A1	86D4
T29_A_HV_EN	T29_A_HV_EN - @mlb_lib.MLB	86A3	87C4
T29_A_HV_EN_R	T29_A_HV_EN_R - @mlb_lib.MLB	86A5	
T29_A_LSX_P2R	T29_A_LSX_P2R - @mlb_lib.MLB	86A5	
T29_A_LSX_R2P	T29_A_LSX_R2P - @mlb_lib.MLB	86A5	
T29_A_RSVD_N	T29_A_RSVD_N - @mlb_lib.MLB	86B3	
T29_A_RSVD_P	T29_A_RSVD_P - @mlb_lib.MLB	86B3	
T29_A_UC_ADDR	T29_A_UC_ADDR - @mlb_lib.MLB	86A4	86A8
T29_CLKREQ_ISOL_L	T29_CLKREQ_ISOL_L - @mlb_lib.MLB	83C5	85B6
T29_CLKREQ_L	T29_CLKREQ_L - @mlb_lib.MLB	17B4	17B5 85B8
T29_D2R1_BIASN	T29_D2R1_BIASN - @mlb_lib.MLB	86B3	
T29_D2R1_BIASP	T29_D2R1_BIASP - @mlb_lib.MLB	86B3	
T29_D2R_CC_N<0>	T29_D2R_CC_N<0> - @mlb_lib.MLB	95A3	
T29_D2R_CC_P<0>	T29_D2R_CC_P<0> - @mlb_lib.MLB	95A3	
T29_D2R_C_N<0>	T29_D2R_C_N<0> - @mlb_lib.MLB	86D1	87B8 95C3
T29_D2R_C_N<1>	T29_D2R_C_N<1> - @mlb_lib.MLB	86D1	87B8 95C3
T29_D2R_C_P<0>	T29_D2R_C_P<0> - @mlb_lib.MLB	86D1	87B8 95C3
T29_D2R_C_P<1>	T29_D2R_C_P<1> - @mlb_lib.MLB	86D1	87B8 95C3
T29_D2R_N<0>	T29_D2R_N<0> - @mlb_lib.MLB	83A3	86D5
T29_D2R_N<3..0>	T29_D2R_N<3..0> - @mlb_lib.MLB	95C3	
T29_D2R_N<1>	T29_D2R_N<1> - @mlb_lib.MLB	83A3	86D5
T29_D2R_P<0>	T29_D2R_P<0> - @mlb_lib.MLB	83A3	86D5
T29_D2R_P<3..0>	T29_D2R_P<3..0> - @mlb_lib.MLB	95C3	
T29_D2R_P<1>	T29_D2R_P<1> - @mlb_lib.MLB	83A3	86D5
T29_DP_ATEST	T29_DP_ATEST - @mlb_lib.MLB	83B3	
T29_DP_A_PWR_EN	T29_DP_A_PWR_EN - @mlb_lib.MLB	87C7	87D8
T29_DP_PORTA_PWR_EN	T29_DP_PORTA_PWR_EN - @mlb_lib.MLB	19C1	24D4 87C8
T29_DP_RES	T29_DP_RES - @mlb_lib.MLB	83B3	
T29_GPIO<1>	T29_GPIO<1> - @mlb_lib.MLB	83C5	
T29_GPIO<2>	T29_GPIO<2> - @mlb_lib.MLB	83C5	
T29_LSEO<0>	T29_LSEO<0> - @mlb_lib.MLB	83A3	86A7
T29_LSEO<1>	T29_LSEO<1> - @mlb_lib.MLB	83A3	86A4
T29_LSEO_LSOE0	T29_LSEO_LSOE0 - @mlb_lib.MLB	83A5	
T29_LSEO_LSOE1	T29_LSEO_LSOE1 - @mlb_lib.MLB	83A5	
T29_LSOE<0>	T29_LSOE<0> - @mlb_lib.MLB	83A3	86A7
T29_LSOE<1>	T29_LSOE<1> - @mlb_lib.MLB	83A3	86A7
T29_MCU_INT_L	T29_MCU_INT_L - @mlb_lib.MLB	19D6	86A7
T29_MONDC0	T29_MONDC0 - @mlb_lib.MLB	83D5	
T29_MONDC1	T29_MONDC1 - @mlb_lib.MLB	83D5	
T29_MONOBSN	T29_MONOBSN - @mlb_lib.MLB	83C5	
T29_MONOBSP	T29_MONOBSP - @mlb_lib.MLB	83D5	
T29_PCIE_WAKE_L	T29_PCIE_WAKE_L - @mlb_lib.MLB	83D3	
T29_PWR_EN	T29_PWR_EN - @mlb_lib.MLB	20B1	85A8
T29_PWR_EN_PCH	T29_PWR_EN_PCH - @mlb_lib.MLB	17D5	20B3
T29_PWR_EN_U2916	T29_PWR_EN_U2916 - @mlb_lib.MLB	85A7	
T29_R2D_C_F_N<0>	T29_R2D_C_F_N<0> - @mlb_lib.MLB	86D4	
T29_R2D_C_F_N<1..0>	T29_R2D_C_F_N<1..0> - @mlb_lib.MLB	95B3	
T29_R2D_C_F_N<1>	T29_R2D_C_F_N<1> - @mlb_lib.MLB	86D4	
T29_R2D_C_F_P<0>	T29_R2D_C_F_P<0> - @mlb_lib.MLB	86D4	
T29_R2D_C_F_P<1..0>	T29_R2D_C_F_P<1..0> - @mlb_lib.MLB	95B3	
T29_R2D_C_F_P<1>	T29_R2D_C_F_P<1> - @mlb_lib.MLB	86D4	
T29_R2D_C_N<0>	T29_R2D_C_N<0> - @mlb_lib.MLB	83A3	86D5
T29_R2D_C_N<3..0>	T29_R2D_C_N<3..0> - @mlb_lib.MLB	95C3	
T29_R2D_C_N<1>	T29_R2D_C_N<1> - @mlb_lib.MLB	83A3	86D5
T29_R2D_C_P<0>	T29_R2D_C_P<0> - @mlb_lib.MLB	83A3	86D5
T29_R2D_C_P<3..0>	T29_R2D_C_P<3..0> - @mlb_lib.MLB	95C3	
T29_R2D_C_P<1>	T29_R2D_C_P<1> - @mlb_lib.MLB	83A3	86D5
T29_R2D_N<0>	T29_R2D_N<0> - @mlb_lib.MLB	86D3	95C3
T29_R2D_N<1>	T29_R2D_N<1> - @mlb_lib.MLB	86D3	95C3
T29_R2D_P<0>	T29_R2D_P<0> - @mlb_lib.MLB	86D3	95C3
T29_R2D_P<1>	T29_R2D_P<1> - @mlb_lib.MLB	86D3	95C3
T29_RBIAS	T29_RBIAS - @mlb_lib.MLB	83C3	
T29_RESET_L	T29_RESET_L - @mlb_lib.MLB	83D2	85C6
T29_RSENSE	T29_RSENSE - @mlb_lib.MLB	83D3	
T29_RSVD	T29_RSVD - @mlb_lib.MLB	83C5	

T29_SPI_CLK	T29_SPI_CLK - @mlb_lib.MLB	83C5	95C3
T29_SPI_CS_L	T29_SPI_CS_L - @mlb_lib.MLB	83C5	95C3
T29_SPI_MISO	T29_SPI_MISO - @mlb_lib.MLB	83C5	95C3
T29_SPI_MOSI	T29_SPI_MOSI - @mlb_lib.MLB	83C5	95C3
T29_SW_RESET_L	T29_SW_RESET_L - @mlb_lib.MLB	20A4	20C6 85B8
T29_TEST_EN	T29_TEST_EN - @mlb_lib.MLB	83C5	
T29_TEST_POINT_3	T29_TEST_POINT_3 - @mlb_lib.MLB	83C5	
T29_THERMD_N	T29_THERMD_N - @mlb_lib.MLB	98B1	
T29_THERMD_P	T29_THERMD_P - @mlb_lib.MLB	98B1	
T29_THRM_SNS3_N	T29_THRM_SNS3_N - @mlb_lib.MLB	52A7	
T29_THRM_SNS3_P	T29_THRM_SNS3_P - @mlb_lib.MLB	52A7	
T29_TMU_CLK_IN	T29_TMU_CLK_IN - @mlb_lib.MLB	83C3	
T29_TMU_CLK_OUT	T29_TMU_CLK_OUT - @mlb_lib.MLB	83C3	
TIPDET_UNFILT	TIPDET_UNFILT - @mlb_lib.MLB	58A3	58D4
TP_1V0S_S0_PCH_VCCAP LLEXP	TP_1V0S_S0_PCH_VCCAPLLEXP - @mlb_lib.MLB	21C4	
TP_AUD_DMIC_CLK	TP_AUD_DMIC_CLK - @mlb_lib.MLB	53C2	
TP_BCM57765_SPD100LE D_L	TP_BCM57765_SPD100LED_L - @mlb_lib.MLB	37B6	
TP_BCM57765_TRAFFICL ED_L	TP_BCM57765_TRAFFICLED_L - @mlb_lib.MLB	37B6	
TP_CLK98M_TS_L	TP_CLK98M_TS_L - @mlb_lib.MLB	39C1	
TP_CPU_CFG<8>	TP_CPU_CFG<8> - @mlb_lib.MLB	10D3	
TP_CPU_CFG<9>	TP_CPU_CFG<9> - @mlb_lib.MLB	10D3	
TP_CPU_CFG<10>	TP_CPU_CFG<10> - @mlb_lib.MLB	10D3	
TP_CPU_CFG<11>	TP_CPU_CFG<11> - @mlb_lib.MLB	10D3	
TP_CPU_CFG<12>	TP_CPU_CFG<12> - @mlb_lib.MLB	10D3	
TP_CPU_CFG<13>	TP_CPU_CFG<13> - @mlb_lib.MLB	10D3	
TP_CPU_CFG<14>	TP_CPU_CFG<14> - @mlb_lib.MLB	10D3	
TP_CPU_CFG<15>	TP_CPU_CFG<15> - @mlb_lib.MLB	10D3	
TP_CPU_CFG<17>	TP_CPU_CFG<17> - @mlb_lib.MLB	10D3	
TP_CPU_DC_TEST_A4	TP_CPU_DC_TEST_A4 - @mlb_lib.MLB	10C1	
TP_CPU_DC_TEST_A58	TP_CPU_DC_TEST_A58 - @mlb_lib.MLB	10C1	
TP_CPU_DC_TEST_BD1	TP_CPU_DC_TEST_BD1 - @mlb_lib.MLB	10B1	
TP_CPU_DC_TEST_BD61	TP_CPU_DC_TEST_BD61 - @mlb_lib.MLB	10C1	
TP_CPU_DC_TEST_BG4	TP_CPU_DC_TEST_BG4 - @mlb_lib.MLB	10C1	
TP_CPU_DC_TEST_BG58	TP_CPU_DC_TEST_BG58 - @mlb_lib.MLB	10C1	
TP_CPU_DC_TEST_D1	TP_CPU_DC_TEST_D1 - @mlb_lib.MLB	10C1	
TP_CPU_DC_TEST_D61	TP_CPU_DC_TEST_D61 - @mlb_lib.MLB	10C1	
TP_CPU_VCC_DIE_SENSE	TP_CPU_VCC_DIE_SENSE - @mlb_lib.MLB	10C4	
TP_CPU_VDDQ_SENSEN	TP_CPU_VDDQ_SENSEN - @mlb_lib.MLB	13C1	
TP_CPU_VDDQ_SENSEP	TP_CPU_VDDQ_SENSEP - @mlb_lib.MLB	13C1	
TP_DPAPWRSW_FLT_L	TP_DPAPWRSW_FLT_L - @mlb_lib.MLB	87D1	
TP_DVPCLK	TP_DVPCLK - @mlb_lib.MLB	79D6	
TP_DVPCNTL<0>	TP_DVPCNTL<0> - @mlb_lib.MLB	79D6	
TP_DVPCNTL<1>	TP_DVPCNTL<1> - @mlb_lib.MLB	79D6	
TP_DVPCNTL<2>	TP_DVPCNTL<2> - @mlb_lib.MLB	79D6	
TP_DVPCNTL_M<0>	TP_DVPCNTL_M<0> - @mlb_lib.MLB	79D6	
TP_DVPCNTL_M<1>	TP_DVPCNTL_M<1> - @mlb_lib.MLB	79D6	
TP_DVPDATA<4>	TP_DVPDATA<4> - @mlb_lib.MLB	79D6	
TP_DVPDATA<5>	TP_DVPDATA<5> - @mlb_lib.MLB	79D6	
TP_DVPDATA<6>	TP_DVPDATA<6> - @mlb_lib.MLB	79D6	
TP_DVPDATA<7>	TP_DVPDATA<7> - @mlb_lib.MLB	79D6	
TP_DVPDATA<8>	TP_DVPDATA<8> - @mlb_lib.MLB	79D6	
TP_DVPDATA<9>	TP_DVPDATA<9> - @mlb_lib.MLB	79D6	
TP_DVPDATA<10>	TP_DVPDATA<10> - @mlb_lib.MLB	79D6	
TP_DVPDATA<11>	TP_DVPDATA<11> - @mlb_lib.MLB	79D6	
TP_DVPDATA<12>	TP_DVPDATA<12> - @mlb_lib.MLB	79D6	
TP_DVPDATA<13>	TP_DVPDATA<13> - @mlb_lib.MLB	79D6	
TP_DVPDATA<14>	TP_DVPDATA<14> - @mlb_lib.MLB	79D6	
TP_DVPDATA<15>	TP_DVPDATA<15> - @mlb_lib.MLB	79D6	
TP_DVPDATA<16>	TP_DVPDATA<16> - @mlb_lib.MLB	79D6	
TP_DVPDATA<17>	TP_DVPDATA<17> - @mlb_lib.MLB	79D6	
TP_DVPDATA<18>	TP_DVPDATA<18> - @mlb_lib.MLB	79C6	
TP_DVPDATA<19>	TP_DVPDATA<19> - @mlb_lib.MLB	79C6	
TP_DVPDATA<20>	TP_DVPDATA<20> - @mlb_lib.MLB	79C6	
TP_DVPDATA<21>	TP_DVPDATA<21> - @mlb_lib.MLB	79C6	
TP_DVPDATA<22>	TP_DVPDATA<22> - @mlb_lib.MLB	79C6	
TP_DVPDATA<23>	TP_DVPDATA<23> - @mlb_lib.MLB	79C6	
TP_FWOHCI_XO	TP_FWOHCI_XO - @mlb_lib.MLB	39C2	
TP_FWPHY_CNA	TP_FWPHY_CNA - @mlb_lib.MLB	39B2	
TP_FWXIO_GRST_L	TP_FWXIO_GRST_L - @mlb_lib.MLB	39B6	
TP_FWXIO_JTAG_TDI	TP_FWXIO_JTAG_TDI - @mlb_lib.MLB	39B6	
TP_FWXIO_JTAG_TDO	TP_FWXIO_JTAG_TDO - @mlb_lib.MLB	39B6	
TP_FWXIO_JTAG_TMS	TP_FWXIO_JTAG_TMS - @mlb_lib.MLB	39B6	
TP_GFXIMVP6_IMON	TP_GFXIMVP6_IMON - @mlb_lib.MLB	82C7	
TP_GPU_GENERICA	TP_GPU_GENERICA - @mlb_lib.MLB	79B6	
TP_HDMI_CEC_CONN	TP_HDMI_CEC_CONN - @mlb_lib.MLB	89C4	
TP_IRUC_RCVR_PWR_EN_ L	TP_IRUC_RCVR_PWR_EN_L - @mlb_lib.MLB	44C6	
TP_LPC_CLK33M_GMUX_R	TP_LPC_CLK33M_GMUX_R - @mlb_lib.MLB	19C6	
TP_PCH_TP23	TP_PCH_TP23 - @mlb_lib.MLB	18C5	
TP_PCI_CLK33M_OUT3	TP_PCI_CLK33M_OUT3 - @mlb_lib.MLB	19C6	
TP_PM_SLP_A_L	TP_PM_SLP_A_L - @mlb_lib.MLB	18C5	
TP_PM_SLP_SUS_L	TP_PM_SLP_SUS_L - @mlb_lib.MLB	18B5	
TP_PPVOUT_PCH_DCPSUS BYP	TP_PPVOUT_PCH_DCPSUSBYP - @mlb_lib.MLB	21D8	
TP_SPI_CS1_L	TP_SPI_CS1_L - @mlb_lib.MLB	17C8	
TP_T29_MONDC0	TP_T29_MONDC0 - @mlb_lib.MLB	83D6	
TP_T29_MONDC1	TP_T29_MONDC1 - @mlb_lib.MLB	83D6	
TP_T29_MONOBSN	TP_T29_MONOBSN - @mlb_lib.MLB	83C6	
TP_T29_MONOBSP	TP_T29_MONOBSP - @mlb_lib.MLB	83D6	
TP_T29_TEST_POINT_0	TP_T29_TEST_POINT_0 - @mlb_lib.MLB	83C5	
TP_T29_TEST_POINT_1	TP_T29_TEST_POINT_1 - @mlb_lib.MLB	83C5	
TP_T29_TEST_POINT_2	TP_T29_TEST_POINT_2 - @mlb_lib.MLB	83C5	
TP_T29_THERMDP	TP_T29_THERMDP - @mlb_lib.MLB	83C5	
TP_T29_XTAL250UT	TP_T29_XTAL250UT - @mlb_lib.MLB	83C3	
TP_USB_HUB1_OCS1	TP_USB_HUB1_OCS1 - @mlb_lib.MLB	25C4	
TP_USB_HUB1_OCS4	TP_USB_HUB1_OCS4 - @mlb_lib.MLB	25C4	
TP_USB_HUB1_PRTPWR1	TP_USB_HUB1_PRTPWR1 - @mlb_lib.MLB	25C4	
TP_USB_HUB1_PRTPWR2	TP_USB_HUB1_PRTPWR2 - @mlb_lib.MLB	25C4	
TP_USB_HUB1_PRTPWR3	TP_USB_HUB1_PRTPWR3 - @mlb_lib.MLB	25C4	
TP_USB_HUB1_PRTPWR4	TP_USB_HUB1_PRTPWR4 - @mlb_lib.MLB	25C4	
TP_USB_HUB2_OCS1	TP_USB_HUB2_OCS1 - @mlb_lib.MLB	25A4	
TP_USB_HUB2_OCS4	TP_USB_HUB2_OCS4 - @mlb_lib.MLB	25A4	
TP_USB_HUB2_PRTPWR1	TP_USB_HUB2_PRTPWR1 - @mlb_lib.MLB	25A4	
TP_USB_HUB2_PRTPWR2	TP_USB_HUB2_PRTPWR2 - @mlb_lib.MLB	25A4	
TP_USB_HUB2_PRTPWR3	TP_USB_HUB2_PRTPWR3 - @mlb_lib.MLB	25A4	
TP_USB_HUB2_PRTPWR4	TP_USB_HUB2_PRTPWR4 - @mlb_lib.MLB	25A4	
U4600_ILIM	U4600_ILIM - @mlb_lib.MLB	43C7	
U4601_ILIM	U4601_ILIM - @mlb_lib.MLB	43D7	
U5900_GAIN	U5900_GAIN - @mlb_lib.MLB	56B4	
USB_BT_CONN_N	USB_BT_CONN_N - @mlb_lib.MLB	35C6	92B3 100D7
USB_BT_CONN_P	USB_BT_CONN_P - @mlb_lib.MLB	35C6	92B3 100D7
USB_BT_N	USB_BT_N - @mlb_lib.MLB	25B4	35C4 92B3
USB_BT_P	USB_BT_P - @mlb_lib.MLB	25B4	35C4 92B3
USB_B_MUXED_N	USB_B_MUXED_N - @mlb_lib.MLB	43D3	92B3
USB_B_MUXED_P	USB_B_MUXED_P - @mlb_lib.MLB	43D3	92B3
USB_DEBUGPRT_EN_L	USB_DEBUGPRT_EN_L - @mlb_lib.MLB	43C3	46B8
USB_EXTA_N	USB_EXTA_N - @mlb_lib.MLB	25A4	43A6 92C3
USB_EXTA_OC_L	USB_EXTA_OC_L - @mlb_lib.MLB	25A4	43C8
USB_EXTA_P	USB_EXTA_P - @mlb_lib.MLB	25A4	43A6 92C3
USB_EXTB_N	USB_EXTB_N - @mlb_lib.MLB	25C4	43D5 92B3
USB_EXTB_OC_L	USB_EXTB_OC_L - @mlb_lib.MLB	25C4	43D8

USB_EXTB_P	USB_EXTB_P - @mlb_lib.MLB	25C4	43D5 92B3
USB_EXTC_N	USB_EXTC_N - @mlb_lib.MLB	25C4	43C3 92B3
USB_EXTC_OC_L	USB_EXTC_OC_L - @mlb_lib.MLB	25C4	43D8
USB_EXTC_P	USB_EXTC_P - @mlb_lib.MLB	25C4	43B3 92B3
USB_EXTD_N	USB_EXTD_N - @mlb_lib.MLB	25B4	43B6 92B3
USB_EXTD_OC_L	USB_EXTD_OC_L - @mlb_lib.MLB	25A4	43B8
USB_EXTD_P	USB_EXTD_P - @mlb_lib.MLB	25A4	43B6 92B3
USB_HUB1_CFG_SEL0	USB_HUB1_CFG_SEL0 - @mlb_lib.MLB	25C6	
USB_HUB1_CFG_SEL1	USB_HUB1_CFG_SEL1 - @mlb_lib.MLB	25C6	
USB_HUB1_NONREM0	USB_HUB1_NONREM0 - @mlb_lib.MLB	25C6	
USB_HUB1_NONREM1	USB_HUB1_NONREM1 - @mlb_lib.MLB	25C6	
USB_HUB1_RBIAS	USB_HUB1_RBIAS - @mlb_lib.MLB	25C5	
USB_HUB1_TEST	USB_HUB1_TEST - @mlb_lib.MLB	25C6	
USB_HUB1_UP_N	USB_HUB1_UP_N - @mlb_lib.MLB	19D3	25C4 92C3
USB_HUB1_UP_P	USB_HUB1_UP_P - @mlb_lib.MLB	19D3	25C4 92C3
USB_HUB1_VBUS_DET	USB_HUB1_VBUS_DET - @mlb_lib.MLB	25C5	
USB_HUB1_XTAL1	USB_HUB1_XTAL1 - @mlb_lib.MLB	25C6	
USB_HUB1_XTAL2	USB_HUB1_XTAL2 - @mlb_lib.MLB	25C6	
USB_HUB2_CFG_SEL0	USB_HUB2_CFG_SEL0 - @mlb_lib.MLB	25A6	
USB_HUB2_CFG_SEL1	USB_HUB2_CFG_SEL1 - @mlb_lib.MLB	25A6	
USB_HUB2_NONREM0	USB_HUB2_NONREM0 - @mlb_lib.MLB	25A6	
USB_HUB2_NONREM1	USB_HUB2_NONREM1 - @mlb_lib.MLB	25A6	
USB_HUB2_RBIAS	USB_HUB2_RBIAS - @mlb_lib.MLB	25B6	
USB_HUB2_TEST	USB_HUB2_TEST - @mlb_lib.MLB	25B6	
USB_HUB2_UP_N	USB_HUB2_UP_N - @mlb_lib.MLB	19D3	25A4 92C3
USB_HUB2_UP_P	USB_HUB2_UP_P - @mlb_lib.MLB	19C3	25A4 92C3
USB_HUB2_VBUS_DET	USB_HUB2_VBUS_DET - @mlb_lib.MLB	25A5	
USB_HUB2_XTAL1	USB_HUB2_XTAL1 - @mlb_lib.MLB	25B6	
USB_HUB2_XTAL2	USB_HUB2_XTAL2 - @mlb_lib.MLB	25A6	
USB_HUB_RESET	USB_HUB_RESET - @mlb_lib.MLB	25B2	
USB_HUB_RESET_L	USB_HUB_RESET_L - @mlb_lib.MLB	25B1	25B6 25C6
USB_HUB_SOFT_RESET_L	USB_HUB_SOFT_RESET_L - @mlb_lib.MLB	19C1	24D4 25B2
USB_IR_N	USB_IR_N - @mlb_lib.MLB	25C4	44C3 92B3
USB_IR_P	USB_IR_P - @mlb_lib.MLB	25C4	44C3 92B3
USB_IR_R_N	USB_IR_R_N - @mlb_lib.MLB	44C4	92B3
USB_IR_R_P	USB_IR_R_P - @mlb_lib.MLB	44C4	92B3
USB_PORT0_N	USB_PORT0_N - @mlb_lib.MLB	43A4	92B3
USB_PORT0_P	USB_PORT0_P - @mlb_lib.MLB	43A4	92B3
USB_PORT1_N	USB_PORT1_N - @mlb_lib.MLB	43B5	92B3
USB_PORT1_P	USB_PORT1_P - @mlb_lib.MLB	43B5	92B3
USB_PORT2_N	USB_PORT2_N - @mlb_lib.MLB	43C2	92B3
USB_PORT2_P	USB_PORT2_P - @mlb_lib.MLB	43B2	92B3
USB_PORT3_N	USB_PORT3_N - @mlb_lib.MLB	43D2	92B3
USB_PORT3_P	USB_PORT3_P - @mlb_lib.MLB	43D2	92B3
USB_PWR_EN	USB_PWR_EN - @mlb_lib.MLB	43C8	62D1
VBIAS_DAC	VBIAS_DAC - @mlb_lib.MLB	53D5	
VCCSAS0_AGND	VCCSAS0_AGND - @mlb_lib.MLB	64B6	
VCCSAS0_BOOT_RC	VCCSAS0_BOOT_RC - @mlb_lib.MLB	64C5	
VCCSAS0_CS_N	VCCSAS0_CS_N - @mlb_lib.MLB	50A8	64B2 98D3
VCCSAS0_CS_P	VCCSAS0_CS_P - @mlb_lib.MLB	50A8	64B2 98D3
VCCSAS0_DRVH	VCCSAS0_DRVH - @mlb_lib.MLB	64C5	
VCCSAS0_DRVL	VCCSAS0_DRVL - @mlb_lib.MLB	64C5	
VCCSAS0_FB	VCCSAS0_FB - @mlb_lib.MLB	64C6	
VCCSAS0_FSEL	VCCSAS0_FSEL - @mlb_lib.MLB	64B6	
VCCSAS0_LL	VCCSAS0_LL - @mlb_lib.MLB	64C5	
VCCSAS0_OCSET	VCCSAS0_OCSET - @mlb_lib.MLB	64C6	
VCCSAS0_SET0	VCCSAS0_SET0 - @mlb_lib.MLB	64B6	
VCCSAS0_SET1	VCCSAS0_SET1 - @mlb_lib.MLB	64B6	
VCCSAS0_SNUB	VCCSAS0_SNUB - @mlb_lib.MLB	64C3	
VCCSAS0_SREF	VCCSAS0_SREF - @mlb_lib.MLB	64C6	
VCCSAS0_VBST	VCCSAS0_VBST - @mlb_lib.MLB	64C5	
VCCSAS0_VO	VCCSAS0_VO - @mlb_lib.MLB	64C6	
VCCSAVSENSE_IN	VCCSAVSENSE_IN - @mlb_lib.MLB	50A4	
VCCSA_IOUT	VCCSA_IOUT - @mlb_lib.MLB	50A7	
VCORE_GPU_IN	VCORE_GPU_IN - @mlb_lib.MLB	50A4	
VDDQ_IOUT	VDDQ_IOUT - @mlb_lib.MLB	50D6	
VDD_1V5S0	VDD_1V5S0 - @mlb_lib.MLB	71B7	
VMON_3V3_DIV	VMON_3V3_DIV - @mlb_lib.MLB	62C8	
VMON_Q2_BASE	VMON_Q2_BASE - @mlb_lib.MLB	62C7	
VMON_Q3_BASE	VMON_Q3_BASE - @mlb_lib.MLB	62C7	
VMON_Q4_BASE	VMON_Q4_BASE - @mlb_lib.MLB	62B7	
VR3V3_G3H_BST	VR3V3_G3H_BST - @mlb_lib.MLB	65D5	
VR3V3_G3H_EN	VR3V3_G3H_EN - @mlb_lib.MLB	65D6	
VR3V3_G3H_ENL	VR3V3_G3H_ENL - @mlb_lib.MLB	65C5	
VR3

XDP_CPU_PREQ_L	XDP_CPU_PREQ_L - @mlb_lib.MLB	11C2 24D7 90D1
XDP_CPU_PWRBTN_L	XDP_CPU_PWRBTN_L - @mlb_lib.MLB	24C7 90C1
XDP_CPU_PWRGD	XDP_CPU_PWRGD - @mlb_lib.MLB	24C7 90C1
XDP_CPU_TCK	XDP_CPU_TCK - @mlb_lib.MLB	11C2 24A8 24C7 24D2 90D1
XDP_CPU_TDI	XDP_CPU_TDI - @mlb_lib.MLB	11C2 24B6 24D2 90D1
XDP_CPU_TDO	XDP_CPU_TDO - @mlb_lib.MLB	11C2 24A6 24D2 90D1
XDP_CPU_TMS	XDP_CPU_TMS - @mlb_lib.MLB	11C2 24A6 24D2 90D1
XDP_CPU_TRST_L	XDP_CPU_TRST_L - @mlb_lib.MLB	11C2 24C4 24D2 90D1
XDP_DBRESET_L	XDP_DBRESET_L - @mlb_lib.MLB	11C2 24C4 27A4 90C1
XDP_PCH_TCK	XDP_PCH_TCK - @mlb_lib.MLB	17C8 24A4 24A8 24C7 90D1
XDP_PCH_TDI	XDP_PCH_TDI - @mlb_lib.MLB	17C8 24A4 24B6 90D1
XDP_PCH_TDO	XDP_PCH_TDO - @mlb_lib.MLB	17C8 24A4 24B6 90D1
XDP_PCH_TMS	XDP_PCH_TMS - @mlb_lib.MLB	17C8 24A4 24B6 90D1
XDP_PRESENT_L	XDP_PRESENT_L - @mlb_lib.MLB	24B2 24C4 90C1
XDP_RES_RL	XDP_RES_RL - @mlb_lib.MLB	24C2 90C1
XDP_SEL	XDP_SEL - @mlb_lib.MLB	24A8 24B1 24B8
XDP_TDI	XDP_TDI - @mlb_lib.MLB	24B8 24C4 90D1
XDP_TDO	XDP_TDO - @mlb_lib.MLB	24A8 24C4 90D1
XDP_TMS	XDP_TMS - @mlb_lib.MLB	24A4 24C4 90D1
XDP_VR_READY	XDP_VR_READY - @mlb_lib.MLB	24C7 90C1

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Design: mlb
Date: Apr 7 20:19:40 2011

C81A0	CAP_402	mlb[74A4]
C81A1	CAP_402	mlb[74A3]
C81A2	CAP_402	mlb[74A3]
C81A3	CAP_402	mlb[74A3]
C81A4	CAP_402	mlb[74A3]
C81A5	CAP_402	mlb[74A2]
C81A6	CAP_402	mlb[74A2]
C81A7	CAP_402	mlb[74A2]
C81A8	CAP_402	mlb[74A2]
C81A9	CAP_402	mlb[74A1]
C81B0	CAP_603	mlb[74A4]
C81B1	CAP_603	mlb[74A3]
C81B2	CAP_603	mlb[74A3]
C81C0	CAP_402	mlb[74D3]
C81C1	CAP_201	mlb[74D2]
C160X	CAP_402-1	mlb[15B2]
C160Y	CAP_402-1	mlb[15B2]
C160Z	CAP_P_CASE-B4-SM	mlb[15B2]
C161A	CAP_402-1	mlb[15B5]
C161B	CAP_402-1	mlb[15B4]
C161C	CAP_402-1	mlb[15B4]
C161D	CAP_402-1	mlb[15B4]
C161E	CAP_603	mlb[15A7]
C161F	CAP_0402-1	mlb[15A7]
C162A	CAP_0402-1	mlb[15A7]
C162B	CAP_0402-1	mlb[15A6]
C162C	CAP_0402-1	mlb[15A6]
C162D	CAP_0402-1	mlb[15A6]
C162E	CAP_0402-1	mlb[15A6]
C167A	CAP_0402-1	mlb[15A5]
C167B	CAP_0402-1	mlb[15A5]
C167C	CAP_0402-1	mlb[15A5]
C167F	CAP_402-1	mlb[15A7]
C169A	CAP_402-1	mlb[15B6]
C169B	CAP_402-1	mlb[15B6]
C169C	CAP_402-1	mlb[15B6]
C169D	CAP_402-1	mlb[15B6]
C169E	CAP_402-1	mlb[15B5]
C169F	CAP_402-1	mlb[15B5]
C1330	CAP_402	mlb[13B1]
C1600	CAP_402-LF	mlb[15D7]
C1601	CAP_402-LF	mlb[15D7]
C1602	CAP_402-LF	mlb[15D7]
C1603	CAP_402-LF	mlb[15D6]
C1604	CAP_402-LF	mlb[15D6]
C1605	CAP_402-LF	mlb[15D6]
C1606	CAP_402-LF	mlb[15D6]
C1607	CAP_402-LF	mlb[15D5]
C1608	CAP_402-LF	mlb[15D5]
C1609	CAP_402-LF	mlb[15D5]
C1610	CAP_402-LF	mlb[15D5]
C1611	CAP_402-LF	mlb[15D4]
C1612	CAP_402-LF	mlb[15D4]
C1613	CAP_402-LF	mlb[15D4]
C1614	CAP_402-LF	mlb[15D4]
C1615	CAP_402-LF	mlb[15D3]
C1616	CAP_402-LF	mlb[15D3]
C1617	CAP_402-LF	mlb[15D3]
C1618	CAP_402-LF	mlb[15D2]
C1619	CAP_402-LF	mlb[15D2]
C1620	CAP_402-LF	mlb[15D2]
C1621	CAP_402-LF	mlb[15D2]
C1622	CAP_402-LF	mlb[15D1]
C1623	CAP_402-LF	mlb[15D1]
C1624	CAP_402-LF	mlb[15D1]
C1625	CAP_402-LF	mlb[15D7]
C1626	CAP_402-LF	mlb[15D7]
C1627	CAP_402-LF	mlb[15D7]
C1628	CAP_402-LF	mlb[15D6]
C1629	CAP_402-LF	mlb[15D6]
C1630	CAP_402-LF	mlb[15D6]
C1631	CAP_402-LF	mlb[15D6]
C1632	CAP_402-LF	mlb[15D5]
C1633	CAP_402-LF	mlb[15D5]
C1634	CAP_402-LF	mlb[15D5]
C1635	CAP_402-LF	mlb[15D5]
C1636	CAP_402-LF	mlb[15D4]
C1637	CAP_402-LF	mlb[15D4]
C1638	CAP_402-LF	mlb[15D4]
C1639	CAP_402-LF	mlb[15D4]
C1640	CAP_402-LF	mlb[15D3]
C1641	CAP_402-LF	mlb[15D3]
C1642	CAP_402-LF	mlb[15D3]
C1643	CAP_402-LF	mlb[15D2]
C1644	CAP_402-LF	mlb[15D2]
C1645	CAP_402-LF	mlb[15D2]
C1646	CAP_402-LF	mlb[15D2]
C1647	CAP_402-LF	mlb[15D1]
C1648	CAP_402-LF	mlb[15D1]
C1649	CAP_402-LF	mlb[15D1]
C1650	CAP_402-LF	mlb[15D7]
C1651	CAP_402-LF	mlb[15D7]
C1652	CAP_402-LF	mlb[15D7]
C1653	CAP_402-LF	mlb[15D6]
C1654	CAP_402-LF	mlb[15D6]
C1655	CAP_0603	mlb[15C7]
C1656	CAP_0603	mlb[15C7]
C1657	CAP_0603	mlb[15C7]
C1658	CAP_0603	mlb[15C6]
C1659	CAP_0603	mlb[15C6]
C1660	CAP_0603	mlb[15C6]
C1661	CAP_0603	mlb[15C5]
C1662	CAP_0603	mlb[15C5]
C1663	CAP_0603	mlb[15C5]
C1664	CAP_0603	mlb[15C5]
C1665	CAP_0603	mlb[15C4]
C1666	CAP_0603	mlb[15C4]
C1667	CAP_0603	mlb[15C7]
C1668	CAP_0603	mlb[15C7]
C1669	CAP_0603	mlb[15C7]
C1670	CAP_0603	mlb[15C6]
C1671	CAP_0603	mlb[15C6]
C1672	CAP_0603	mlb[15C6]
C1673	CAP_0603	mlb[15C5]
C1674	CAP_0603	mlb[15C5]
C1675	CAP_0603	mlb[15C5]
C1676	CAP_0603	mlb[15C5]
C1677	CAP_0603	mlb[15C4]
C1678	CAP_0603	mlb[15C4]
C1679	CAP_0603	mlb[15C4]
C1684	CAP_402-1	mlb[15B7]
C1685	CAP_402-1	mlb[15B7]
C1686	CAP_402-1	mlb[15B7]
C1687	CAP_402-1	mlb[15B6]
C1688	CAP_402-1	mlb[15B6]
C1689	CAP_402-1	mlb[15B6]
C1690	CAP_402-1	mlb[15B5]
C1691	CAP_402-1	mlb[15B5]
C1692	CAP_402-1	mlb[15B5]
C1693	CAP_402-1	mlb[15B5]
C1694	CAP_402-1	mlb[15B4]
C1695	CAP_402-1	mlb[15B4]
C1696	CAP_402-1	mlb[15B4]
C1697	CAP_402-1	mlb[15B7]
C1698	CAP_402-1	mlb[15B7]
C1699	CAP_402-1	mlb[15B7]
C1700	CAP_402-1	mlb[16D7]
C1701	CAP_402-1	mlb[16D7]
C1702	CAP_402-1	mlb[16D6]
C1703	CAP_402-1	mlb[16D6]
C1704	CAP_402-1	mlb[16D6]
C1705	CAP_402-1	mlb[16D5]
C1706	CAP_402-1	mlb[16D5]
C1707	CAP_402-1	mlb[16D5]
C1708	CAP_402-1	mlb[16D4]
C1709	CAP_402-1	mlb[16D4]
C1710	CAP_402-1	mlb[16D4]
C1711	CAP_0402-1	mlb[16D7]
C1712	CAP_0402-1	mlb[16D7]
C1713	CAP_0402-1	mlb[16D6]
C1714	CAP_0402-1	mlb[16D6]
C1715	CAP_0402-1	mlb[16D6]
C1716	CAP_0402-1	mlb[16D5]
C1717	CAP_0603	mlb[16C7]
C1718	CAP_0603	mlb[16C7]
C1719	CAP_0603	mlb[16C6]
C1720	CAP_0603	mlb[16C6]
C1721	CAP_0603	mlb[16C6]
C1722	CAP_0603	mlb[16C5]
C1738	CAP_402-1	mlb[16B7]
C1739	CAP_402-1	mlb[16B7]
C1740	CAP_402-1	mlb[16B6]
C1741	CAP_402-1	mlb[16B6]
C1742	CAP_402-1	mlb[16B6]
C1743	CAP_402-1	mlb[16B5]
C1744	CAP_402-1	mlb[16B5]
C1745	CAP_402-1	mlb[16B5]
C1746	CAP_402-1	mlb[16B4]
C1747	CAP_402-1	mlb[16B4]
C1748	CAP_0402-1	mlb[16B7]
C1749	CAP_0402-1	mlb[16B7]
C1750	CAP_603	mlb[16B6]
C1751	CAP_0402-1	mlb[16B6]
C1752	CAP_0402-1	mlb[16B6]
C1753	CAP_0402-1	mlb[16B5]
C1754	CAP_603	mlb[16B5]
C1755	CAP_0402-1	mlb[16B5]
C1756	CAP_P_CASE-B4-SM	mlb[16B7]
C1757	CAP_402-1	mlb[16A6]
C1758	CAP_402-1	mlb[16B3]
C1759	CAP_402-1	mlb[16B3]
C1760	CAP_402-1	mlb[16B2]
C1761	CAP_402-1	mlb[16B2]
C1762	CAP_402-1	mlb[16B2]
C1763	CAP_0402-1	mlb[16B3]
C1764	CAP_0402-1	mlb[16B3]
C1765	CAP_0402-1	mlb[16B2]
C1766	CAP_0402-1	mlb[16B2]
C1767	CAP_0402-1	mlb[16B2]
C1768	CAP_P_CASE-B4-SM	mlb[16B3]
C1802	CAP_402-1	mlb[17A7]
C1803	CAP_402-1	mlb[17A7]
C2150	CAP_402	mlb[20C2]
C2151	CAP_402	mlb[20C2]
C2152	CAP_402	mlb[20B2]
C2210	CAP_402	mlb[21B8]
C2222	CAP_402	mlb[21B8]
C2231	CAP_402-1	mlb[21B7]
C2232	CAP_402	mlb[21B7]
C2233	CAP_402	mlb[21B7]
C2401	CAP_603	mlb[23B1]
C2407	CAP_402-1	mlb[23B2]
C2411	CAP_402	mlb[23D6]
C2413	CAP_402	mlb[23D4]
C2414	CAP_402-1	mlb[23B2]
C2416	CAP_402	mlb[23D5]
C2417	CAP_402	mlb[23D4]
C2419	CAP_402-1	mlb[23C5]
C2420	CAP_0603	mlb[23B1]
C2421	CAP_402	mlb[23A7]
C2423	CAP_402	mlb[23A6]
C2424	CAP_402	mlb[23A7]
C2426	CAP_402-1	mlb[23B2]
C2428	CAP_0603	mlb[23B1]
C2429	CAP_402-1	mlb[23B2]
C2430	CAP_402	mlb[23D4]
C2434	CAP_402-1	mlb[23C2]
C2438	CAP_402	mlb[23B7]
C2439	CAP_402-1	mlb[23B7]
C2440	CAP_402	mlb[23D3]
C2441	CAP_402	mlb[23D3]
C2442	CAP_402-1	mlb[23C3]
C2444	CAP_402-1	mlb[23D2]
C2446	CAP_402-1	mlb[23D1]
C2450	CAP_603	mlb[23C7]
C2451	CAP_402	mlb[23C7]
C2452	CAP_402-1	mlb[23D2]
C2453	CAP_603	mlb[23C4]
C2454	CAP_402-1	mlb[23C3]
C2455	CAP_402	mlb[23C7]
C2456	CAP_402-1	mlb[23B2]
C2460	CAP_603	mlb[23C1]
C2463	CAP_402-1	mlb[23B1]
C2469	CAP_402-1	mlb[23C1]
C2475	CAP_402-1	mlb[23D2]
C2476	CAP_402-1	mlb[23D1]
C2481	CAP_402-1	mlb[23C2]
C2482	CAP_402-1	mlb[23C2]
C2483	CAP_402-1	mlb[23C2]
C2484	CAP_402	mlb[23D5]
C2485	CAP_402	mlb[23A6]
C2486	CAP_402	mlb[23A6]
C2491	CAP_P_CASE-B2-SM1	mlb[23B4]
C2492	CAP_402-1	mlb[23B4]
C2493	CAP_P_CASE-B2-SM1	mlb[23A4]
C2494	CAP_402-1	mlb[23A4]
C2496	CAP_402-1	mlb[23B2]
C2499	CAP_402	mlb[23C3]
C2500	CAP_402	mlb[24C6]
C2501	CAP_402	mlb[24C5]
C2557	CAP_402	mlb[24B3]
C2602	CAP_603	mlb[25D7]
C2603	CAP_402	mlb[25D6]
C2607	CAP_603	mlb[25D7]
C2608	CAP_402	mlb[25D6]
C2609	CAP_402	mlb[25D6]
C2610	CAP_402	mlb[25D6]
C2611	CAP_402	mlb[25D6]
C2612	CAP_402	mlb[25D6]
C2615	CAP_402	mlb[25D4]
C2616	CAP_402	mlb[25D4]
C2617	CAP_402	mlb[25D4]
C2618	CAP_402	mlb[25D4]
C2619	CAP_402	mlb[25D7]
C2620	CAP_402	mlb[25D7]
C2640	CAP_402	mlb[25B2]
C2641	CAP_402	mlb[25B2]
C2652	CAP_603	mlb[25B7]
C2653	CAP_402	mlb[25B7]
C2657	CAP_603	mlb[25B7]
C2658	CAP_402	mlb[25B6]
C2659	CAP_402	mlb[25B6]
C2660	CAP_402	mlb[25B6]
C2661	CAP_402	mlb[25B6]
C2662	CAP_402	mlb[25B6]
C2665	CAP_402	mlb[25B4]
C2666	CAP_402	mlb[25B4]
C2667	CAP_402	mlb[25B4]
C2668	CAP_402	mlb[25B4]
C2669	CAP_402	mlb[25B7]
C2670	CAP_402	mlb[25B7]
C2702	CAP_402-1	mlb[26D6]
C2705	CAP_402	mlb[26C7]
C2706	CAP_402	mlb[26C7]
C2720	CAP_402	mlb[26D6]
C2722	CAP_402	mlb[26D6]
C2724	CAP_402	mlb[26D6]
C2810	CAP_402	mlb[27C6]
C2811	CAP_402	mlb[27C6]
C2840	CAP_402	mlb[27C3]
C2850	CAP_402	mlb[27A7]
C2860	CAP_402	mlb[27A6]
C2880	CAP_402	mlb[27B3]
C2916	CAP_402	mlb[28B5]
C2920	CAP_402	mlb[28C3]
C2951	CAP_402	mlb[28B3]
C3100	CAP_603	mlb[30D3]
C3101	CAP_603	mlb[30D3]
C3110	CAP_402	mlb[30D3]
C3111	CAP_402	mlb[30D3]
C3112	CAP_402	mlb[30D2]
C3113	CAP_402	mlb[30D2]
C3114	CAP_402	mlb[30D2]
C3115	CAP_402	mlb[30D1]
C3116	CAP_402	mlb[30D1]
C3117	CAP_402	mlb[30D1]
C3130	CAP_402-LF	mlb[30D1]
C3131	CAP_402	mlb[30D1]
C3132	CAP_402	mlb[30D1]
C3135	CAP_402-LF	mlb[30C1]
C3136	CAP_402	mlb[30C1]
C3137	CAP_402	mlb[30C1]
C3140	CAP_402-LF	mlb[30B2]
C3150	CAP_402-LF	mlb[30C1]
C3151	CAP_402-LF	mlb[30C1]
C3152	CAP_402	mlb[30C1]
C3200	CAP_603	mlb[31D3]
C3201	CAP_603	mlb[31D3]
C3210	CAP_402	mlb[31D3]
C3211	CAP_402	mlb[31D3]
C3212	CAP_402	mlb[31D2]
C3213	CAP_402	mlb[31D2]
C3214	CAP_402	mlb[31D2]
C3215	CAP_402	mlb[31D1]
C3216	CAP_402	mlb[31D1]
C3217	CAP_402	mlb[31D1]
C3222	CAP_402	mlb[31A4]
C3224	CAP_402	mlb[31A4]
C3226	CAP_402	mlb[31A3]
C3228	CAP_402	mlb[31A2]
C3230	CAP_402-LF	mlb[31D1]
C3231	CAP_402	mlb[31D1]
C3232	CAP_402	mlb[31D1]
C3235	CAP_402-LF	mlb[31C1]
C3236	CAP_402	mlb[31C1]
C3237	CAP_402	mlb[31C1]
C3240	CAP_402-LF	mlb[31B2]
C3250	CAP_402-LF	mlb[31C1]
C3251	CAP_402-LF	mlb[31C1]
C3252	CAP_402	mlb[31C1]
C3331	CAP_402	mlb[32B5]
C3332	CAP_402	mlb[32B4]
C3333	CAP_402	mlb[32B4]
C3334	CAP_402	mlb[32B4]
C3336	CAP_402	mlb[32B3]
C3338	CAP_402	mlb[32A5]
C3339	CAP_402	mlb[32A5]
C3340	CAP_402	mlb[32A4]
C3341	CAP_402	mlb[32A4]
C3342	CAP_402	mlb[32A4]
C3400	CAP_402-LF	mlb[33D6]
C3401	CAP_402	mlb[33D6]
C3402	CAP_402	mlb[33C6]
C3403	CAP_402	mlb[33D4]
C3404	CAP_402	mlb[33C4]
C3405	CAP_402	mlb[33B4]
C3500	CAP_402	mlb[34D4]
C3501	CAP_603	mlb[34D4]
C3505	CAP_402	mlb[34D2]
C3507	CAP_603	mlb[34D3]
C3511	CAP_402	mlb[34D8]
C3512	CAP_402	mlb[34D8]
C3513	CAP_402	mlb[34D8]
C3514	CAP_402	mlb[34D8]
C3515	CAP_402	mlb[34C8]
C3516	CAP_402	mlb[34C8]
C3517	CAP_402	mlb[34C8]
C3518	CAP_402	mlb[34C8]
C3519	CAP_402	mlb[34C8]
C3520	CAP_402	mlb[34C8]
C3521	CAP_402	mlb[34C8]
C3530	CAP_402-1	mlb[34B4]
C3535	CAP_402-1	mlb[34B4]
C3541	CAP_402	mlb[34C6]
C3542	CAP_402	mlb[34C7]
C3550	CAP_402	mlb[34C3]
C3551	CAP_402	mlb[34C4]
C3620	CAP_0805	mlb[35B5]
C3621	CAP_402	mlb[35B5]
C3622	CAP_402	mlb[35B7]
C3623	CAP_402	mlb[35B6]
C3624	CAP_402-1	mlb[35B6]
C3630	CAP_402	mlb[35C5]
C3631	CAP_402	mlb[35C5]
C3632	CAP_402	mlb[35C6]
C3633	CAP_402-1	mlb[35C6]
C3640	CAP_402	mlb[35B3]
C3650	CAP_402	mlb[35C3]
C3651	CAP_402	mlb[35C2]
C3800	CAP_402	mlb[36D5]
C3801	CAP_402	mlb[36D4]
C3802	CAP_402	mlb[36D4]
C3803	CAP_402	mlb[36D4]
C3810	CAP_1206	mlb[36B3]
C3900	CAP_402	mlb[37D6]
C3905	CAP_402	mlb[37D6]
C3910	CAP_402	mlb[37C6]
C3911	CAP_402	mlb[37C5]
C3915	CAP_603	mlb[37C5]
C3916	CAP_402	mlb[37C5]
C3920	CAP_603	mlb[37D3]
C3921	CAP_402	mlb[37D4]
C3925	CAP_603	mlb[37D3]
C3926	CAP_402	mlb[37D4]
C3930	CAP_603	mlb[37C3]
C3931	CAP_402	mlb[37C4]
C3935	CAP_0805	mlb[37C3]
C3936	CAP_402	mlb[37C3]
C3950	CAP_402	mlb[37C7]
C3951	CAP_402	mlb[37C7]
C3955	CAP_402	mlb[37C7]
C3956	CAP_402	mlb[37B7]
C3970	CAP_603	mlb[37C2]
C3971	CAP_402	mlb[37C2]
C3972	CAP_402	mlb[37C2]
C3990	CAP_402	mlb[37A7]
C4020	CAP_603	mlb[38D7]
C4021	CAP_402	mlb[38D7]
C4025	CAP_603	mlb[38C6]
C4026	CAP_402	mlb[38C6]
C4100	CAP_402-1	mlb[39D7]
C4101	CAP_402-1	mlb[39D7]
C4102	CAP_402-1	mlb[39D6]
C4103	CAP_402-1	mlb[39D6]
C4104	CAP_402-1	mlb[39D6]
C4105	CAP_402-1	mlb[39D6]
C4106	CAP_402-1	mlb[39D6]
C4107	CAP_402-1	mlb[39D6]
C4108	CAP_402-1	mlb[39D6]
C4110	CAP_402-1	mlb[39D7]
C4111	CAP_402-1	mlb[39D7]
C4112	CAP_402-1	mlb[39D6]
C4113	CAP_402-1	mlb[39D6]
C4114	CAP_402-1	mlb[39D6]
C4115	CAP_402-1	mlb[39D6]
C4117	CAP_402-1	mlb[39C6]
C4118	CAP_402-1	mlb[39C6]
C4119	CAP_402-1	mlb[39C6]
C4120	CAP_402-1	mlb[39D2]
C4121	CAP_402-1	mlb[39D3]
C4122	CAP_402-1	mlb[39D3]
C4123	CAP_402-1	mlb[39D3]
C4124	CAP_402-1	mlb[39D3]
C4125	CAP_402-1	mlb[39D2]
C4126	CAP_402-1	mlb[39D3]
C4127	CAP_402-1	mlb[39D3]
C4128	CAP_402-1	mlb[39D3]
C4130	CAP_402-1	mlb[39D2]
C4131	CAP_402-1	mlb[39D2]
C4132	CAP_402-1	mlb[39D2]
C4135	CAP_402-1	mlb[39C2]
C4137	CAP_402-1	mlb[39C3]
C4138	CAP_402-1	mlb[39C3]
C4139	CAP_402-1	mlb[39C2]
C4140	CAP_402	mlb[39C7]
C4141	CAP_402	mlb[39C7]
C4145	CAP_402	mlb[39C7]
C4146	CAP_402	mlb[39C7]
C4189	CAP_402	mlb[39A2]
C4190	CAP_402	mlb[39C1]
C4200	CAP_402-1	mlb[40D7]
C4201	CAP_402	mlb[40D6]
C4202	CAP_402-LF	mlb[40D6]
C4250	CAP_402-1	mlb[40D3]
C4254	CAP_402	mlb[40B3]
C4300	CAP_603	mlb[41D2]
C4305	CAP_603	mlb[41B6]
C4309	CAP_402	mlb[41C7]
C4310	CAP_402	mlb[41C4]
C4311	CAP_402	mlb[41C3]
C4312	CAP_402	mlb[41B4]
C4313	CAP_402	mlb[41B3]
C4332	CAP_402	mlb[41B1]
C4335	CAP_603-1	mlb[41B2]
C4350	CAP_402	mlb[41A4]
C4351	CAP_402	mlb[41A5]
C4355	CAP_603	mlb[41A3]
C4400	CAP_402	mlb[42C6]
C4401	CAP_402	mlb[42C6]
C4402	CAP_402	mlb[42B6]
C4403	CAP_402	mlb[42B6]
C4420	CAP_402	mlb[42C2]
C4421	CAP_402	mlb[42C2]
C4422	CAP_402	mlb[42B2]
C4423	CAP_402	mlb[42B2]
C4431	CAP_402	mlb[42D6]
C4441	CAP_402	mlb[42D2]
C4450	CAP_0201	mlb[42C6]
C4451	CAP_0201	mlb[42C6]
C4452	CAP_0201	mlb[42B6]
C4453	CAP_0201	mlb[42B6]

C4460	CAP_0201	mlb[42C3]
C4461	CAP_0201	mlb[42C3]
C4462	CAP_0201	mlb[42B3]
C4463	CAP_0201	mlb[42B3]
C4600	CAP_P_CASE-B2-SM	mlb[43B7]
C4601	CAP_402	mlb[43B8]
C4603	CAP_402	mlb[43D6]
C4604	CAP_402	mlb[43D8]
C4605	CAP_402	mlb[43D2]
C4606	CAP_P_CASE-B2-SM	mlb[43D8]
C4612	CAP_402	mlb[43D6]
C4615	CAP_402	mlb[43C2]
C4623	CAP_402	mlb[43B6]
C4625	CAP_402	mlb[43B4]
C4632	CAP_402	mlb[43B6]
C4635	CAP_402	mlb[43A4]
C4650	CAP_402	mlb[43D5]
C4790	CAP_402-1	mlb[44C4]
C4791	CAP_402	mlb[44C4]
C4792	CAP_402	mlb[44C5]
C4793	CAP_402-1	mlb[44B4]
C4794	CAP_402	mlb[44B5]
C4800	CAP_402	mlb[45C3]
C4801	CAP_402	mlb[45D6]
C4802	CAP_402	mlb[45A3]
C4803	CAP_402	mlb[45C2]
C4806	CAP_402	mlb[45C6]
C4809	CAP_402	mlb[45C4]
C4902	CAP_805	mlb[46D4]
C4903	CAP_402	mlb[46D4]
C4904	CAP_402	mlb[46D3]
C4905	CAP_402	mlb[46D3]
C4906	CAP_402	mlb[46D3]
C4907	CAP_402	mlb[46D2]
C4910	CAP_402	mlb[46A5]
C4920	CAP_402	mlb[46D3]
C5001	CAP_402	mlb[47D8]
C5010	CAP_402	mlb[47B7]
C5011	CAP_402	mlb[47B7]
C5020	CAP_402	mlb[47D7]
C5025	CAP_603	mlb[47D7]
C5026	CAP_402	mlb[47D6]
C5050	CAP_402	mlb[47B5]
C5051	CAP_402	mlb[47A4]
C5300	CAP_402	mlb[50D6]
C5301	CAP_402	mlb[50D5]
C5305	CAP_402	mlb[50C6]
C5306	CAP_402	mlb[50C5]
C5320	CAP_402	mlb[50C2]
C5322	CAP_402	mlb[50A3]
C5330	CAP_402	mlb[50B2]
C5333	CAP_402	mlb[50A3]
C5340	CAP_402	mlb[50D2]
C5341	CAP_402	mlb[50D2]
C5345	CAP_402	mlb[50D3]
C5351	CAP_402	mlb[50B2]
C5355	CAP_402	mlb[50B3]
C5360	CAP_402	mlb[50B7]
C5361	CAP_402	mlb[50B6]
C5365	CAP_402	mlb[50B7]
C5366	CAP_402	mlb[50A6]
C5370	CAP_402	mlb[50A7]
C5371	CAP_402	mlb[50A6]
C5375	CAP_402	mlb[50C7]
C5376	CAP_402	mlb[50C6]
C5401	CAP_402	mlb[51C6]
C5403	CAP_402	mlb[51C5]
C5414	CAP_402	mlb[51C2]
C5418	CAP_402	mlb[51D6]
C5421	CAP_402	mlb[51B6]
C5423	CAP_402	mlb[51A5]
C5437	CAP_402	mlb[51D5]
C5500	CAP_402-1	mlb[52D6]
C5510	CAP_402	mlb[52D3]
C5520	CAP_402	mlb[52D3]
C5530	CAP_402	mlb[52B6]
C5535	CAP_402-1	mlb[52B5]
C5540	CAP_402	mlb[52A6]
C5570	CAP_402	mlb[52C3]
C5580	CAP_402	mlb[52C3]
C5600	CAP_0306	mlb[53D6]
C5602	CAP_P_2012-LLP	mlb[53D5]
C5603	CAP_402	mlb[53D4]
C5604	CAP_P_2012-LLP	mlb[53D4]
C5605	CAP_402	mlb[53D3]
C5606	CAP_402-1	mlb[53D3]
C5608	CAP_0508	mlb[53D3]
C5613	CAP_P_CASE-P3-HF	mlb[53B4]
C5614	CAP_P_CASE-B2-SM	mlb[53B4]
C5650	CAP_402	mlb[53A7]
C5651	CAP_402-1	mlb[53A6]
C5652	CAP_402	mlb[53A6]
C5653	CAP_402	mlb[53A4]
C5654	CAP_402-1	mlb[53A4]
C5700	CAP_P_CASE-M	mlb[54D4]
C5702	CAP_P_CASE-M	mlb[54C4]
C5703	CAP_P_CASE-M	mlb[54C4]
C5713	CAP_201	mlb[54C5]
C5800	CAP_0508	mlb[55D5]
C5801	CAP_402	mlb[55D5]
C5804	CAP_402-1	mlb[55B4]
C5805	CAP_402-1	mlb[55B3]
C5806	CAP_402-1	mlb[55B3]
C5812	CAP_P_CASE-P	mlb[55C7]
C5813	CAP_P_CASE-P	mlb[55C7]
C5814	CAP_P_CASE-P	mlb[55B7]
C5815	CAP_P_CASE-P	mlb[55B7]
C5901	CAP_P_1206-LLP	mlb[56C3]
C5902	CAP_402	mlb[56C3]
C5904	CAP_402-1	mlb[56C5]
C5950	CAP_402	mlb[56B6]
C5951	CAP_402	mlb[56C6]
C6000	CAP_402-1	mlb[57A8]
C6050	CAP_402-1	mlb[57A8]
C6051	CAP_402	mlb[57A7]
C6054	CAP_402	mlb[57A6]
C6100	CAP_402	mlb[58A3]
C6101	CAP_402	mlb[58B7]
C6102	CAP_402	mlb[58B7]
C6111	CAP_402	mlb[58A6]
C6160	CAP_402	mlb[58A3]
C6180	CAP_603	mlb[58D3]
C6181	CAP_402	mlb[58C2]
C6182	CAP_P_603-HF	mlb[58C2]
C6183	CAP_402	mlb[58C3]
C6184	CAP_402	mlb[58C3]
C6185	CAP_402	mlb[58C2]
C6186	CAP_402	mlb[58C3]
C6187	CAP_402	mlb[58D3]
C6400	CAP_402	mlb[59C5]
C6500	CAP_402	mlb[60C4]
C6502	CAP_402	mlb[60D5]
C6503	CAP_402	mlb[60C4]
C6505	CAP_603	mlb[60C4]
C6506	CAP_603	mlb[60C3]
C6507	CAP_402	mlb[60C3]
C6520	CAP_402	mlb[60C4]
C6700	CAP_402	mlb[61D2]
C6701	CAP_402	mlb[61B7]
C6702	CAP_603	mlb[61B7]
C6709	CAP_402	mlb[61D3]
C6710	CAP_402	mlb[61D6]
C6711	CAP_402	mlb[61D6]
C6730	CAP_402	mlb[61C2]
C6731	CAP_402	mlb[61C3]
C6740	CAP_402	mlb[61B2]
C6741	CAP_402	mlb[61C3]
C6760	CAP_402	mlb[61B2]
C6761	CAP_402	mlb[61B3]
C6810	CAP_402	mlb[62D2]
C6812	CAP_402	mlb[62D3]
C6821	CAP_402	mlb[62B2]
C6822	CAP_402	mlb[62B1]
C6842	CAP_402	mlb[62D7]
C6860	CAP_402	mlb[62A7]
C6881	CAP_402	mlb[62C3]
C6886	CAP_402	mlb[62C2]
C6887	CAP_402	mlb[62C3]
C6888	CAP_402	mlb[62C2]
C7101	CAP_603	mlb[64C5]
C7102	CAP_402	mlb[64B6]
C7103	CAP_402	mlb[64B6]
C7105	CAP_402	mlb[64B7]
C7119	CAP_402	mlb[64B3]
C7120	CAP_P_SM	mlb[64C3]
C7121	CAP_402	mlb[64C3]
C7122	CAP_402	mlb[64C3]
C7123	CAP_402	mlb[64B2]
C7130	CAP_402	mlb[64C4]
C7140	CAP_402	mlb[64B3]
C7201	CAP_402	mlb[65D5]
C7202	CAP_402	mlb[65D6]
C7203	CAP_402	mlb[65C5]
C7204	CAP_402	mlb[65D4]
C7205	CAP_P_CASED2-SM	mlb[65D4]
C7208	CAP_402	mlb[65C4]
C7209	CAP_805	mlb[65C3]
C7210	CAP_805	mlb[65C3]
C7211	CAP_402	mlb[65D6]
C7212	CAP_402	mlb[65C3]
C7213	CAP_402	mlb[65D5]
C7250	CAP_402	mlb[65B6]
C7251	CAP_P_SM	mlb[65B7]
C7252	CAP_603	mlb[65B7]
C7253	CAP_402	mlb[65B7]
C7254	CAP_402	mlb[65B5]
C7255	CAP_402	mlb[65A6]
C7256	CAP_402	mlb[65B4]
C7257	CAP_402	mlb[65A5]
C7258	CAP_402	mlb[65A5]
C7259	CAP_402	mlb[65A4]
C7260	CAP_402	mlb[65A3]
C7261	CAP_0805	mlb[65A3]
C7262	CAP_P_CASE-B2-SM	mlb[65A3]
C7300	CAP_603	mlb[66C7]
C7301	CAP_402	mlb[66D6]
C7302	CAP_603	mlb[66D5]
C7305	CAP_402	mlb[66B8]
C7320	CAP_402	mlb[66B7]
C7321	CAP_402	mlb[66B4]
C7325	CAP_402	mlb[66C4]
C7330	CAP_P_SM	mlb[66C5]
C7331	CAP_603	mlb[66C4]
C7332	CAP_P_SM	mlb[66C4]
C7333	CAP_402	mlb[66C4]
C7340	CAP_P_CASE-B2-SM	mlb[66C3]
C7341	CAP_P_CASE-B2-SM	mlb[66C2]
C7345	CAP_603	mlb[66C2]
C7350	CAP_402	mlb[66B6]
C7355	CAP_603	mlb[66C6]
C7360	CAP_0603	mlb[66B5]
C7361	CAP_0603	mlb[66B5]
C7398	CAP_402	mlb[66C3]
C7399	CAP_402	mlb[66C3]
C7400	CAP_402	mlb[67C2]
C7401	CAP_402	mlb[67C2]
C7402	CAP_402	mlb[67C2]
C7403	CAP_402	mlb[67C2]
C7404	CAP_402	mlb[67C2]
C7405	CAP_402	mlb[67B2]
C7406	CAP_402	mlb[67C2]
C7409	CAP_402	mlb[67C4]
C7411	CAP_402	mlb[67A2]
C7412	CAP_402	mlb[67B2]
C7413	CAP_402	mlb[67D5]
C7414	CAP_603	mlb[67C3]
C7416	CAP_402	mlb[67D7]
C7417	CAP_402	mlb[67C7]
C7418	CAP_402	mlb[67C7]
C7419	CAP_402	mlb[67C8]
C7420	CAP_402	mlb[67C7]
C7422	CAP_402	mlb[67B8]
C7423	CAP_402	mlb[67B7]
C7426	CAP_402	mlb[67A6]
C7427	CAP_402	mlb[67A5]
C7432	CAP_402	mlb[67B7]
C7455	CAP_402	mlb[67D6]
C7456	CAP_402	mlb[67D6]
C7457	CAP_402	mlb[67D6]
C7458	CAP_402	mlb[67A6]
C7459	CAP_402	mlb[67A7]
C7460	CAP_402	mlb[67A6]
C7501	CAP_402	mlb[68D7]
C7503	CAP_402	mlb[68D5]
C7505	CAP_P_SM	mlb[68D3]
C7506	CAP_P_SM	mlb[68D3]
C7507	CAP_603	mlb[68D4]
C7508	CAP_402	mlb[68D4]
C7509	CAP_402	mlb[68D3]
C7510	CAP_402	mlb[68D4]
C7511	CAP_402	mlb[68D4]
C7515	CAP_P_SM	mlb[68D2]
C7520	CAP_402	mlb[68B3]
C7521	CAP_402	mlb[68C7]
C7523	CAP_402	mlb[68C5]
C7526	CAP_P_SM	mlb[68D2]
C7528	CAP_402	mlb[68B4]
C7530	CAP_402	mlb[68C4]
C7531	CAP_402	mlb[68C4]
C7560	CAP_P_CASE-B4-SM	mlb[68A7]
C7561	CAP_P_CASE-B4-SM	mlb[68A6]
C7562	CAP_P_CASE-B4-SM	mlb[68A6]
C7563	CAP_P_CASE-B4-SM	mlb[68A6]
C7564	CAP_P_CASE-B4-SM	mlb[68A5]
C7565	CAP_P_CASE-B4-SM	mlb[68A5]
C7580	CAP_402	mlb[68D5]
C7581	CAP_603	mlb[68D5]
C7582	CAP_603	mlb[68C4]
C7601	CAP_402	mlb[69C7]
C7602	CAP_402	mlb[69C3]
C7603	CAP_402	mlb[69C6]
C7607	CAP_402	mlb[69D4]
C7608	CAP_402	mlb[69C4]
C7610	CAP_402	mlb[69D4]
C7615	CAP_603	mlb[69D4]
C7620	CAP_P_CASE-B4-SM	mlb[69C3]
C7621	CAP_P_CASE-B4-SM	mlb[69C2]
C7622	CAP_P_CASE-B4-SM	mlb[69C2]
C7623	CAP_402	mlb[69C2]
C7651	CAP_P_CASED2-SM	mlb[69D5]
C7652	CAP_P_CASED2-SM	mlb[69D5]
C7701	CAP_603	mlb[70C5]
C7702	CAP_402	mlb[70B6]
C7703	CAP_402	mlb[70B7]
C7704	CAP_402	mlb[70B7]
C7705	CAP_402	mlb[70B7]
C7720	CAP_P_SM	mlb[70C4]
C7721	CAP_P_SM	mlb[70C4]
C7722	CAP_402	mlb[70C3]
C7723	CAP_402	mlb[70C2]
C7724	CAP_402	mlb[70C3]
C7725	CAP_P_CASE-B4-SM	mlb[70C2]
C7726	CAP_P_CASE-B4-SM	mlb[70C2]
C7727	CAP_P_CASE-B4-SM	mlb[70C1]
C7730	CAP_402	mlb[70C4]
C7731	CAP_402	mlb[70B3]
C7740	CAP_402	mlb[70B3]
C7860	CAP_0805	mlb[71D7]
C7861	CAP_402	mlb[71D7]
C7862	CAP_0603	mlb[71D5]
C7863	CAP_402	mlb[71D5]
C7864	CAP_402	mlb[71C7]
C7865	CAP_402	mlb[71C8]
C7866	CAP_402	mlb[71D6]
C7867	CAP_0805	mlb[71D7]
C7868	CAP_402	mlb[71C7]
C7870	CAP_402	mlb[71B7]
C7871	CAP_603	mlb[71A7]
C7872	CAP_603	mlb[71B6]
C7873	CAP_0603	mlb[71D5]
C7900	CAP_402	mlb[72B7]
C7901	CAP_402	mlb[72B7]
C7902	CAP_603	mlb[72B6]
C7920	CAP_402	mlb[72B6]
C7950	CAP_402	mlb[72C2]
C7951	CAP_402	mlb[72C2]
C7952	CAP_402	mlb[72C2]
C7953	CAP_402	mlb[72C1]
C7962	CAP_402	mlb[72B2]
C7963	CAP_402	mlb[72B1]
C7970	CAP_402	mlb[72B2]
C7971	CAP_402	mlb[72B2]
C7972	CAP_402	mlb[72B2]
C7973	CAP_402	mlb[72B1]
C8020	CAP_201	mlb[73D7]
C8021	CAP_201	mlb[73D7]
C8022	CAP_201	mlb[73D7]
C8023	CAP_201	mlb[73D7]
C8024	CAP_201	mlb[73D7]
C8025	CAP_201	mlb[73C7]
C8026	CAP_201	mlb[73C7]
C8027	CAP_201	mlb[73C7]
C8028	CAP_201	mlb[73C7]
C8029	CAP_201	mlb[73C7]
C8030	CAP_201	mlb[73C7]
C8031	CAP_201	mlb[73C7]
C8032	CAP_201	mlb[73C7]
C8033	CAP_201	mlb[73C7]
C8034	CAP_201	mlb[73C7]
C8035	CAP_201	mlb[73C7]
C8055	CAP_201	mlb[73D5]
C8056	CAP_201	mlb[73D5]
C8057	CAP_201	mlb[73D5]
C8058	CAP_201	mlb[73D5]
C8059	CAP_201	mlb[73D5]
C8060	CAP_201	mlb[73C5]
C8061	CAP_201	mlb[73C5]
C8062	CAP_201	mlb[73C5]
C8063	CAP_201	mlb[73C5]
C8064	CAP_201	mlb[73C5]
C8065	CAP_201	mlb[73C5]
C8066	CAP_201	mlb[73C5]
C8067	CAP_201	mlb[73C5]
C8068	CAP_201	mlb[73C5]
C8069	CAP_201	mlb[73C5]
C8070	CAP_201	mlb[73C5]
C8100	CAP_603	mlb[74D7]
C8101	CAP_603	mlb[74D6]
C8102	CAP_603	mlb[74D6]
C8103	CAP_603	mlb[74D6]
C8104	CAP_603	mlb[74D5]
C8105	CAP_402	mlb[74D8]
C8106	CAP_402	mlb[74D8]
C8107	CAP_402	mlb[74D7]
C8108	CAP_402	mlb[74D7]
C8109	CAP_402	mlb[74D7]
C8110	CAP_402	mlb[74D7]
C8111	CAP_402	mlb[74D6]
C8112	CAP_402	mlb[74D6]
C8113	CAP_402	mlb[74D6]
C8114	CAP_402	mlb[74D5]
C8115	CAP_201	mlb[74C8]
C8116	CAP_201	mlb[74C8]
C8117	CAP_201	mlb[74C7]
C8118	CAP_201	mlb[74C7]
C8119	CAP_201	mlb[74C7]
C8120	CAP_201	mlb[74C7]
C8121	CAP_201	mlb[74C6]
C8122	CAP_201	mlb[74C6]
C8123	CAP_201	mlb[74C6]
C8124	CAP_201	mlb[74C5]
C8125	CAP_603	mlb[74C7]
C8126	CAP_402	mlb[74C7]
C8127	CAP_402	mlb[74C6]
C8128	CAP_402	mlb[74C6]
C8129	CAP_201	mlb[74C6]
C8130	CAP_603	mlb[74C7]
C8131	CAP_402	mlb[74C7]
C8132	CAP_201	mlb[74C7]
C8133	CAP_603	mlb[74C6]
C8134	CAP_402	mlb[74C6]
C8135	CAP_402	mlb[74C6]
C8136	CAP_402	mlb[74C5]
C8137	CAP_603	mlb[74B7]
C8138	CAP_402	mlb[74B7]
C8139	CAP_402	mlb[74B7]
C8140	CAP_201	mlb[74B6]
C8141	CAP_201	mlb[74B6]
C8142	CAP_603	mlb[74B7]
C8143	CAP_402	mlb[74B7]
C8144	CAP_201	mlb[74B7]
C8145	CAP_603	mlb[74A7]
C8146	CAP_402	mlb[74A7]
C8147	CAP_402	mlb[74A6]
C8148	CAP_402	mlb[74A6]
C8149	CAP_201	mlb[74A6]
C8150	CAP_201	mlb[74A5]
C8151	CAP_603	mlb[74A7]
C8152	CAP_402	mlb[74A7]
C8153	CAP_402	mlb[74A7]
C8154	CAP_402	mlb[74A7]
C8155	CAP_402	mlb[74A6]
C8156	CAP_402	mlb[74A6]
C8157	CAP_402	mlb[74A6]
C8158	CAP_402	mlb[74A5]
C8160	CAP_402	mlb[74D4]
C8161	CAP_402	mlb[74D3]
C8162	CAP_402	mlb[74D3]
C8163	CAP_402	mlb[74D3]
C8164	CAP_402	mlb[74D3]
C8165	CAP_402	mlb[74D2]
C8166	CAP_402	mlb[74D2]
C8167	CAP_402	mlb[74D2]
C8168	CAP_402	mlb[74D2]
C8169	CAP_402	mlb[74D1]
C8170	CAP_402	mlb[74C4]
C8171	CAP_402	mlb[74C3]
C8172	CAP_402	mlb[74C3]
C8173	CAP_402	mlb[74C3]
C8174	CAP_402	mlb[74C3]
C8175	CAP_402	mlb[74C2]
C8176	CAP_402	mlb[74C2]
C8177	CAP_402	mlb[74C2]
C8178	CAP_402	mlb[74C2]
C8179	CAP_402	mlb[74C1]
C8180	CAP_402	mlb[74C4]
C8181	CAP_402	mlb[74C3]
C8182	CAP_402	mlb[74C3]
C8183	CAP_402	mlb[74C3]
C8184	CAP_402	mlb[74C3]
C8185	CAP_402	mlb[74C2]
C8186	CAP_402	mlb[74C2]
C8187	CAP_402	mlb[74C2]
C8188	CAP_402	mlb[74C2]
C8189	CAP_402	mlb[74C1]
C8190	CAP_603	mlb[74B4]
C8191	CAP_603	mlb[74B3]
C8192	CAP_603	mlb[74B3]
C8193	CAP_603	mlb[74B3]
C8194	CAP_603	mlb[74B3]
C8195	CAP_603	mlb[74B2]
C8196	CAP_603	mlb[74B2]
C8197	CAP_603	mlb[74B2]
C8198	CAP_603	mlb[74B2]
C8199	CAP_603	mlb[74B1]
C8200	CAP_402	mlb[75A7]
C8201	CAP_402	mlb[75A6]
C8202	CAP_402	mlb[75A5]
C8203	CAP_402	mlb[75A4]
C8251	CAP_402	mlb[75A3]
C8252	CAP_402	mlb[75A3]
C8260	CAP_402	mlb[75A2]
C8301	CAP_402	mlb[76D5]
C8302	CAP_402	mlb[76D4]
C8303	CAP_402	mlb[76D4]
C8304	CAP_402	mlb[76D3]
C8305	CAP_0603	mlb[76D2]
C8307	CAP_402	mlb[76C5]
C8308	CAP_402	mlb[76D4]
C8309	CAP_402	mlb[76C5]
C8310	CAP_402	mlb[76C5]
C8311	CAP_P_CASE-B2-SM	mlb[76D2]
C8315	CAP_P_SM	mlb[76D3]
C8332	CAP_402	mlb[76A8]
C8333	CAP_402	mlb[76A7]
C8334	CAP_402	mlb[76A7]
C8350	CAP_402	mlb[76B5]
C8351	CAP_P_SM	mlb[76B6]
C8352	CAP_603	mlb[76B6]
C8353	CAP_402	mlb[76B6]
C8354	CAP_402	mlb[76B4]
C8355	CAP_402	mlb[76A5]
C8356	CAP_402	mlb[76B4]
C8357	CAP_402	mlb[76A4]
C8358	CAP_402	mlb[76A4]
C8359	CAP_402	mlb[76A3]
C8360	CAP_402	mlb[76B2]
C8361	CAP_P_CASE-B2-SM	mlb[76B2]
C8362	CAP_P_CASE-B2-SM	mlb[76B2]
C8401	CAP_402	mlb[77D6]
C8402	CAP_402	mlb[77D5]
C8403	CAP_402	mlb[77D5]
C8404	CAP_402	mlb[77C4]
C8405	CAP_0603	mlb[77C3]
C8407	CAP_402	mlb[77C6]
C8408	CAP_402	mlb[77C4]

C8409	CAP_402	mlb[77C6]
C8410	CAP_402	mlb[77C6]
C8411	CAP_P_CASE-B2-SM	mlb[77C3]
C8415	CAP_603	mlb[77D4]
C8500	CAP_402	mlb[78C8]
C8501	CAP_402	mlb[78C8]
C8502	CAP_402	mlb[78C8]
C8503	CAP_402	mlb[78B8]
C8504	CAP_402	mlb[78B8]
C8505	CAP_402	mlb[78B8]
C8506	CAP_402-1	mlb[78B8]
C8507	CAP_402-1	mlb[78B8]
C8508	CAP_402-1	mlb[78B8]
C8509	CAP_402-1	mlb[78B7]
C8510	CAP_402-1	mlb[78B8]
C8511	CAP_402-1	mlb[78B8]
C8512	CAP_402-1	mlb[78B8]
C8513	CAP_402-1	mlb[78B7]
C8514	CAP_402-1	mlb[78A8]
C8515	CAP_402-1	mlb[78A8]
C8516	CAP_201	mlb[78A8]
C8517	CAP_201	mlb[78A7]
C8518	CAP_201	mlb[78A8]
C8519	CAP_201	mlb[78A8]
C8520	CAP_201	mlb[78A8]
C8521	CAP_201	mlb[78A7]
C8522	CAP_201	mlb[78A8]
C8523	CAP_201	mlb[78A8]
C8524	CAP_201	mlb[78A8]
C8525	CAP_201	mlb[78A7]
C8530	CAP_402-1	mlb[78B5]
C8531	CAP_402-1	mlb[78B5]
C8532	CAP_402-1	mlb[78B5]
C8533	CAP_402-1	mlb[78A5]
C8534	CAP_402-1	mlb[78A5]
C8535	CAP_402-1	mlb[78A5]
C8550	CAP_402	mlb[78C5]
C8551	CAP_402	mlb[78C4]
C8552	CAP_402	mlb[78C4]
C8553	CAP_402	mlb[78B5]
C8554	CAP_402	mlb[78B4]
C8555	CAP_402	mlb[78B4]
C8556	CAP_402-1	mlb[78B5]
C8557	CAP_402-1	mlb[78B4]
C8558	CAP_402-1	mlb[78B4]
C8559	CAP_402-1	mlb[78B4]
C8560	CAP_402-1	mlb[78B5]
C8561	CAP_402-1	mlb[78B4]
C8562	CAP_402-1	mlb[78B4]
C8563	CAP_402-1	mlb[78B4]
C8564	CAP_402-1	mlb[78B5]
C8565	CAP_402-1	mlb[78B4]
C8566	CAP_201	mlb[78B4]
C8567	CAP_201	mlb[78B4]
C8568	CAP_201	mlb[78A5]
C8569	CAP_201	mlb[78A4]
C8570	CAP_201	mlb[78A4]
C8571	CAP_201	mlb[78A4]
C8572	CAP_201	mlb[78A5]
C8573	CAP_201	mlb[78A4]
C8574	CAP_201	mlb[78A4]
C8575	CAP_201	mlb[78A4]
C8580	CAP_402-1	mlb[78B2]
C8581	CAP_402-1	mlb[78B2]
C8582	CAP_402-1	mlb[78B2]
C8583	CAP_402-1	mlb[78A2]
C8584	CAP_402-1	mlb[78B1]
C8585	CAP_402-1	mlb[78B1]
C8600	CAP_402	mlb[79B7]
C8601	CAP_603	mlb[79B7]
C8602	CAP_402	mlb[79B7]
C8603	CAP_402	mlb[79B7]
C8604	CAP_603	mlb[79A7]
C8605	CAP_402	mlb[79A7]
C8606	CAP_402	mlb[79A7]
C8607	CAP_603	mlb[79A7]
C8608	CAP_402	mlb[79A7]
C8609	CAP_402	mlb[79A7]
C8700	CAP_402	mlb[80B4]
C8701	CAP_402	mlb[80B3]
C8702	CAP_402	mlb[80C3]
C8703	CAP_402	mlb[80C3]
C8721	CAP_402	mlb[80C5]
C8800	CAP_603	mlb[81B7]
C8801	CAP_402	mlb[81B7]
C8802	CAP_402	mlb[81B7]
C8803	CAP_603	mlb[81B5]
C8804	CAP_402	mlb[81B5]
C8805	CAP_402	mlb[81B4]
C8806	CAP_603	mlb[81A7]
C8807	CAP_402	mlb[81A7]
C8808	CAP_402	mlb[81A7]
C8809	CAP_603	mlb[81A5]
C8810	CAP_402	mlb[81A5]
C8811	CAP_402	mlb[81A4]
C8812	CAP_603	mlb[81B7]
C8813	CAP_402	mlb[81B7]
C8814	CAP_402	mlb[81B7]
C8815	CAP_603	mlb[81B5]
C8816	CAP_402	mlb[81B5]
C8817	CAP_402	mlb[81B4]
C8901	CAP_402	mlb[82D7]
C8902	CAP_402	mlb[82D6]
C8903	CAP_402	mlb[82D6]
C8904	CAP_402	mlb[82D7]
C8906	CAP_402	mlb[82B4]
C8920	CAP_402	mlb[82C7]
C8921	CAP_402	mlb[82C6]
C8922	CAP_402	mlb[82C7]
C8923	CAP_402	mlb[82C7]
C8932	CAP_603	mlb[82D5]
C8933	CAP_402	mlb[82D2]
C8934	CAP_402	mlb[82D5]
C8940	CAP_P_SM	mlb[82D4]
C8941	CAP_P_SM	mlb[82D3]
C8942	CAP_P_CASE-B4-SM	mlb[82C1]
C8943	CAP_P_CASE-B4-SM	mlb[82C1]
C8945	CAP_603	mlb[82D2]
C8950	CAP_402	mlb[82B7]
C8951	CAP_402	mlb[82B7]
C8952	CAP_402	mlb[82B7]
C8953	CAP_402	mlb[82C6]
C8956	CAP_402	mlb[82C5]
C8965	CAP_603	mlb[82C2]

C8966	CAP_603	mlb[82C2]
C8967	CAP_P_CASE-B4-SM	mlb[82C2]
C8968	CAP_603	mlb[82C2]
C8969	CAP_402	mlb[82C3]
C8970	CAP_P_SM	mlb[82D3]
C8971	CAP_402-1	mlb[82B5]
C8972	CAP_402	mlb[82B5]
C8980	CAP_402	mlb[82C4]
C9000	CAP_402	mlb[83D6]
C9001	CAP_402	mlb[83D6]
C9002	CAP_402	mlb[83D6]
C9003	CAP_402	mlb[83D6]
C9004	CAP_402	mlb[83D6]
C9005	CAP_402	mlb[83D6]
C9006	CAP_402	mlb[83D6]
C9007	CAP_402	mlb[83D6]
C9015	CAP_402	mlb[83D5]
C9016	CAP_402	mlb[83C5]
C9020	CAP_402	mlb[83B7]
C9021	CAP_402	mlb[83B7]
C9022	CAP_402	mlb[83B7]
C9023	CAP_402	mlb[83B7]
C9024	CAP_402	mlb[83B7]
C9025	CAP_402	mlb[83B7]
C9026	CAP_402	mlb[83B7]
C9027	CAP_402	mlb[83B7]
C9028	CAP_402	mlb[83B7]
C9029	CAP_402	mlb[83B7]
C9030	CAP_201	mlb[83A7]
C9031	CAP_201	mlb[83A7]
C9032	CAP_201	mlb[83A7]
C9033	CAP_201	mlb[83A7]
C9034	CAP_201	mlb[83A7]
C9035	CAP_201	mlb[83A7]
C9036	CAP_201	mlb[83A7]
C9037	CAP_201	mlb[83A7]
C9038	CAP_201	mlb[83A7]
C9039	CAP_201	mlb[83A7]
C9040	CAP_402	mlb[83D2]
C9041	CAP_402	mlb[83D2]
C9042	CAP_402	mlb[83D2]
C9043	CAP_402	mlb[83D2]
C9044	CAP_402	mlb[83D2]
C9045	CAP_402	mlb[83D2]
C9046	CAP_402	mlb[83D2]
C9047	CAP_402	mlb[83D2]
C9085	CAP_402	mlb[83B2]
C9086	CAP_402	mlb[83B2]
C9090	CAP_402-1	mlb[83C7]
C9100	CAP_603	mlb[84D7]
C9101	CAP_603	mlb[84D7]
C9105	CAP_402-1	mlb[84D7]
C9106	CAP_402-1	mlb[84D6]
C9107	CAP_402-1	mlb[84D6]
C9108	CAP_402-1	mlb[84D6]
C9109	CAP_402-1	mlb[84D5]
C9110	CAP_402-1	mlb[84D7]
C9111	CAP_402-1	mlb[84D6]
C9112	CAP_402-1	mlb[84D6]
C9113	CAP_402-1	mlb[84D6]
C9114	CAP_402-1	mlb[84D5]
C9120	CAP_402-1	mlb[84C6]
C9121	CAP_402-1	mlb[84C6]
C9122	CAP_402-1	mlb[84C5]
C9130	CAP_402-LF	mlb[84C5]
C9143	CAP_402-1	mlb[84D3]
C9144	CAP_402-1	mlb[84D4]
C9145	CAP_402-1	mlb[84D3]
C9146	CAP_603	mlb[84D3]
C9147	CAP_603	mlb[84D3]
C9150	CAP_402-1	mlb[84C3]
C9151	CAP_402-1	mlb[84C3]
C9152	CAP_402-1	mlb[84C3]
C9153	CAP_402-1	mlb[84C4]
C9160	CAP_402-LF	mlb[84C4]
C9170	CAP_402-LF	mlb[84C4]
C9200	CAP_402	mlb[85C7]
C9210	CAP_402-1	mlb[85B7]
C9215	CAP_402-1	mlb[85A7]
C9221	CAP_0201	mlb[85B2]
C9222	CAP_0201	mlb[85B2]
C9223	CAP_0201	mlb[85B2]
C9224	CAP_0201	mlb[85B2]
C9225	CAP_0201	mlb[85A4]
C9226	CAP_0201	mlb[85A2]
C9227	CAP_0201	mlb[85A2]
C9228	CAP_0201	mlb[85B4]
C9230	CAP_0201	mlb[85A4]
C9231	CAP_0201	mlb[85B4]
C9300	CAP_402	mlb[86D7]
C9301	CAP_402	mlb[86D7]
C9302	CAP_402	mlb[86D7]
C9303	CAP_402	mlb[86D7]
C9304	CAP_402	mlb[86D7]
C9305	CAP_402	mlb[86D7]
C9306	CAP_402	mlb[86D7]
C9307	CAP_402	mlb[86D7]
C9308	CAP_402	mlb[86D7]
C9309	CAP_402	mlb[86D7]
C9310	CAP_402-LF	mlb[86C7]
C9311	CAP_402	mlb[86C7]
C9312	CAP_402	mlb[86C7]
C9319	CAP_402-LF	mlb[86B5]
C9330	CAP_402	mlb[86A5]
C9331	CAP_402	mlb[86A5]
C9357	CAP_402	mlb[86A7]
C9358	CAP_402	mlb[86C3]
C9359	CAP_402	mlb[86C3]
C9360	CAP_0201	mlb[86C3]
C9361	CAP_0201	mlb[86C3]
C9362	CAP_402	mlb[86C4]
C9363	CAP_402	mlb[86C4]
C9364	CAP_0201	mlb[86C3]
C9365	CAP_0201	mlb[86C3]
C9366	CAP_402	mlb[86C4]
C9367	CAP_402	mlb[86C4]
C9368	CAP_402	mlb[86B4]
C9369	CAP_402	mlb[86B4]
C9370	CAP_201	mlb[86D3]
C9371	CAP_201	mlb[86D3]
C9372	CAP_201	mlb[86D3]
C9373	CAP_201	mlb[86D3]
C9380	CAP_201	mlb[86D3]
C9381	CAP_201	mlb[86D3]

C9382	CAP_201	mlb[86D3]
C9383	CAP_201	mlb[86D3]
C9390	CAP_402	mlb[86B1]
C9391	CAP_402	mlb[86B1]
C9400	CAP_402	mlb[87C6]
C9401	CAP_0201	mlb[87A6]
C9402	CAP_0201	mlb[87A6]
C9405	CAP_201	mlb[87C2]
C9406	CAP_201	mlb[87B2]
C9410	CAP_603-1	mlb[87D3]
C9411	CAP_603-1	mlb[87D2]
C9420	CAP_0805	mlb[87D8]
C9421	CAP_402	mlb[87D8]
C9422	CAP_0805	mlb[87D7]
C9423	CAP_402	mlb[87D6]
C9424	CAP_805	mlb[87D5]
C9425	CAP_805	mlb[87D5]
C9427	CAP_402-1	mlb[87D8]
C9428	CAP_402-1	mlb[87D7]
C9450	CAP_603-1	mlb[87C7]
C9470	CAP_201	mlb[87B2]
C9471	CAP_201	mlb[87B2]
C9472	CAP_201	mlb[87B2]
C9473	CAP_201	mlb[87B2]
C9494	CAP_201	mlb[87A7]
C9495	CAP_201	mlb[87A7]
C9498	CAP_402	mlb[87A6]
C9499	CAP_402	mlb[87A6]
C9710	CAP_402	mlb[88D7]
C9711	CAP_402	mlb[88D7]
C9712	CAP_402	mlb[88C7]
C9713	CAP_402	mlb[88D7]
C9714	CAP_402	mlb[88C7]
C9715	CAP_402	mlb[88C7]
C9716	CAP_402	mlb[88C7]
C9717	CAP_402	mlb[88C7]
C9740	CAP_402	mlb[88D3]
C9741	CAP_402	mlb[88D2]
C9742	CAP_402	mlb[88D2]
C9743	CAP_402	mlb[88D2]
C9744	CAP_402	mlb[88D4]
C9745	CAP_402	mlb[88D4]
C9746	CAP_402	mlb[88D3]
C9747	CAP_402	mlb[88D3]
C9748	CAP_402	mlb[88D3]
C9749	CAP_402	mlb[88D2]
C9750	CAP_402	mlb[88D2]
C9751	CAP_402	mlb[88D2]
C9760	CAP_402-LF	mlb[88B5]
C9800	CAP_0603	mlb[89C4]
C9802	CAP_402	mlb[89C4]
C9803	CAP_603	mlb[89C3]
C9810	CAP_402	mlb[89B5]
C9811	CAP_402	mlb[89B6]
C9813	CAP_402	mlb[89A6]
C9814	CAP_402	mlb[89A6]
C9830	CAP_603	mlb[89C2]
CL3601	SPRING_CLIP_1P_CLIP-SM-K40	mlb[35C8]
CL3602	SPRING_CLIP_1P_CLIP-SM-K40	mlb[35C8]
CL3603	SPRING_CLIP_1P_CLIP-SM-K40	mlb[35C8]
CL3604	SPRING_CLIP_1P_CLIP-SM-K40	mlb[35B8]
CL3606	SPRING_CLIP_1P_CLIP-SM-K40	mlb[35B8]
CL3608	SPRING_CLIP_1P_CLIP-SM-K40	mlb[35B8]
CL3614	SPRING_CLIP_1P_CLIP-SM-K40	mlb[35B8]
CL3615	SPRING_CLIP_1P_CLIP-SM-K40	mlb[35B8]
CL3616	SPRING_CLIP_1P_CLIP-SM-K40	mlb[35B8]
CL3617	SPRING_CLIP_1P_CLIP-SM-K40	mlb[35B8]
CL3618	SPRING_CLIP_1P_CLIP-SM-K40	mlb[35B8]
D2400	DIODE_SCHOT_6PB_SOT-363	mlb[23B7 23C7]
D2600	DIODE_SCHOT_SOD-523	mlb[25B1]
D2800	DIODE_SCHOT_6PB_SOT-363	mlb[27D6]
D3800	RCLAMP0524P_SLP2510P8	mlb[36B7]
D3801	RCLAMP0524P_SLP2510P8	mlb[36B7]
D4300	DIODE_SMB	mlb[41D4]
D4305	DIODE_3P_CA_SOT-523-3	mlb[41D5]
D4350	DIODE_SCHOT_3P_SOT323	mlb[41A4]
D4390	ZENER_SOT23	mlb[41B2]
D4600	DIODE_SCHOT_3P_A_SC-75	mlb[43B2]
D4601	DIODE_SCHOT_3P_A_SC-75	mlb[43B4]
D4602	DIODE_SCHOT_3P_A_SC-75	mlb[43A4]
D4603	DIODE_SCHOT_3P_A_SC-75	mlb[43C2]
D4700	DIODE_SCHOT_SOD-323	mlb[44C5]
D9360	DIODE_TSLP-2-7	mlb[86D2]
D9361	DIODE_TSLP-2-7	mlb[86C2]
D9364	DIODE_TSLP-2-7	mlb[86D2]
D9365	DIODE_TSLP-2-7	mlb[86D2]
D9372	DIODE_TSLP-2-7	mlb[86D2]
D9373	DIODE_TSLP-2-7	mlb[86D2]
D9382	DIODE_TSLP-2-7	mlb[86D2]
D9383	DIODE_TSLP-2-7	mlb[86D2]
D9401	DIODE_SCHOT_POWERDI-123	mlb[87D6]
D9403	ZENER_SOT23	mlb[87D3]
D9410	DIODE_SCHOT_DSN2	mlb[87D1]
D9498	DIODE_TSLP-2-7	mlb[87B7]
D9499	DIODE_TSLP-2-7	mlb[87B7]
D9800	RCLAMP0504F_SC70-6-1	mlb[89B7]
D9810	RCLAMP0524P_SLP2510P8	mlb[89D6 89C6]
D9811	RCLAMP0524P_SLP2510P8	mlb[89D6 89C6]
DP4310	DIODE_DUAL_6P_SOT-363	mlb[41C3 41C3]

DP4311	DIODE_DUAL_6P_SOT-363	mlb[41B3 41B3]
DZ6000	SUPPR_TRANSIENT1_402	mlb[57C6]
DZ6001	SUPPR_TRANSIENT1_402	mlb[57C6]
DZ6002	SUPPR_TRANSIENT1_SOD882	mlb[57C6]
DZ6003	SUPPR_TRANSIENT1_402	mlb[57C5]
DZ6004	SUPPR_TRANSIENT1_402	mlb[57C5]
DZ6005	SUPPR_TRANSIENT1_SOD882	mlb[57C5]
DZ6006	SUPPR_TRANSIENT1_SOD882	mlb[57C5]
DZ6050	SUPPR_TRANSIENT1_402	mlb[57A5]
DZ6051	SUPPR_TRANSIENT1_SOD882	mlb[57A7]
DZ6052	SUPPR_TRANSIENT1_402	mlb[57A5]
DZ6053	SUPPR_TRANSIENT1_402	mlb[57A5]
DZ6054	SUPPR_TRANSIENT1_SOD882	mlb[57A6]
DZ6055	SUPPR_TRANSIENT1_SOD882	mlb[57A6]
F4300	FUSE_603	mlb[41D3]
J0900	TP1_SM-TP3P4X1P8-TOP	mlb[9B5]
J0901	TP1_SM-TP3P4X1P8-TOP	mlb[9B5]
J2500	CON_F60ST_D_SM1_F-ST-SM	mlb[24D6]
J2800	BATTERY_2P_SM	mlb[27D8]
J3100	CON_F408RT_4MT_DDR3DIMM_SM1_F-RT-SM	mlb[30D6]
J3100	CON_F408RT_4MT_DDR3DIMM_SM1_F-RT-SM	mlb[31D6]
J3500	CON_F16RT_4MT_SDCARD_S_TH_F-RT-TH	mlb[34C2]
J3601	CON_F30ST_D4MT_SM_F-ST-SM	mlb[35D6]
J3800	CON_RJ45_8RT_D4MT_TH2_F-R-TH	mlb[36C1]
J4300	CON_F9RT_D4MT_1394B_TH_F-RT-TH	mlb[41C1]
J4401	CON_F16ST_D_SM_F-ST-SM-J40	mlb[42D6]
J4410	CON_F16ST_D_SM_F-ST-SM-J40	mlb[42D3]
J4600	CON_F4RT_USB_S2MT_TH_F-RT-TH	mlb[43D1]
J4610	CON_F4RT_USB_S2MT_TH_F-RT-TH	mlb[43C1]
J4620	CON_F4RT_USB_S2MT_TH_F-RT-TH	mlb[43B4]
J4630	CON_F4RT_USB_S2MT_TH_F-RT-TH	mlb[43A3]
J4800	CON_M5RT_S2MT_SMA_M-RT-SM	mlb[45D2]
J4801	CON_M2RT_S2MT_SM_M-RT-SM	mlb[45A4]
J5100	CON_M30ST_D4MT_SM_M-ST-SM	mlb[48D4]
J6000	CON_F21RT_4MT_AUDIO_SPDIF_TH1_F-RT-TH	mlb[57C8]
J6001	CON_M2RT_S2MT_SM_M-RT-SM	mlb[57B1]
J6500	CON_M4RT_S2MT_SM_M-RT-SM	mlb[60C2]
J7900	CON_M9RT_S_SM_M-RT-SM	mlb[72B8]
J9400	CON_F20RT_D16MT_DSPLYPRT_TH_F-RT-TH	mlb[87B3]
J9830	CON_F19RT_17MT_HDMI_F-RT-SM	mlb[89C3]
L2406	IND_0805	mlb[23D8]
L2451	IND_0603	mlb[23C4]
L2490	IND_0603	mlb[23B4]
L2491	IND_0603	mlb[23B4]
L3540	IND_0402	mlb[34C6]
L3541	IND_0402	mlb[34C5]
L3550	IND_0402	mlb[34C4]
L3551	IND_0402	mlb[34C3]
L3601	FILTER_4P2_DLP11S	mlb[35D5]
L3603	FILTER_4P2_DLP0NS	mlb[35C5]
L3604	IND_0603	mlb[35C5]
L3606	IND_0402	mlb[35C5]
L3900	IND_SM	mlb[37D7]
L3905	IND_SM	mlb[37D7]
L3910	IND_SM	mlb[37C7]
L3920	IND_SM	mlb[37D2]
L3925	IND_SM	mlb[37D2]
L3930	IND_SM	mlb[37C2]
L4020	IND_2520	mlb[38D6]
L4250	IND_0402	mlb[40D3]
L4251	IND_0402	mlb[40D2]
L4252	IND_0402	mlb[40C3]
L4253	IND_0402	mlb[40C2]
L4300	IND_SM	mlb[41D2]
L4310	FILTER_4P_TCM1210-4SM	mlb[41C2]
L4311	FILTER_4P_TCM1210-4SM	mlb[41C2]
L4600	IND_0603	mlb[43D3]
L4602	FILTER_4P_2012-HF	mlb[43D3]
L4610	IND_0603	mlb[43C3]
L4612	FILTER_4P_2012-HF	mlb[43B3]
L4620	IND_0603	mlb[43C5]
L4622	FILTER_4P_2012-HF	mlb[43B5]
L4630	IND_0603	mlb[43A5]
L4632	FILTER_4P_2012-HF	mlb[43A5]
L4800	IND_SM	mlb[45B2]
L4810	IND_0402	mlb[45D2]
L4811	IND_0402	mlb[45C2]
L5650	IND_0402	mlb[53A7]
L5651	IND_0402	mlb[53A7]
L5801	IND_0402	mlb[55B5]
L5900	IND_0402	mlb[56B7]
L5901	IND_0402	mlb[56C7]
L5902	IND_0402	mlb[56B7]
L6000	IND_0402	mlb[57D4]
L6001	IND_0402	mlb[57D4]
L6002	IND_0402	mlb[57D4]
L6003	IND_0402	mlb[57C4]
L6004	IND_0603	mlb[57C4]
L6005	IND_0402	mlb[57C4]
L6006	IND_0402	mlb[57D4]
L6007	IND_0402	mlb[57D4]
L6051	IND_0402	mlb[57B4]
L6052	IND_0402	mlb[57B4]

L6053	IND_0402	mlb[57B4]
L6054	IND_0402	mlb[57B4]
L6092	IND_0603	mlb[57C2]
L6100	IND_0402	mlb[58A3]
L6180	IND_0402	mlb[58D3]
L6500	IND_0402	mlb[60C3]
L6510	FILTER_2P_0603	mlb[60D3]
L6520	FILTER_2P_0603	mlb[60C3]
L7100	IND_FDV0630H-SM	mlb[64C3]
L7201	IND_MMD-06CZ	mlb[65C4]
L7251	IND_PIMB065T-SM	mlb[65B4]
L7302	IND_PIMB042T-COMBO	mlb[66D5]
L7330	IND_PIMB103E-SM-1	mlb[66C3]
L7500	IND_PCMB063T-MMD06CZ -SM	mlb[68D5]
L7501	IND_PIMA104E-SM-1	mlb[68D3]
L7521	IND_PIMA104E-SM-1	mlb[68C3]
L7601	IND_PIMB065T-SM	mlb[69C4]
L7730	IND_PIMB104T-SM	mlb[70C3]
L7860	IND_2520	mlb[71D6]
L8120	IND_0402	mlb[74C7]
L8130	FILTER_2P_0603	mlb[74C7]
L8131	FILTER_2P_0603	mlb[74B7]
L8132	IND_0402	mlb[74B7]
L8140	IND_0603	mlb[74A7]
L8150	IND_0402	mlb[74D3]
L8155	IND_0603	mlb[74A8]
L8300	IND_PIMB042T-SM	mlb[76D3]
L8351	IND_PIMB065T-SM	mlb[76B3]
L8400	IND_PIMB042T-SM	mlb[77C4]
L8600	FILTER_2P_0603	mlb[79B8]
L8601	FILTER_2P_0603	mlb[79A8]
L8602	IND_0402	mlb[79A8]
L8702	IND_0402	mlb[80C3]
L8703	IND_0402	mlb[80C3]
L8800	FILTER_2P_0603	mlb[81B7]
L8801	FILTER_2P_0603	mlb[81B5]
L8802	FILTER_2P_0603	mlb[81A7]
L8803	FILTER_2P_0603	mlb[81A5]
L8804	FILTER_2P_0603	mlb[81B7]
L8805	FILTER_2P_0603	mlb[81B5]
L8900	IND_PIMB042T-COMBO	mlb[82D3]
L8920	IND_FDU1040D-SM	mlb[82C4]
L9130	IND_0402	mlb[84C7]
L9170	IND_0402	mlb[84C2]
L9372	IND_0201-1	mlb[86D4]
L9373	IND_0201-1	mlb[86D4]
L9382	IND_0201-1	mlb[86D4]
L9383	IND_0201-1	mlb[86D4]
L9400	IND_0603	mlb[87C5]
L9408	IND_0603	mlb[87A2]
L9498	IND_0603	mlb[87B6]
L9499	IND_0603	mlb[87A6]
L9810	IND_0402	mlb[89B6]
L9811	IND_0402	mlb[89A6]
L9830	IND_SM-1	mlb[89D2]
L9841	IND_0402	mlb[89A6]
L9890	FILTER_4P_ACM2012H	mlb[89D7]
L9891	FILTER_4P_ACM2012H	mlb[89C7]
L9892	FILTER_4P_ACM2012H	mlb[89C7]
L9893	FILTER_4P_ACM2012-SM	mlb[89B7]
LED0600	LED_2.0X1.25MM-SM	mlb[6C3]
LED0602	LED_2.0X1.25MM-SM	mlb[6C2]
LED0603	LED_2.0X1.25MM-SM	mlb[6C1]
LED0605	LED_2X125-SM	mlb[6B1]
Q0603	TRA_SSM3K15FV_SOD-VE -HF	mlb[6C2]
Q0605	TRA_NMOSFET_NPN_6P2_ SOT-563	mlb[6B2 6B2]
Q2520	TRA_SSM3K15FV_SOD-VE -HF	mlb[24B5]
Q2530	TRA_PNP_SOT323_SOT323	mlb[24C1]
Q2550	TRA_SSM3K15FV_SOD-VE -HF	mlb[24B3]
Q2640	TRA_2N7002DW_SOT-363	mlb[25B2 25B1]
Q2900	TRA_DUAL_SSM6N15FE_S OT563	mlb[28B6 28C6]
Q2905	TRA_DUAL_SSM6N15FE_S OT563	mlb[28C6 28C6]
Q2910	TRA_DUAL_SSM6N15FE_S OT563	mlb[28B6 28B6]
Q2915	TRA_DUAL_SSM6N15FE_S OT563	mlb[28B7 28B6]
Q2920	TRA_NMOSFET_NPN_6P2_ SOT-563	mlb[28C2 28C3]
Q2950	TRA_DUAL_SSM6N15FE_S OT563	mlb[28B2 28B3]
Q3530	TRA_SSM3K15FV_SOD-VE -HF	mlb[34B5]
Q3650	TRA_MOSFET_PCHN_8P4_ 23V1K-SM	mlb[35C3]
Q4010	TRA_DUAL_SSM6N15FE_S OT563	mlb[38A4 38B3]
Q4050	TRA_SSM3K15FV_SOD-VE -HF	mlb[38C3]
Q4300	TRA_MOSFET_PCHN_5P1_ MLP3.3X3.3	mlb[41D5]
Q4301	TRA_PNP_SOT23_SOT23	mlb[41D7]
Q4302	TRA_DUAL_MMDT3906_SO T-363	mlb[41C6 41C5]
Q4303	TRA_DUAL_MMDT3904_SO T-363-LF	mlb[41B5 41B5]
Q4305	TRA_BSS84_SOT23-3-HF	mlb[41D6]
Q4370	TRA_2N7002DW_SOT-363	mlb[41C7 41C7]
Q4800	TRA_SSM3K15FV_SOD-VE -HF	mlb[45C6]
Q4801	TRA_DUAL_MMDT3906_SO T-363	mlb[45D5 45D5]
Q5059	TRA_DUAL_SSM6N15FE_S OT563	mlb[47D3 47C3]
Q5060	TRA_NMOSFET_NPN_6P2_ SOT-563	mlb[47D2 47D2]
Q5415	TRA_DUAL_COMP_DMG101 6V_SOT-563	mlb[51C3 51D3]
Q5520	TRA_BC846BM3T5G_NPN_ SOT732-3	mlb[52D2]
Q5530	TRA_BC846BM3T5G_NPN_ SOT732-3	mlb[52A7]
Q5540	TRA_BC846BM3T5G_NPN_ SOT732-3	mlb[52A7]
Q5560	TRA_BC846BM3T5G_NPN_ SOT732-3	mlb[52B2]
Q5570	TRA_BC846BM3T5G_NPN_ SOT732-3	mlb[52C2]
Q5580	TRA_BC846BM3T5G_NPN_ SOT732-3	mlb[52C2]
Q5590	TRA_BC846BM3T5G_NPN_ SOT732-3	mlb[52B2]
Q6100	TRA_DUAL_SSM6N15FE_S OT563	mlb[58C7 58B6]
Q6101	TRA_DUAL_SSM6N15FE_S OT563	mlb[58C5 58C6]
Q6102	TRA_SSM3K15FV_SOD-VE -HF	mlb[58A5]
Q6103	TRA_DUAL_SSM6N15FE_S OT563	mlb[58B3 58B2]
Q6500	TRA_FDC638P_SM	mlb[60D4]
Q6501	TRA_SSM3K15FV_SOD-VE -HF	mlb[60C6]
Q6700	TRA_MOSFET_PCHN_4P_S C70-6L	mlb[61D2]
Q6701	TRA_MOSFET_NCHN_PWRP K-1212-8-HF	mlb[61B6]
Q6702	TRA_DUAL_SSM6N15FE_S OT563	mlb[61B3 61D4]
Q6710	TRA_MOSFET_PCHN_4P_S C70-6L	mlb[61D6]
Q6711	TRA_DUAL_SSM6N15FE_S OT563	mlb[61D7]
Q6712	TRA_DUAL_SSM6N15FE_S OT563	mlb[61C4]
Q6722	TRA_DUAL_SSM6N15FE_S OT563	mlb[61C4]
Q6730	TRA_MOSFET_PCHN_4P_S C70-6L	mlb[61C2]
Q6740	TRA_MOSFET_PCHN_4P_S C70-6L	mlb[61C2]
Q6760	TRA_MOSFET_PCHN_8P4_ 23V1K-SM	mlb[61B2]
Q6821	TRA_SSM3K15FV_SOD-VE -HF	mlb[62A3]
Q6822	TRA_SINGLE_MOSFET_PC HN_SOT-23-HF	mlb[62B1]
Q6825	TRA_2N7002DW_SOT-363	mlb[62A2 62A3]
Q6850	TRA_NMOSFET_NPN_8P_D FN2015H4-8	mlb[62C7]
Q7100	TRA_DUAL_MOSFET_NCHN 9_WPAK2	mlb[64C4]
Q7330	TRA_MOSFET_NCHN_5P1_ HVSON-3333	mlb[66C4]
Q7335	TRA_MOSFET_NCHN_5P5_ HVSON-333	mlb[66C4]
Q7503	TRA_DUAL_MOSFET_NCHN 9_WPAK	mlb[68D5]
Q7523	TRA_DUAL_MOSFET_NCHN 9_WPAK	mlb[68C5]
Q7603	TRA_DUAL_MOSFET_NCHN 9_WPAK2	mlb[69C5]
Q7730	TRA_DUAL_MOSFET_NCHN 9_WPAK2	mlb[70C4]
Q8365	TRA_2N7002DW_SOT-363	mlb[76A3 76A3]
Q8798	TRA_DUAL_SSM6N15FE_S OT563	mlb[80A2]
Q8950	TRA_DUAL_MOSFET_NCHN 9_WPAK	mlb[82D4]
Q9320	TRA_SSM3K15FV_SOD-VE -HF	mlb[86A4]
Q9415	TRA_SSM3K15FV_SOD-VE -HF	mlb[87C4]
Q9420	TRA_2N7002DW_SOT-363	mlb[87C6 87C6]
R0600	RES_402	mlb[6D3]
R0602	RES_402	mlb[6D2]
R0603	RES_402	mlb[6D1]
R0605	RES_402	mlb[6C1]
R0615	RES_402	mlb[6B2]
R0616	RES_402	mlb[6B3]
R0831	RES_402	mlb[8D2]
R0832	RES_402	mlb[8D2]
R1010	RES_402	mlb[10D5]
R1020	RES_402	mlb[10B2]
R1021	RES_402	mlb[10B2]
R1022	RES_402	mlb[10B2]
R1023	RES_402	mlb[10B3]
R1030	RES_402	mlb[10C8]
R1040	RES_402	mlb[10A7]
R1041	RES_402	mlb[10A6]
R1042	RES_402	mlb[10A8]
R1043	RES_402	mlb[10A6]
R1044	RES_402	mlb[10A8]
R1045	RES_402	mlb[10A7]
R1046	RES_402	mlb[10A7]
R1047	RES_402	mlb[10A7]
R1049	RES_402	mlb[10A6]
R1064	RES_402	mlb[10D4]
R1065	RES_402	mlb[10C4]
R1070	RES_402	mlb[10D4]
R1071	RES_402	mlb[10C4]
R1100	RES_402	mlb[11C5]
R1101	RES_402	mlb[11C6]
R1102	RES_402	mlb[11C5]
R1103	RES_402	mlb[11C6]
R1104	RES_402	mlb[11C5]
R1111	RES_402	mlb[11B4]
R1112	RES_402	mlb[11B5]
R1113	RES_402	mlb[11B5]
R1114	RES_402	mlb[11B5]
R1120	RES_402	mlb[11C7]
R1121	RES_402	mlb[11C6]
R1125	RES_402	mlb[11B6]
R1126	RES_402	mlb[11B7]
R1140	RES_402	mlb[11C2]
R1141	RES_402	mlb[11C2]
R1300	RES_402	mlb[13B5]
R1302	RES_402	mlb[13B6]
R1310	RES_402	mlb[13B5]
R1311	RES_402	mlb[13B5]
R1312	RES_402	mlb[13B5]
R1313	RES_402	mlb[13B2]
R1314	RES_402	mlb[13B2]
R1320	RES_402	mlb[13B6]
R1330	RES_402	mlb[13B1]
R1331	RES_402	mlb[13B1]
R1362	RES_402	mlb[13A5]
R1363	RES_402	mlb[13A5]
R1382	RES_402	mlb[13C1]
R1600	RES_402	mlb[15B2]
R1601	RES_0603	mlb[15A7]
R1702	RES_0603	mlb[16A7]
R1800	RES_201	mlb[17A8]
R1801	RES_201	mlb[17A8]
R1802	RES_201	mlb[17B7]
R1803	RES_201	mlb[17B7]
R1810	RES_201	mlb[17A5]
R1811	RES_201	mlb[17A4]
R1812	RES_201	mlb[17A5]
R1813	RES_201	mlb[17A4]
R1820	RES_201	mlb[17D5]
R1830	RES_201	mlb[17C5]
R1831	RES_201	mlb[17C5]
R1832	RES_201	mlb[17B5]
R1833	RES_201	mlb[17A6]
R1840	RES_201	mlb[17A5]
R1841	RES_201	mlb[17A5]
R1842	RES_201	mlb[17B6]
R1843	RES_201	mlb[17B7]
R1844	RES_201	mlb[17B6]
R1845	RES_201	mlb[17B6]
R1846	RES_201	mlb[17B6]
R1847	RES_201	mlb[17A6]
R1848	RES_201	mlb[17B7]
R1849	RES_201	mlb[17A3]
R1853	RES_201	mlb[17A3]
R1854	RES_201	mlb[17A3]
R1855	RES_201	mlb[17A2]
R1860	RES_201	mlb[17D5]
R1861	RES_201	mlb[17D5]
R1862	RES_201	mlb[17D5]
R1863	RES_201	mlb[17D5]
R1864	RES_201	mlb[17D5]
R1866	RES_201	mlb[17A4]
R1869	RES_201	mlb[17B6]
R1870	RES_201	mlb[17A2]
R1871	RES_201	mlb[17A2]
R1876	RES_201	mlb[17B5]
R1877	RES_201	mlb[17B5]
R1878	RES_201	mlb[17B6]
R1879	RES_201	mlb[17C5]
R1890	RES_201	mlb[17D1]
R1891	RES_201	mlb[17A8]
R1892	RES_201	mlb[17A7]
R1893	RES_201	mlb[17A7]
R1894	RES_201	mlb[17A7]
R1895	RES_201	mlb[17A7]
R1896	RES_201	mlb[17A7]
R1897	RES_201	mlb[17A6]
R1900	RES_201	mlb[18D8]
R1905	RES_201	mlb[18D8]
R1909	RES_201	mlb[18B7]
R1915	RES_201	mlb[18B5]
R1920	RES_201	mlb[18C8]
R1921	RES_201	mlb[18A4]
R1922	RES_201	mlb[18A4]
R1924	RES_201	mlb[18A4]
R1925	RES_201	mlb[18A7]
R1951	RES_201	mlb[18B4]
R1980	RES_201	mlb[18B5]
R1981	RES_201	mlb[18C5]
R1982	RES_201	mlb[18A7]
R1983	RES_201	mlb[18A7]
R1985	RES_201	mlb[18A7]
R1986	RES_201	mlb[18B6]
R1991	RES_201	mlb[18A5]
R2010	RES_201	mlb[19D7]
R2011	RES_201	mlb[19D7]
R2012	RES_201	mlb[19D7]
R2013	RES_201	mlb[19D7]
R2014	RES_201	mlb[19D7]
R2016	RES_201	mlb[19D7]
R2017	RES_201	mlb[19D7]
R2018	RES_201	mlb[19D7]
R2030	RES_201	mlb[19D7]
R2031	RES_201	mlb[19D7]
R2052	RES_201	mlb[19A7]
R2053	RES_201	mlb[19A7]
R2054	RES_201	mlb[19A6]
R2060	RES_201	mlb[19C3]
R2061	RES_201	mlb[19C3]
R2062	RES_201	mlb[19C3]
R2064	RES_201	mlb[19C3]
R2065	RES_201	mlb[19C2]
R2067	RES_201	mlb[19C2]
R2068	RES_201	mlb[19C2]
R2069	RES_201	mlb[19C2]
R2070	RES_201	mlb[19B4]
R2111	RES_201	mlb[20D8]
R2112	RES_201	mlb[20D7]
R2113	RES_201	mlb[20D7]
R2114	RES_201	mlb[20A7]
R2115	RES_201	mlb[20A7]
R2116	RES_201	mlb[20A3]
R2117	RES_201	mlb[20A6]
R2118	RES_201	mlb[20A2]
R2130	RES_201	mlb[20A3]
R2140	RES_201	mlb[20D3]
R2150	RES_201	mlb[20D3]
R2155	RES_201	mlb[20D3]
R2156	RES_201	mlb[20C3]
R2160	RES_201	mlb[20B8]
R2170	RES_201	mlb[20D4]
R2172	RES_201	mlb[20A7]
R2173	RES_201	mlb[20A7]
R2174	RES_201	mlb[20A7]
R2175	RES_201	mlb[20A8]
R2184	RES_201	mlb[20B7]
R2185	RES_201	mlb[20B7]
R2186	RES_201	mlb[20B7]
R2190	RES_201	mlb[20D6]
R2191	RES_201	mlb[20A6]
R2192	RES_201	mlb[20C7]
R2193	RES_201	mlb[20C8]
R2194	RES_201	mlb[20C7]
R2196	RES_201	mlb[20A5]
R2197	RES_201	mlb[20A4]
R2198	RES_201	mlb[20A3]
R2199	RES_201	mlb[20A3]
R2404	RES_402	mlb[23B7]
R2405	RES_402	mlb[23C7]
R2415	RES_402	mlb[23D7]
R2450	RES_201	mlb[23C7]
R2451	RES_402	mlb[23C5]
R2490	RES_402	mlb[23B5]
R2491	RES_402	mlb[23B5]
R2500	RES_402	mlb[24C8]
R2501	RES_402	mlb[24C8]
R2502	RES_402	mlb[24C7]
R2504	RES_402	mlb[24C7]
R2505	RES_402	mlb[24C4]
R2510	RES_402	mlb[24D2]
R2511	RES_402	mlb[24D1]
R2512	RES_402	mlb[24D1]
R2513	RES_402	mlb[24D2]
R2514	RES_402	mlb[24D1]
R2515	RES_402	mlb[24C4]
R2516	RES_402	mlb[24C4]
R2520	RES_402	mlb[24B7]
R2521	RES_402	mlb[24B7]
R2522	RES_402	mlb[24A7]
R2523	RES_402	mlb[24A7]
R2524	RES_402	mlb[24A5]
R2526	RES_402	mlb[24A6]
R2530	RES_402	mlb[24C2]
R2531	RES_402	mlb[24B2]
R2532	RES_402	mlb[24B1]
R2540	RES_402	mlb[24D6]
R2550	RES_402	mlb[24A3]
R2551	RES_402	mlb[24A3]
R2552	RES_402	mlb[24A2]
R2553	RES_402	mlb[24B3]
R2556	RES_402	mlb[24A2]
R2557	RES_402	mlb[24B3]
R2600	RES_402	mlb[25C4]
R2601	RES_402	mlb[25C8]
R2602	RES_402	mlb[25C8]
R2603	RES_402	mlb[25C8]
R2604	RES_402	mlb[25C8]
R2605	RES_402	mlb[25C7]
R2606	RES_402	mlb[25C7]
R2607	RES_402	mlb[25C6]
R2620	RES_402	mlb[25C4]
R2621	RES_402	mlb[25C3]
R2622	RES_402	mlb[25C3]
R2630	RES_402	mlb[25C7]
R2640	RES_402	mlb[25C2]
R2641	RES_402	mlb[25B1]
R2642	RES_402	mlb[25B3]
R2650	RES_402	mlb[25A4]
R2651	RES_402	mlb[25B8]
R2652	RES_402	mlb[25A8]
R2653	RES_402	mlb[25B8]
R2654	RES_402	mlb[25A8]
R2655	RES_402	mlb[25B7]
R2656	RES_402	mlb[25A7]
R2657	RES_402	mlb[25A6]
R2670	RES_402	mlb[25A4]
R2671	RES_402	mlb[25A3]
R2672	RES_402	mlb[25A3]
R2680	RES_402	mlb[25B7]
R2705	RES_402	mlb[26C6]
R2706	RES_402	mlb[26C6]
R2740	RES_402	mlb[26D3]
R2741	RES_402	mlb[26D2]
R2743	RES_402	mlb[26C3]
R2745	RES_402	mlb[26C3]
R2800	RES_402	mlb[27D7]
R2810	RES_402	mlb[27C7]
R2811	RES_402	mlb[27C7]
R2826	RES_402	mlb[27B2]
R2827	RES_402	mlb[27B2]
R2829	RES_402	mlb[27B2]
R2840	RES_402	mlb[27C3]
R2850	RES_402	mlb[27A7]
R2860	RES_402	mlb[27A6]
R2861	RES_402	mlb[27A5]
R2862	RES_402	mlb[27A5]
R2863	RES_402	mlb[27A6]
R2871	RES_402	mlb[27C2]
R2875	RES_402	mlb[27D2]
R2876	RES_402	mlb[27D2]
R2877	RES_402	mlb[27D3]
R2879	RES_402	mlb[27D3]
R2880	RES_402	mlb[27B3]
R2881	RES_402	mlb[27C2]
R2883	RES_402	mlb[27C2]
R2888	RES_402	mlb[27D2]
R2895	RES_402	mlb[27A3]
R2896	RES_402	mlb[27A4]
R2897	RES_402	mlb[27A3]
R2901	RES_402	mlb[28C6]
R2902	RES_402	mlb[28B6]
R2905	RES_402	mlb[28D6]
R2910	RES_402	mlb[28C6]
R2915	RES_402	mlb[28B7]
R2916	RES_402	mlb[28B6]
R2917	RES_402	mlb[28A6]
R2920	RES_402	mlb[28C4]
R2921	RES_402	mlb[28C4]
R2922	RES_402	mlb[28D3]
R2923	RES_402	mlb[28C4]
R2950	RES_603	mlb[28B2]
R2951	RES_402	mlb[28B3]
R3140	RES_402	mlb[30B2]
R3141	RES_402	mlb[30B2]
R3240	RES_402	mlb[31B2]
R3241	RES_402	mlb[31B2]
R3401	RES_402	mlb[33D4]
R3402	RES_402	mlb[33C4]
R3403	RES_402	mlb[33D2]
R3404	RES_402	mlb[33D2]
R3405	RES_402	mlb[33D2]
R3406	RES_402	mlb[33C2]
R3407	RES_402	mlb[33B4]
R3408	RES_402	mlb[33B4]
R3409	RES_402	mlb[33C2]
R3410	RES_402	mlb[33C2]
R3411	RES_402	mlb[33C2]
R3412	RES_402	mlb[33B2]
R3413	RES_402	mlb[33B4]
R3414	RES_402	mlb[33B2]
R3415	RES_402	mlb[33A4]
R3418	RES_402	mlb[33D7]
R3419	RES_402	mlb[33C7]
R3502	RES_402	mlb[34D4]
R3505	RES_402	mlb[34D2]
R3510	RES_402	mlb[34B7]
R3511	RES_402	mlb[34B7]

R3512	RES_402	mlb[34B2]
R3514	RES_402	mlb[34B3]
R3530	RES_402	mlb[34B6]
R3531	RES_402	mlb[34B3]
R3535	RES_402	mlb[34A3]
R3555	RES_402	mlb[34C4]
R3560	RES_402	mlb[34C4]
R3561	RES_402	mlb[34C4]
R3562	RES_402	mlb[34C4]
R3563	RES_402	mlb[34C4]
R3564	RES_402	mlb[34C4]
R3565	RES_402	mlb[34C4]
R3566	RES_402	mlb[34C4]
R3567	RES_402	mlb[34C4]
R3601	RES_402	mlb[35D7]
R3640	RES_402	mlb[35B4]
R3650	RES_402	mlb[35C2]
R3651	RES_402	mlb[35C2]
R3653	RES_402	mlb[35B4]
R3654	RES_402	mlb[35A4]
R3800	RES_402	mlb[36B4]
R3801	RES_402	mlb[36B4]
R3802	RES_402	mlb[36B4]
R3803	RES_402	mlb[36B3]
R3910	RES_402	mlb[37C6]
R3930	RES_402	mlb[37B2]
R3940	RES_402	mlb[37C6]
R3941	RES_402	mlb[37C6]
R3942	RES_402	mlb[37C6]
R3943	RES_402	mlb[37B7]
R3950	RES_402	mlb[37B2]
R3951	RES_402	mlb[37B2]
R3952	RES_402	mlb[37B2]
R3953	RES_402	mlb[37B2]
R3965	RES_402	mlb[37A6]
R3971	RES_402	mlb[37B2]
R3974	RES_402	mlb[37B2]
R3975	RES_402	mlb[37B2]
R3976	RES_402	mlb[37B2]
R3977	RES_402	mlb[37B2]
R3978	RES_402	mlb[37B2]
R3980	RES_402	mlb[37B2]
R3990	RES_402	mlb[37A7]
R3997	RES_402	mlb[37A6]
R4010	RES_402	mlb[38B4]
R4011	RES_402	mlb[38A4]
R4012	RES_402	mlb[38A4]
R4019	RES_402	mlb[38B4]
R4050	RES_402	mlb[38C2]
R4110	RES_603	mlb[39D7]
R4117	RES_603	mlb[39D7]
R4119	RES_603	mlb[39D8]
R4125	RES_603	mlb[39D2]
R4129	RES_402	mlb[39D2]
R4135	RES_603	mlb[39D1]
R4140	RES_402	mlb[39C6]
R4141	RES_402	mlb[39C7]
R4150	RES_402	mlb[39B7]
R4151	RES_402	mlb[39B7]
R4152	RES_402	mlb[39B7]
R4153	RES_402	mlb[39B7]
R4160	RES_402	mlb[39B7]
R4162	RES_402	mlb[39A7]
R4170	RES_402	mlb[39C2]
R4171	RES_402	mlb[39C2]
R4175	RES_402	mlb[39B2]
R4180	RES_402	mlb[39A7]
R4181	RES_402	mlb[39A8]
R4182	RES_402	mlb[39A8]
R4183	RES_402	mlb[39A7]
R4184	RES_402	mlb[39A7]
R4185	RES_402	mlb[39B2]
R4186	RES_402	mlb[39B2]
R4190	RES_402	mlb[39C1]
R4191	RES_402	mlb[39C2]
R4250	RES_402	mlb[40C3]
R4251	RES_402	mlb[40C3]
R4252	RES_402	mlb[40C3]
R4253	RES_402	mlb[40C3]
R4254	RES_402	mlb[40B3]
R4255	RES_402	mlb[40B7]
R4256	RES_402	mlb[40B6]
R4257	RES_402	mlb[40A7]
R4258	RES_402	mlb[40A7]
R4300	RES_2512	mlb[41D7]
R4310	RES_402	mlb[41C2]
R4311	RES_402	mlb[41B2]
R4312	RES_402	mlb[41C2]
R4313	RES_402	mlb[41B2]
R4320	RES_402	mlb[41D7]
R4321	RES_402	mlb[41D7]
R4322	RES_402	mlb[41C7]
R4323	RES_402	mlb[41D7]
R4324	RES_402	mlb[41C5]
R4325	RES_402	mlb[41C6]
R4326	RES_402	mlb[41C6]
R4327	RES_402	mlb[41B5]
R4328	RES_402	mlb[41B5]
R4329	RES_402	mlb[41B6]
R4335	RES_402	mlb[41B2]
R4340	RES_402	mlb[41A8]
R4341	RES_402	mlb[41A7]
R4342	RES_402	mlb[41A8]
R4343	RES_402	mlb[41A7]
R4350	RES_402	mlb[41A5]
R4351	RES_402	mlb[41A5]
R4352	RES_402	mlb[41A5]
R4353	RES_402	mlb[41A4]
R4354	RES_402	mlb[41A3]
R4390	RES_402	mlb[41B3]
R4450	RES_201	mlb[42C7]
R4451	RES_201	mlb[42C7]
R4452	RES_201	mlb[42B7]
R4453	RES_201	mlb[42B7]
R4460	RES_201	mlb[42C3]
R4461	RES_201	mlb[42C3]
R4462	RES_201	mlb[42B3]
R4463	RES_201	mlb[42B3]
R4600	RES_402	mlb[43B6]
R4601	RES_402	mlb[43D6]
R4650	RES_402	mlb[43D4]
R4651	RES_402	mlb[43C4]
R4652	RES_402	mlb[43C4]
R4700	RES_402	mlb[44D5]

R4790	RES_402	mlb[44C7]
R4794	RES_402	mlb[44B7]
R4798	RES_402	mlb[44C3]
R4799	RES_402	mlb[44C3]
R4800	RES_402	mlb[45C5]
R4801	RES_402	mlb[45D5]
R4802	RES_402	mlb[45D5]
R4803	RES_402	mlb[45C6]
R4805	RES_402	mlb[45D3]
R4808	RES_402	mlb[45D3]
R4820	RES_402	mlb[45B2]
R4821	RES_805	mlb[45A3]
R4822	RES_805	mlb[45A3]
R4823	RES_402	mlb[45A2]
R4901	RES_201	mlb[46D1]
R4902	RES_201	mlb[46C2]
R4909	RES_201	mlb[46D1]
R4910	RES_402	mlb[46A4]
R4911	RES_402	mlb[46A4]
R4912	RES_402	mlb[46A4]
R4998	RES_201	mlb[46C2]
R4999	RES_402	mlb[46D4]
R5000	RES_402	mlb[47D7]
R5001	RES_603	mlb[47D8]
R5010	RES_402	mlb[47B8]
R5012	RES_402	mlb[47C5]
R5020	RES_201	mlb[47C5]
R5051	RES_201	mlb[47A4]
R5060	RES_402	mlb[47D1]
R5061	RES_402	mlb[47D2]
R5062	RES_402	mlb[47D3]
R5071	RES_201	mlb[47C1]
R5072	RES_201	mlb[47C1]
R5073	RES_201	mlb[47B1]
R5074	RES_201	mlb[47B1]
R5075	RES_201	mlb[47B1]
R5076	RES_201	mlb[47B5]
R5077	RES_201	mlb[47B1]
R5078	RES_201	mlb[47B1]
R5079	RES_201	mlb[47B1]
R5080	RES_201	mlb[47B1]
R5081	RES_201	mlb[47B1]
R5084	RES_201	mlb[47B1]
R5085	RES_201	mlb[47B1]
R5086	RES_201	mlb[47B1]
R5087	RES_201	mlb[47B1]
R5088	RES_201	mlb[47B1]
R5089	RES_201	mlb[47A1]
R5090	RES_201	mlb[47B1]
R5091	RES_201	mlb[47B1]
R5092	RES_201	mlb[47B1]
R5093	RES_201	mlb[47B1]
R5110	RES_402	mlb[48B5]
R5111	RES_402	mlb[48B5]
R5112	RES_402	mlb[48A5]
R5120	RES_402	mlb[48B4]
R5121	RES_402	mlb[48B4]
R5122	RES_402	mlb[48A4]
R5123	RES_402	mlb[48A4]
R5125	RES_402	mlb[48B4]
R5126	RES_402	mlb[48B4]
R5127	RES_402	mlb[48B4]
R5128	RES_402	mlb[48B4]
R5200	RES_402	mlb[49D7]
R5201	RES_402	mlb[49D7]
R5202	RES_402	mlb[49D7]
R5203	RES_402	mlb[49D7]
R5204	RES_402	mlb[49D7]
R5205	RES_402	mlb[49D7]
R5206	RES_402	mlb[49D7]
R5207	RES_402	mlb[49D7]
R5208	RES_402	mlb[49C7]
R5209	RES_402	mlb[49C7]
R5210	RES_402	mlb[49B7]
R5211	RES_402	mlb[49B7]
R5212	RES_402	mlb[49C7]
R5213	RES_402	mlb[49C7]
R5220	RES_402	mlb[49A7]
R5221	RES_402	mlb[49A7]
R5222	RES_402	mlb[49A6]
R5223	RES_402	mlb[49A6]
R5230	RES_402	mlb[49B2]
R5231	RES_402	mlb[49B2]
R5234	RES_402	mlb[49B2]
R5235	RES_402	mlb[49B2]
R5236	RES_402	mlb[49B7]
R5237	RES_402	mlb[49B7]
R5250	RES_402	mlb[49D4]
R5251	RES_402	mlb[49D4]
R5260	RES_402	mlb[49A4]
R5261	RES_402	mlb[49A4]
R5262	RES_402	mlb[49A5]
R5263	RES_402	mlb[49A5]
R5264	RES_402	mlb[49A4]
R5265	RES_402	mlb[49A4]
R5270	RES_402	mlb[49C4]
R5271	RES_402	mlb[49C4]
R5290	RES_402	mlb[49C2]
R5291	RES_402	mlb[49C2]
R5300	RES_SENSE_1206	mlb[50D7]
R5301	RES_402	mlb[50D6]
R5302	RES_402	mlb[50D7]
R5304	RES_402	mlb[50D6]
R5305	RES_SENSE_1206	mlb[50C7]
R5306	RES_402	mlb[50C6]
R5320	RES_402	mlb[50C2]
R5322	RES_402	mlb[50A3]
R5330	RES_402	mlb[50B2]
R5333	RES_402	mlb[50A3]
R5341	RES_402	mlb[50D2]
R5343	RES_402	mlb[50D4]
R5345	RES_402	mlb[50D3]
R5351	RES_402	mlb[50C2]
R5353	RES_402	mlb[50B4]
R5355	RES_402	mlb[50B3]
R5361	RES_402	mlb[50B6]
R5366	RES_402	mlb[50A6]
R5371	RES_402	mlb[50A6]
R5376	RES_402	mlb[50C6]
R5400	RES_SENSE_0612	mlb[51C7]
R5403	RES_402	mlb[51C5]
R5411	RES_402	mlb[51C3]
R5412	RES_402	mlb[51C2]
R5413	RES_402	mlb[51D2]

R5414	RES_402	mlb[51C2]
R5420	RES_SENSE_0612-3	mlb[51B7]
R5423	RES_402	mlb[51A5]
R5433	RES_402	mlb[51D5]
R5493	RES_SENSE_1206	mlb[51D7]
R5500	RES_402	mlb[52D5]
R5501	RES_402	mlb[52D5]
R5502	RES_402	mlb[52D5]
R5536	RES_402	mlb[52B5]
R5537	RES_402	mlb[52B5]
R5600	RES_402	mlb[53D6]
R5601	RES_402	mlb[53C7]
R5602	RES_402	mlb[53C6]
R5603	RES_402	mlb[53B5]
R5650	RES_201	mlb[53A7]
R5700	RES_402	mlb[54D5]
R5701	RES_402	mlb[54D5]
R5703	RES_201	mlb[54C6]
R5705	RES_402	mlb[54C5]
R5706	RES_402	mlb[54C5]
R5800	RES_201	mlb[55B5]
R5801	RES_402	mlb[55C6]
R5802	RES_402	mlb[55C6]
R5803	RES_402	mlb[55C6]
R5804	RES_402	mlb[55C6]
R5805	RES_402	mlb[55B6]
R5806	RES_402	mlb[55B6]
R5807	RES_402	mlb[55B6]
R5808	RES_402	mlb[55B6]
R5902	RES_402	mlb[56B5]
R5903	RES_402	mlb[56B4]
R6060	RES_402	mlb[57B4]
R6090	RES_402	mlb[57C2]
R6091	RES_402	mlb[57C2]
R6100	RES_201	mlb[58B8]
R6101	RES_201	mlb[58C7]
R6102	RES_402	mlb[58B7]
R6103	RES_201	mlb[58C7]
R6105	RES_201	mlb[58C5]
R6106	RES_201	mlb[58C6]
R6111	RES_201	mlb[58A6]
R6112	RES_402	mlb[58A6]
R6113	RES_402	mlb[58A5]
R6114	RES_201	mlb[58A4]
R6160	RES_402	mlb[58A3]
R6161	RES_201	mlb[58B3]
R6162	RES_201	mlb[58B2]
R6163	RES_201	mlb[58B1]
R6164	RES_201	mlb[58B3]
R6180	RES_201	mlb[58C3]
R6181	RES_402	mlb[58C2]
R6182	RES_402	mlb[58C1]
R6183	RES_402	mlb[58C3]
R6184	RES_201	mlb[58C4]
R6185	RES_402	mlb[58C2]
R6186	RES_402	mlb[58D4]
R6401	RES_402	mlb[59C5]
R6500	RES_402	mlb[60C7]
R6501	RES_402	mlb[60C5]
R6502	RES_402	mlb[60D5]
R6506	RES_402	mlb[60C6]
R6599	RES_402	mlb[60C7]
R6700	RES_402	mlb[61D3]
R6701	RES_402	mlb[61B6]
R6702	RES_402	mlb[61D3]
R6710	RES_402	mlb[61D7]
R6711	RES_402	mlb[61D7]
R6730	RES_402	mlb[61C3]
R6732	RES_402	mlb[61C3]
R6740	RES_402	mlb[61B3]
R6742	RES_402	mlb[61C3]
R6760	RES_402	mlb[61B3]
R6762	RES_402	mlb[61B3]
R6811	RES_402	mlb[62D2]
R6812	RES_402	mlb[62D3]
R6821	RES_402	mlb[62B2]
R6822	RES_402	mlb[62B2]
R6840	RES_402	mlb[62D7]
R6841	RES_402	mlb[62D7]
R6851	RES_402	mlb[62C8]
R6852	RES_402	mlb[62C8]
R6853	RES_402	mlb[62C7]
R6854	RES_402	mlb[62C7]
R6855	RES_402	mlb[62B7]
R6856	RES_402	mlb[62C7]
R6857	RES_402	mlb[62B6]
R6860	RES_402	mlb[62A8]
R6861	RES_402	mlb[62A8]
R6862	RES_402	mlb[62A6]
R6863	RES_402	mlb[62A6]
R6864	RES_402	mlb[62A6]
R6865	RES_402	mlb[62A6]
R6866	RES_402	mlb[62A5]
R6867	RES_402	mlb[62B5]
R6868	RES_402	mlb[62B6]
R6869	RES_402	mlb[62B5]
R6870	RES_402	mlb[62A7]
R6871	RES_402	mlb[62A7]
R6872	RES_402	mlb[62A7]
R6873	RES_402	mlb[62A7]
R6874	RES_402	mlb[62C5]
R6875	RES_402	mlb[62B4]
R6876	RES_402	mlb[62C5]
R6878	RES_402	mlb[62C3]
R6881	RES_402	mlb[62C3]
R6886	RES_402	mlb[62C2]
R6887	RES_402	mlb[62C3]
R6888	RES_402	mlb[62C2]
R7101	RES_402	mlb[64C5]
R7102	RES_603	mlb[64C5]
R7103	RES_402	mlb[64B6]
R7104	RES_402	mlb[64C7]
R7120	RES_603	mlb[64C3]
R7130	RES_402	mlb[64C4]
R7140	RES_SENSE_0612	mlb[64C2]
R7141	RES_402	mlb[64B3]
R7142	RES_402	mlb[64B3]
R7146	RES_402	mlb[64C6]
R7147	RES_402	mlb[64B6]
R7148	RES_402	mlb[64B6]
R7160	RES_603	mlb[64B2]
R7202	RES_402	mlb[65D6]
R7203	RES_603	mlb[65D6]
R7204	RES_402	mlb[65D7]

R7205	RES_402	mlb[65C6]
R7208	RES_402	mlb[65C5]
R7209	RES_402	mlb[65C5]
R7210	RES_402	mlb[65C4]
R7211	RES_402	mlb[65C4]
R7214	RES_402	mlb[65C7]
R7215	RES_402	mlb[65C5]
R7251	RES_603	mlb[65B6]
R7254	RES_402	mlb[65B6]
R7255	RES_402	mlb[65A6]
R7256	RES_402	mlb[65A5]
R7257	RES_402	mlb[65A4]
R7258	RES_402	mlb[65A4]
R7259	RES_402	mlb[65A4]
R7260	RES_402	mlb[65A4]
R7261	RES_402	mlb[65A3]
R7301	RES_603	mlb[66C7]
R7305	RES_402	mlb[66B7]
R7310	RES_402	mlb[66B7]
R7320	RES_402	mlb[66B8]
R7321	RES_402	mlb[66B8]
R7330	RES_402	mlb[66C5]
R7331	RES_603	mlb[66C4]
R7340	RES_SENSE_0612	mlb[66C2]
R7405	RES_402	mlb[67D3]
R7406	RES_402	mlb[67D3]
R7408	RES_402	mlb[67C2]
R7418	RES_402	mlb[67B3]
R7419	RES_402	mlb[67B3]
R7420	RES_402	mlb[67B3]
R7422	RES_402	mlb[67B3]
R7424	RES_402	mlb[67A3]
R7426	RES_402	mlb[67A2]
R7427	RES_805	mlb[67D4]
R7428	RES_402	mlb[67D7]
R7429	RES_402	mlb[67C7]
R7432	RES_402	mlb[67C7]
R7433	RES_402	mlb[67C7]
R7434	RES_402	mlb[67C8]
R7435	RES_402	mlb[67B8]
R7440	RES_402	mlb[67C5]
R7441	RES_402	mlb[67C5]
R7442	RES_402	mlb[67C5]
R7443	RES_402	mlb[67C6]
R7444	RES_402	mlb[67B5]
R7445	RES_402	mlb[67B8]
R7446	RES_402	mlb[67B6]
R7447	RES_402	mlb[67B6]
R7448	RES_402	mlb[67B5]
R7449	RES_402	mlb[67B5]
R7450	RES_402	mlb[67B5]
R7451	RES_402	mlb[67B4]
R7452	RES_402	mlb[67B6]
R7454	RES_402	mlb[67A5]
R7455	RES_402	mlb[67B3]
R7456	RES_402	mlb[67C6]
R7457	RES_402	mlb[67D4]
R7458	RES_402	mlb[67B4]
R7459	RES_402	mlb[67A8]
R7460	RES_402	mlb[67D7]
R7462	RES_402	mlb[67D7]
R7464	RES_402	mlb[67D7]
R7465	RES_402	mlb[67D7]
R7466	RES_402	mlb[67A7]
R7467	RES_402	mlb[67A7]
R7468	RES_402	mlb[67A7]
R7469	RES_402	mlb[67A7]
R7470	RES_402	mlb[67A7]
R7471	RES_402	mlb[67A7]
R7479	RES_402	mlb[67A5]
R7480	RES_402	mlb[67B2]
R7481	RES_402	mlb[67A3]
R7489	RES_402	mlb[67C5]
R7495	RES_402	mlb[67D3]
R7499	RES_402	mlb[67B5]
R7501	RES_402	mlb[68D3]
R7504	RES_402	mlb[68D6]
R7505	RES_603	mlb[68D7]
R7506	RES_603	mlb[68D4]
R7521	RES_402	mlb[68B3]
R7524	RES_402	mlb[68C6]
R7525	RES_603	mlb[68C7]
R7526	RES_603	mlb[68C4]
R7601	RES_603	mlb[69C7]
R7604	RES_402	mlb[69C6]
R7606	RES_603	mlb[69C4]
R7608	RES_402	mlb[69C3]
R7620	RES_SENSE_0612	mlb[69C3]
R7701	RES_402	mlb[70C5]
R7702	RES_603	mlb[70C5]
R7703	RES_402	mlb[70B6]
R7704	RES_402	mlb[70C7]
R7705	RES_402	mlb[70B7]
R7730	RES_402	mlb[70C5]
R7731	RES_603	mlb[70C3]
R7740	RES_SENSE_0612	mlb[70C3]
R7741	RES_402	mlb[70B3]
R7742	RES_402	mlb[70B3]
R7744	RES_402	mlb[70C7]
R7745	RES_402	mlb[70B7]
R7760	RES_603	mlb[70C1]
R7860	RES_402	mlb[71C6]
R7861	RES_402	mlb[71C5]
R7862	RES_402	mlb[71C5]
R7863	RES_402	mlb[71D5]
R7865	RES_402	mlb[71C7]
R7870	RES_402	mlb[71B7]
R7920	RES_402	mlb[72C6]
R8001	RES_402	mlb[73B1]
R8002	RES_402	mlb[73B1]
R8005	RES_402	mlb[73B3]
R8010	RES_402	mlb[73B3]
R8200	RES_402	mlb[75A8]
R8201	RES_402	mlb[75A8]
R8202	RES_402	mlb[75A7]
R8203	RES_402	mlb[75A7]
R8204	RES_402	mlb[75A6]
R8205	RES_402	mlb[75A6]
R8206	RES_402	mlb[75A4]
R8207	RES_402	mlb[75A4]
R8210	RES_402	mlb[75B8]
R8211	RES_402	mlb[75B8]
R8212	RES_402	mlb[75B8]
R8213	RES_402	mlb[75A8]

R8214	RES_402	mlb[75A8]
R8215	RES_402	mlb[75A8]
R8250	RES_402	mlb[75B5]
R8251	RES_402	mlb[75A3]
R8252	RES_402	mlb[75A3]
R8260	RES_402	mlb[75A2]
R8261	RES_402	mlb[75B2]
R8262	RES_402	mlb[75B1]
R8300	RES_402	mlb[76D5]
R8301	RES_402	mlb[76C3]
R8302	RES_402	mlb[76D3]
R8303	RES_402	mlb[76C5]
R8304	RES_402	mlb[76C4]
R8305	RES_402	mlb[76C3]
R8330	RES_402	mlb[76A8]
R8331	RES_402	mlb[76A7]
R8332	RES_402	mlb[76A7]
R8333	RES_402	mlb[76A7]
R8340	RES_402	mlb[76C7]
R8341	RES_402	mlb[76C7]
R8342	RES_402	mlb[76C7]
R8343	RES_402	mlb[76C7]
R8351	RES_603	mlb[76B5]
R8352	RES_402	mlb[76A3]
R8354	RES_402	mlb[76B5]
R8355	RES_402	mlb[76A5]
R8356	RES_402	mlb[76B4]
R8357	RES_402	mlb[76A3]
R8358	RES_402	mlb[76A3]
R8359	RES_402	mlb[76A3]
R8360	RES_402	mlb[76A4]
R8361	RES_402	mlb[76B3]
R8362	RES_402	mlb[76A3]
R8400	RES_402	mlb[77D6]
R8401	RES_402	mlb[77C4]
R8402	RES_402	mlb[77C4]
R8403	RES_402	mlb[77C6]
R8404	RES_402	mlb[77C5]
R8405	RES_402	mlb[77C4]
R8500	RES_201	mlb[78C8]
R8501	RES_402	mlb[78D7]
R8502	RES_402	mlb[78D7]
R8503	RES_201	mlb[78C7]
R8504	RES_201	mlb[78C8]
R8530	RES_402	mlb[78B6]
R8531	RES_402	mlb[78B6]
R8532	RES_402	mlb[78B6]
R8533	RES_402	mlb[78A6]
R8534	RES_402	mlb[78A6]
R8535	RES_402	mlb[78A6]
R8550	RES_201	mlb[78C4]
R8551	RES_402	mlb[78D4]
R8552	RES_402	mlb[78D4]
R8553	RES_201	mlb[78C4]
R8554	RES_201	mlb[78C4]
R8580	RES_402	mlb[78B2]
R8581	RES_402	mlb[78B2]
R8582	RES_402	mlb[78B2]
R8583	RES_402	mlb[78A2]
R8584	RES_402	mlb[78B1]
R8585	RES_402	mlb[78B1]
R8600	RES_402	mlb[79C6]
R8601	RES_402	mlb[79C6]
R8602	RES_402	mlb[79B6]
R8603	RES_402	mlb[79B6]
R8604	RES_402	mlb[79C2]
R8605	RES_402	mlb[79C2]
R8606	RES_402	mlb[79B1]
R8607	RES_402	mlb[79B1]
R8610	RES_402	mlb[79D7]
R8611	RES_402	mlb[79D6]
R8612	RES_402	mlb[79D6]
R8613	RES_402	mlb[79D6]
R8700	RES_402	mlb[80C8]
R8701	RES_402	mlb[80C7]
R8702	RES_402	mlb[80C7]
R8703	RES_402	mlb[80C8]
R8704	RES_402	mlb[80C7]
R8705	RES_402	mlb[80C7]
R8706	RES_402	mlb[80B8]
R8707	RES_402	mlb[80B7]
R8708	RES_402	mlb[80B7]
R8709	RES_402	mlb[80B8]
R8710	RES_402	mlb[80B7]
R8711	RES_402	mlb[80B7]
R8712	RES_402	mlb[80A8]
R8713	RES_402	mlb[80A7]
R8714	RES_402	mlb[80A7]
R8720	RES_402	mlb[80C6]
R8721	RES_402	mlb[80C6]
R8722	RES_402	mlb[80C6]
R8723	RES_402	mlb[80C6]
R8724	RES_402	mlb[80C6]
R8725	RES_402	mlb[80C6]
R8726	RES_402	mlb[80C5]
R8730	RES_402	mlb[80C1]
R8731	RES_402	mlb[80C1]
R8740	RES_402	mlb[80D7]
R8741	RES_402	mlb[80D7]
R8742	RES_402	mlb[80D7]
R8743	RES_402	mlb[80D7]
R8744	RES_402	mlb[80D6]
R8745	RES_402	mlb[80D6]
R8750	RES_402	mlb[80A6]
R8780	RES_402	mlb[80B6]
R8781	RES_402	mlb[80A6]
R8790	RES_402	mlb[80B4]
R8791	RES_402	mlb[80B3]
R8792	RES_402	mlb[80A4]
R8793	RES_402	mlb[80A4]
R8794	RES_402	mlb[80A4]
R8795	RES_402	mlb[80B3]
R8796	RES_402	mlb[80B4]
R8797	RES_402	mlb[80B4]
R8798	RES_402	mlb[80B3]
R8799	RES_402	mlb[80B3]
R8800	RES_402	mlb[81D4]
R8801	RES_402	mlb[81C7]
R8802	RES_402	mlb[81D7]
R8900	RES_402	mlb[82B5]
R8901	RES_402	mlb[82B5]
R8902	RES_402	mlb[82B5]
R8903	RES_402	mlb[82B4]
R8904	RES_402	mlb[82D8]

R8905	RES_402	mlb[82D7]
R8907	RES_402	mlb[82C7]
R8908	RES_402	mlb[82C7]
R8909	RES_402	mlb[82C7]
R8910	RES_402	mlb[82C7]
R8911	RES_603	mlb[82D8]
R8912	RES_402	mlb[82D5]
R8920	RES_402	mlb[82C7]
R8924	RES_402	mlb[82C7]
R8925	RES_402	mlb[82B8]
R8930	RES_402	mlb[82D4]
R8940	RES_SENSE_0612	mlb[82C3]
R8950	RES_402	mlb[82B8]
R8951	RES_402	mlb[82B8]
R8953	RES_402	mlb[82B7]
R8980	RES_603	mlb[82C4]
R8982	RES_402	mlb[82A6]
R8983	RES_402	mlb[82A6]
R8984	RES_402	mlb[82A6]
R8985	RES_402	mlb[82A6]
R8987	RES_402	mlb[82A7]
R8988	RES_402	mlb[82A7]
R8990	RES_402	mlb[82A8]
R8991	RES_402	mlb[82A5]
R8992	RES_402	mlb[82A5]
R8993	RES_402	mlb[82A8]
R8994	RES_402	mlb[82A8]
R8995	RES_402	mlb[82A6]
R8996	RES_402	mlb[82A6]
R8998	RES_402	mlb[82A8]
R9010	RES_402	mlb[83D5]
R9011	RES_402	mlb[83D5]
R9021	RES_402	mlb[83C6]
R9022	RES_402	mlb[83C6]
R9023	RES_402	mlb[83C6]
R9025	RES_402	mlb[83C6]
R9029	RES_402	mlb[83B6]
R9030	RES_402	mlb[83B6]
R9031	RES_402	mlb[83A6]
R9032	RES_402	mlb[83A3]
R9051	RES_402	mlb[83D2]
R9055	RES_603	mlb[83C3]
R9085	RES_402	mlb[83A3]
R9090	RES_402	mlb[83C8]
R9091	RES_402	mlb[83C8]
R9092	RES_402	mlb[83C6]
R9093	RES_402	mlb[83C6]
R9095	RES_402	mlb[83C2]
R9096	RES_402	mlb[83C2]
R9098	RES_402	mlb[83C2]
R9099	RES_402	mlb[83B3]
R9120	RES_402	mlb[84C7]
R9150	RES_402	mlb[84D2]
R9160	RES_402	mlb[84C2]
R9203	RES_402	mlb[85C7]
R9207	RES_402	mlb[85C6]
R9210	RES_402	mlb[85A7]
R9215	RES_402	mlb[85C7]
R9221	RES_201	mlb[85B2]
R9222	RES_201	mlb[85B2]
R9223	RES_201	mlb[85B2]
R9224	RES_201	mlb[85B2]
R9225	RES_201	mlb[85A4]
R9226	RES_201	mlb[85A2]
R9227	RES_201	mlb[85A2]
R9228	RES_201	mlb[85B4]
R9230	RES_201	mlb[85B4]
R9231	RES_201	mlb[85B4]
R9300	RES_402	mlb[86B5]
R9301	RES_402	mlb[86B5]
R9302	RES_402	mlb[86B8]
R9308	RES_402	mlb[86C7]
R9309	RES_402	mlb[86D7]
R9310	RES_402	mlb[86B8]
R9311	RES_402	mlb[86B8]
R9312	RES_402	mlb[86B8]
R9318	RES_402	mlb[86B7]
R9319	RES_402	mlb[86B8]
R9330	RES_402	mlb[86A8]
R9334	RES_402	mlb[86A4]
R9335	RES_402	mlb[86A5]
R9336	RES_402	mlb[86A5]
R9338	RES_402	mlb[86A4]
R9339	RES_402	mlb[86A3]
R9350	RES_201	mlb[86C5]
R9351	RES_201	mlb[86C5]
R9352	RES_201	mlb[86C5]
R9353	RES_201	mlb[86C4]
R9354	RES_201	mlb[86C5]
R9355	RES_201	mlb[86C5]
R9360	RES_201	mlb[86C2]
R9361	RES_201	mlb[86C2]
R9364	RES_201	mlb[86C2]
R9365	RES_201	mlb[86C2]
R9372	RES_201	mlb[86D3]
R9373	RES_201	mlb[86D3]
R9374	RES_201	mlb[86D1]
R9375	RES_201	mlb[86D1]
R9382	RES_201	mlb[86D3]
R9383	RES_201	mlb[86D3]
R9384	RES_201	mlb[86C1]
R9385	RES_201	mlb[86C1]
R9392	RES_402	mlb[86B4]
R9393	RES_402	mlb[86B4]
R9396	RES_402	mlb[86B3]
R9397	RES_402	mlb[86B3]
R9398	RES_402	mlb[86B1]
R9399	RES_402	mlb[86B2]
R9401	RES_201	mlb[87A5]
R9402	RES_201	mlb[87A5]
R9403	RES_201	mlb[87B6]
R9404	RES_201	mlb[87B6]
R9407	RES_201	mlb[87B2]
R9408	RES_201	mlb[87A2]
R9410	RES_402	mlb[87C1]
R9411	RES_402	mlb[87C1]
R9412	RES_402	mlb[87C3]
R9416	RES_402	mlb[87D3]
R9417	RES_402	mlb[87D3]
R9418	RES_603	mlb[87D1]
R9421	RES_402	mlb[87D6]
R9422	RES_402	mlb[87D7]
R9423	RES_402	mlb[87D6]
R9424	RES_402	mlb[87D5]

R9425	RES_402	mlb[87D5]
R9426	RES_402	mlb[87C6]
R9430	RES_402	mlb[87C8]
R9431	RES_1206	mlb[87D8]
R9432	RES_1206	mlb[87D8]
R9441	RES_201	mlb[87A6]
R9450	RES_603	mlb[87D4]
R9451	RES_201	mlb[87A7]
R9452	RES_201	mlb[87A7]
R9470	RES_201	mlb[87B2]
R9471	RES_201	mlb[87B2]
R9472	RES_201	mlb[87A2]
R9473	RES_201	mlb[87A2]
R9494	RES_201	mlb[87B7]
R9495	RES_201	mlb[87B7]
R9498	RES_201	mlb[87B8]
R9499	RES_201	mlb[87B7]
R9724	RES_402	mlb[88A6]
R9725	RES_402	mlb[88A7]
R9726	RES_402	mlb[88A5]
R9740	RES_402	mlb[88B5]
R9741	RES_402	mlb[88B5]
R9750	RES_402	mlb[88B7]
R9753	RES_402	mlb[88C7]
R9754	RES_402	mlb[88B7]
R9755	RES_402	mlb[88C7]
R9756	RES_402	mlb[88B6]
R9757	RES_402	mlb[88C6]
R9758	RES_402	mlb[88B6]
R9759	RES_402	mlb[88C6]
R9761	RES_402	mlb[88C6]
R9762	RES_402	mlb[88B3]
R9763	RES_402	mlb[88C3]
R9764	RES_402	mlb[88B3]
R9765	RES_402	mlb[88C3]
R9766	RES_402	mlb[88B3]
R9768	RES_402	mlb[88B3]
R9769	RES_402	mlb[88C3]
R9810	RES_402	mlb[89B5]
R9811	RES_402	mlb[89B5]
R9812	RES_402	mlb[89B5]
R9813	RES_402	mlb[89A5]
R9814	RES_402	mlb[89A5]
RT7403	THERMISTER_0603	mlb[67D4]
RT7404	THERMISTER_0603	mlb[67B7]
S9200	SHLD_1P_SM	mlb[85D5]
S9201	SHLD_1P_SM	mlb[85D3]
S9202	SHLD_1P_SM	mlb[85D2]
S9203	SHLD_1P_SM	mlb[85D4]
S9204	SHLD_1P_SM	mlb[85D3]
S9205	SHLD_1P_SM	mlb[85D5]
S9206	SHLD_1P_SM	mlb[85D3]
S9207	SHLD_1P_SM	mlb[85D2]
S9208	SHLD_1P_SM	mlb[85D4]
S9209	SHLD_1P_SM	mlb[85D3]
S9210	SHLD_1P_SM	mlb[85D5]
S9211	SHLD_1P_SM	mlb[85D3]
S9212	SHLD_1P_SM	mlb[85D2]
S9213	SHLD_1P_SM	mlb[85D4]
S9214	SHLD_1P_SM	mlb[85D3]
S9215	SHLD_1P_SM	mlb[85D5]
S9216	SHLD_1P_SM	mlb[85D3]
S9217	SHLD_1P_SM	mlb[85D2]
S9218	SHLD_1P_SM	mlb[85D4]
S9219	SHLD_1P_SM	mlb[85D3]
S9220	SHLD_1P_SM	mlb[85C5]
S9221	SHLD_1P_SM	mlb[85C3]
S9222	SHLD_1P_SM	mlb[85C2]
S9223	SHLD_1P_SM	mlb[85C4]
S9224	SHLD_1P_SM	mlb[85C3]
S9225	SHLD_1P_SM	mlb[85C5]
S9226	SHLD_1P_SM	mlb[85C3]
S9227	SHLD_1P_SM	mlb[85C2]
S9228	SHLD_1P_SM	mlb[85C4]
S9229	SHLD_1P_SM	mlb[85C3]
SDF3600	PCB_STANDOFF	mlb[35A7]
SDF3601	PCB_STANDOFF	mlb[35A7]
SDF3602	PCB_STANDOFF	mlb[35A6]
SL9202	SLOT_TH-SP	mlb[85D6]
SL9203	SLOT_TH-SP	mlb[85D6]
T3801	XFR_TLA_6T213LF_SM	mlb[36C5]
T3802	XFR_TLA_6T213LF_SM	mlb[36C5]
TP4700	TP_TH-TP30	mlb[44C3]
TP4701	TP_TH-TP30	mlb[44C3]
TP4702	TP_TH-TP30	mlb[44C3]
TP4709	TP_TH-TP30	mlb[44C3]
U1000	SANDY_1023BGA_BGA	mlb[10D3 10D7]
U1000	SANDY_1023BGA_BGA	mlb[11C4]
U1000	SANDY_1023BGA_BGA	mlb[12D3 12D7]
U1000	SANDY_1023BGA_BGA	mlb[13D3 13D8]
U1000	SANDY_1023BGA_BGA	mlb[14D5 14D7]
U1800	COUGARPOINT_MOBILE_F CBGA	mlb[17D3 17D7]
U1800	COUGARPOINT_MOBILE_F CBGA	mlb[18D3 18D7]
U1800	COUGARPOINT_MOBILE_F CBGA	mlb[19D5]
U1800	COUGARPOINT_MOBILE_F CBGA	mlb[20D5]
U1800	COUGARPOINT_MOBILE_F CBGA	mlb[21D7 21C3]
U1800	COUGARPOINT_MOBILE_F CBGA	mlb[22D3 22D6]
U2150	MC74VHC1G08_SC70-HF	mlb[20C3]
U2151	MC74VHC1G08_SC70-HF	mlb[20B3]
U2152	MC74VHC1G08_SC70-HF	mlb[20B3]
U2520	SN74LV4066ARGYR_QFN1	mlb[24A7 24A7 24B7 24B7]
U2600	USB2513B_QFN	mlb[25D6]
U2650	USB2513B_QFN	mlb[25B6]
U2700	SLG3NB148_TQFN	mlb[26D5]
U2840	SN74LVC1G17_SOT553_S OT-553	mlb[27C3]
U2850	MC74VHC1G08_SC70-HF	mlb[27A7]
U2860	MC74VHC1G08_SC70-HF	mlb[27A6]
U2880	SN74LVC1G07_SC70	mlb[27C3]
U3400	DAC5574_MSOP	mlb[33D6]
U3401	PCA9557RGY_QFN	mlb[33C6]
U3402	OPAMP_MAX4253_UCSP_U CSP	mlb[33D3 33C3]
U3403	OPAMP_MAX4253_UCSP_U CSP	mlb[33B3 33C3]
U3404	OPAMP_MAX4253_UCSP_U CSP	mlb[33B3 33A3]
U3500	SWI_TPS2065_DGN	mlb[34D3]

U3530	SLG4AP014_TDFN	mlb[34B5]
U3535	SLG4AP014_TDFN	mlb[34B5]
U3640	SLG4AP016_TDFN	mlb[35B3]
U3900	BCM57765_1_QFN-8X8	mlb[37C5]
U3990	FLASH_AT45DB011D_SOI C-8S1	mlb[37A7]
U4100	XIO2211_1SYM_BGA	mlb[39C5]
U4200	LREG_TPS799195_SON	mlb[40D7]
U4300	COMPARATOR_LM393_SOI -HF	mlb[41A7 41A4]
U4600	SWI_TPS2561_SON	mlb[43C7]
U4601	SWI_TPS2561_SON	mlb[43D7]
U4650	PI3USB102_TQFN	mlb[43D4]
U4700	CY7C63833_QFN	mlb[44C5]
U4900	H8S2117RP_TLP-145V	mlb[46D3 46B7 46D7]
U5010	VREF_SN0903048_DFN	mlb[47D7]
U5050	NC7SB3157_SC70	mlb[47A5]
U5300	INA210_SC70	mlb[50D7]
U5305	INA210_SC70	mlb[50C7]
U5340	OPAMP_OPA2333_DFN	mlb[50C3 50D3]
U5360	INA210_SC70	mlb[50B7]
U5365	INA210_SC70	mlb[50B7]
U5370	INA214_SC70	mlb[50A7]
U5375	INA210_SC70	mlb[50C7]
U5400	INA210_SC70	mlb[51C7]
U5403	INA214_SC70	mlb[51D7]
U5420	INA210_SC70	mlb[51B7]
U5500	EMC1428_QFN	mlb[52D6]
U5535	EMC1414_MSOP10_MSOP	mlb[52B6]
U5600	CS4206B_QFN	mlb[53D5]
U5601	MAX8840_UDFN	mlb[53A5]
U5800	AMP_MAX97220_TQFN	mlb[55C4]
U5900	AUDIO_MAX98300_WLP	mlb[56C5]
U6106	CD3282A1_WCSP	mlb[58D3]
U6400	FLASH_MX25L6406E_SOI C	mlb[59C5]
U6701	SLG5AP021_TDFN	mlb[61B7]
U6860	ISL88042_TDFN	mlb[62A7]
U7100	ISL95870A_UTQFN	mlb[64C5]
U7201	SC414_MLPQ	mlb[65D6]
U7251	IR3859MPBF_QFN	mlb[65B6]
U7300	TPS51916_QFN	mlb[66C6]
U7400	ISL6364_QFN	mlb[67C4]
U7501	ISL6620A_QFN	mlb[68D7]
U7521	ISL6609_QFN1	mlb[68C7]
U7601	ISL6620A_QFN	mlb[69C7]
U7700	ISL95870_UTQFN	mlb[70C6]
U7860	TPS54218_QFN	mlb[71D7]
U7870	LREG_TPS720XX_DRV_SO N	mlb[71B6]
U8000	WHISTLER_FCBGA	mlb[73D2]
U8000	WHISTLER_FCBGA	mlb[74D5]
U8000	WHISTLER_FCBGA	mlb[75D4 75D7]
U8000	WHISTLER_FCBGA	mlb[79B3 79D5]
U8000	WHISTLER_FCBGA	mlb[81D2 81D3 81D7]
U8300	TPS54320_QFN	mlb[76D5]
U8351	IR3859MPBF_QFN	mlb[76B5]
U8400	TPS54320_QFN	mlb[77C5]
U8500	SGRAM_32MX32_GDDR5_1 70BGA_MFL_BGA	mlb[78C7 78D6]
U8550	SGRAM_32MX32_GDDR5_1 70BGA_MFL_BGA	mlb[78D3 78C3]
U8700	CLK_GEN_SL16010DC_TD FN	mlb[80C2]
U8701	FLASH_M25P10A_UFDFPN 8_UFDFPN8	mlb[80C5]
U8900	ISL6263C_QFN	mlb[82D6]
U9000	T29_FCBGA	mlb[83D4]
U9000	T29_FCBGA	mlb[84D5]
U9090	EEPROM_M95320_MLP8_M LP	mlb[83C7]
U9200	SLG4AP016_TDFN	mlb[85C7]
U9210	TPS22924_CSP	mlb[85B7]
U9215	TPS22924_CSP	mlb[85A7]
U9216	TPS22924_CSP	mlb[85A7]
U9310	PS8301_A2_QFN	mlb[86C6]
U9330	LPC1112A_HVQFN25_HVQ FN25	mlb[86A6]
U9359	SN74LVC1G04_SC70	mlb[86C3]
U9390	CBTL04DP081_HVQFN	mlb[86B2]
U9401	ISL88101B_DFN	mlb[87D7]
U9410	SN1010017_QFN	mlb[87D2]
U9420	MC74VHC1G08_SC70-HF	mlb[87C7]
U9740	PS8171_QFN	mlb[88D4]
U9800	SWI_TPS2051B_SOT23	mlb[89D3]
XW0700	SHORT_SM	mlb[7D8]
XW0701	SHORT_SM	mlb[7C8]
XW4020	SHORT_SM	mlb[38C6]
XW4300	SHORT_SM	mlb[41D3]
XW4301	SHORT_SM	mlb[41D8]
XW4302	SHORT_SM	mlb[41D7]
XW4900	SHORT_SM	mlb[46C2]
XW5320	SHORT_SM	mlb[50C3]
XW5322	SHORT_SM	mlb[50A4]
XW5330	SHORT_SM	mlb[50B3]
XW5333	SHORT_SM	mlb[50A4]
XW5500	SHORT_SM	mlb[52C7]
XW5501	SHORT_SM	mlb[52C7]
XW5504	SHORT_SM	mlb[52C6]
XW5505	SHORT_SM	mlb[52C6]
XW5530	SHORT_SM	mlb[52A6]
XW5531	SHORT_SM	mlb[52A6]
XW5600	SHORT_SM	mlb[53A6]
XW5601	SHORT_SM	mlb[53A6]
XW5610	SHORT_SM	mlb[53D2]
XW5800	SHORT_SM	mlb[55B3]
XW6100	SHORT_SM	mlb[58B2]
XW7100	SHORT_SM	mlb[64B5]
XW7201	SHORT_SM	mlb[65C5]
XW7202	SHORT12LP25_WITH_ALT S_SHORT-12L-0.25MM-S M	mlb[65C4]
XW7251	SHORT_SM	mlb[65A6]
XW7300	SHORT_SM	mlb[66B6]
XW7335	SHORT12LP25_WITH_ALT S_SHORT-12L-0.25MM-S M	mlb[66B3]
XW7360	SHORT12LP25_WITH_ALT S_SHORT-12L-0.25MM-S M	mlb[66C5]
XW7401	SHORT12LP25_WITH_ALT S_SHORT-12L-0.25MM-S M	mlb[67C5]
XW7402	SHORT12LP25_WITH_ALT	mlb[67A7]

	S_SHORT-12L-0.25MM-S M	
XW7420	SHORT_SM	mlb[67D8]
XW7423	SHORT_SM	mlb[67A8]
XW7430	SHORT_SM	mlb[67D8]
XW7433	SHORT_SM	mlb[67A8]
XW7501	SHORT_SM	mlb[68D3]
XW7502	SHORT_SM	mlb[68D3]
XW7521	SHORT_SM	mlb[68C3]
XW7522	SHORT_SM	mlb[68C3]
XW7700	SHORT_SM	mlb[70B6]
XW7801	SHORT_SM	mlb[71C6]
XW8100	SHORT_SM	mlb[74B7]
XW8351	SHORT_SM	mlb[76A5]
XW8600	SHORT_SM	mlb[79A8]
XW8601	SHORT_SM	mlb[79A8]
XW8602	SHORT_SM	mlb[79B3]
XW8900	SHORT_SM	mlb[82A6]
XW8940	SHORT_SM	mlb[82C3]
XW8941	SHORT_SM	mlb[82C3]
Y2600	CRYSTAL_5X3.2X1.4-SM	mlb[25D7]
Y2650	CRYSTAL_5X3.2X1.4-SM	mlb[25B7]
Y2705	CRYSTAL_4PIN_SM-3.2X 2.5MM	mlb[26C7]
Y2810	CRYSTAL_4PIN_SM-2	mlb[27C6]
Y4190	OSC_4PIN_TSNC_SM	mlb[39C1]
Y5010	CRYSTAL_5X3.2-SM	mlb[47B7]
Y8700	CRYSTAL_4PIN_SM-2.5X 2.0MM	mlb[80B3]
ZH0930	HOLE_VIA	mlb[9B8]
ZH0931	HOLE_VIA	mlb[9B8]
ZH0932	HOLE_VIA	mlb[9A8]
ZH0933	HOLE_VIA	mlb[9A8]
ZH0934	HOLE_VIA	mlb[9A8]
ZH0935	HOLE_VIA	mlb[9B8]
ZH0936	HOLE_VIA	mlb[9A8]
ZH0937	HOLE_VIA	mlb[9A8]
ZH0938	HOLE_VIA	mlb[9A8]
ZH0940	HOLE_VIA	mlb[9B7]
ZH0941	HOLE_VIA	mlb[9B7]
ZH0942	HOLE_VIA	mlb[9A7]
ZH0943	HOLE_VIA	mlb[9A7]
ZH0944	HOLE_VIA	mlb[9A7]
ZH0945	HOLE_VIA	mlb[9B7]
ZH0946	HOLE_VIA	mlb[9A7]
ZH0947	HOLE_VIA	mlb[9A7]
ZH0948	HOLE_VIA	mlb[9A7]
ZH0949	HOLE_VIA	mlb[9A7]
ZH0950	HOLE_VIA	mlb[9B7]
ZH0951	HOLE_VIA	mlb[9B7]
ZH0952	HOLE_VIA	mlb[9A7]
ZH0953	HOLE_VIA	mlb[9A7]
ZH0954	HOLE_VIA	mlb[9A7]
ZH0955	HOLE_VIA	mlb[9B6]
ZH0956	HOLE_VIA	mlb[9B6]
ZH0957	HOLE_VIA	mlb[9A6]
ZH0958	HOLE_VIA	mlb[9A6]
ZP0900	POGO_PIN_1P_SM	mlb[9D4]
ZP0901	POGO_PIN_1P_SM	mlb[9D4]
ZP0902	POGO_PIN_1P_SM	mlb[9D3]
ZP0903	POGO_PIN_1P_SM	mlb[9D3]
ZP0907	POGO_PIN_1P_SM	mlb[9D1]
ZP0920	POGO_PIN_1P_SM	mlb[9C3]
ZP0921	POGO_PIN_1P_SM	mlb[9C3]
ZP0922	POGO_PIN_1P_SM	mlb[9C2]
ZP0923	POGO_PIN_1P_SM	mlb[9C2]
ZT0840	PCB_STANDOFF	mlb[8C1]
ZT0841	PCB_STANDOFF	mlb[8C1]
ZT0850	PCB_STANDOFF	mlb[8B1]
ZT0851	PCB_STANDOFF	mlb[8B1]
ZT0910	BOSS	mlb[9C8]
ZT0911	BOSS	mlb[9B8]
ZT0912	BOSS	mlb[9C7]
ZT0913	BOSS	mlb[9B7]
ZT0914	BOSS	mlb[9B8]
ZT0915	BOSS	mlb[9B7]
ZT0940	PCB_STANDOFF	mlb[9C8]
ZT0941	PCB_STANDOFF	mlb[9C6]
ZT0960	PCB_STANDOFF	mlb[9D8]
ZT0961	PCB_STANDOFF	mlb[9D6]
ZT0962	PCB_STANDOFF	mlb[9D8]
ZT0966	PCB_STANDOFF	mlb[9D7]
ZT0970	PCB_STANDOFF	mlb[9C3]